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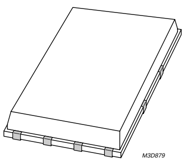


PHM21NQ15T

TrenchMOS™ standard level FET

Rev. 02 — 11 September 2003 **Product data**

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- SOT96 (SO8) footprint compatible
- Surface mounted package
- Low thermal resistance
- Low profile.

1.3 Applications

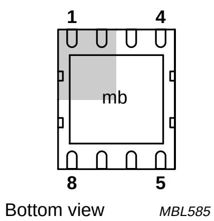
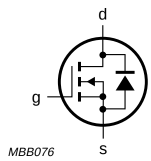
- DC-to-DC primary side
- Portable equipment applications.

1.4 Quick reference data

- $V_{DS} \leq 150$ V
- $P_{tot} \leq 62.5$ W
- $I_D \leq 22.2$ A
- $R_{DSon} \leq 55$ mΩ

2. Pinning information

Table 1: Pinning - SOT685-1 (QLPAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s) [1]		
4	gate (g)		
5,6,7,8	drain (d)		
mb	mounting base connected to drain		

SOT685-1(QLPAK)

[1] Shaded area indicates pin 1 identifier.

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PHM21NQ15T	QLPAK	Plastic surface mounted package; no leads; 8 terminals	SOT685

4. Limiting values

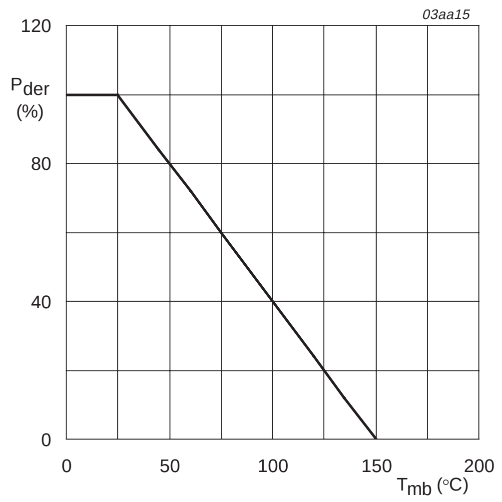
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 150 °C		-	150	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ		-	150	V
V_{GS}	gate-source voltage (DC)			-	±20	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 10 V; Figure 2 and 3		-	22.2	A
		T_{mb} = 100 °C; V_{GS} = 10 V; Figure 2		-	14	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3		-	60	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1		-	62.5	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–55	+150	°C
Source-drain diode						
I_S	source (diode forward) current (DC)	T_{mb} = 25 °C		-	22.2	A
I_{SM}	peak source (diode forward) current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs		-	60	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 12 A; t_p = 0.21 ms; V_{DD} ≤ 150 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting T_j = 25 °C		-	250	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	unclamped inductive load; I_D = 1.2 A; t_p = 0.021 ms; V_{DD} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V	[1] [2]	-	2.5	mJ

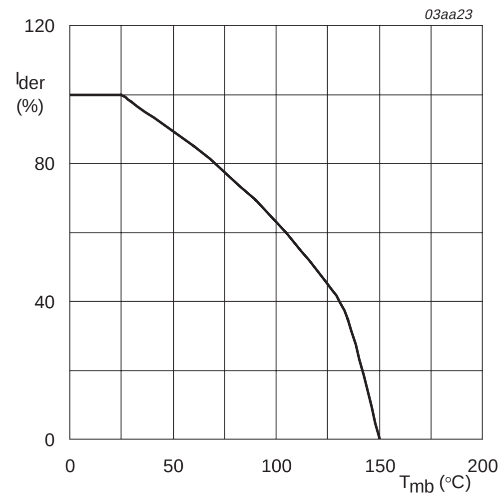
[1] Duty cycle limited by maximum junction temperature.

[2] Repetitive avalanche failure is not determined simply by thermal effects. Repetitive avalanche transients should only be applied for short bursts, not every switching cycle.



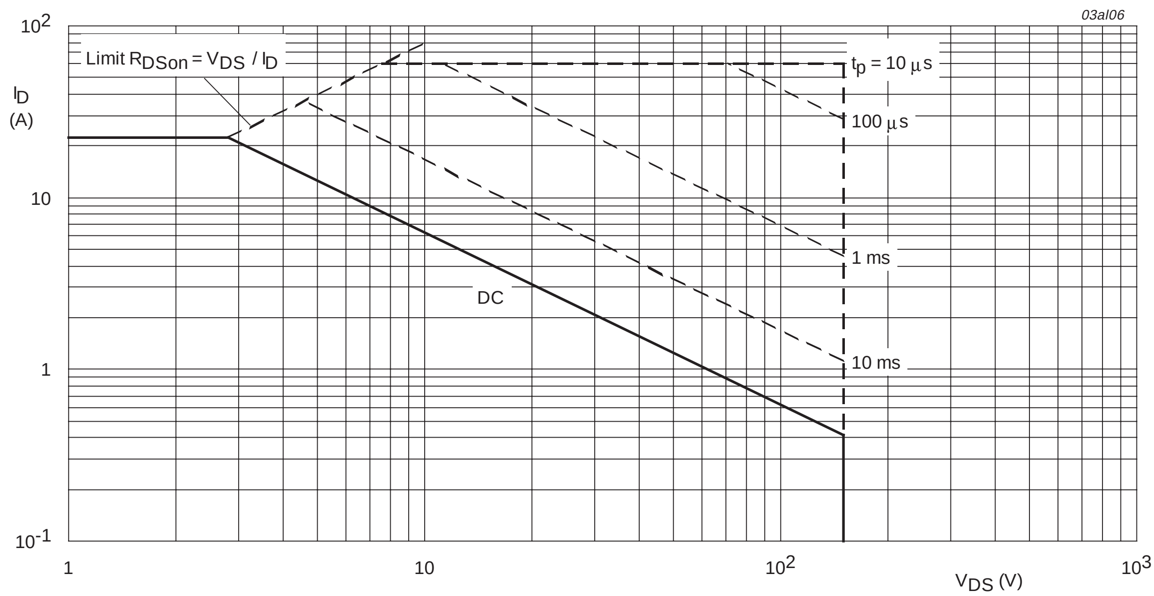
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse; V_{GS} = 10 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

5.1 Transient thermal impedance

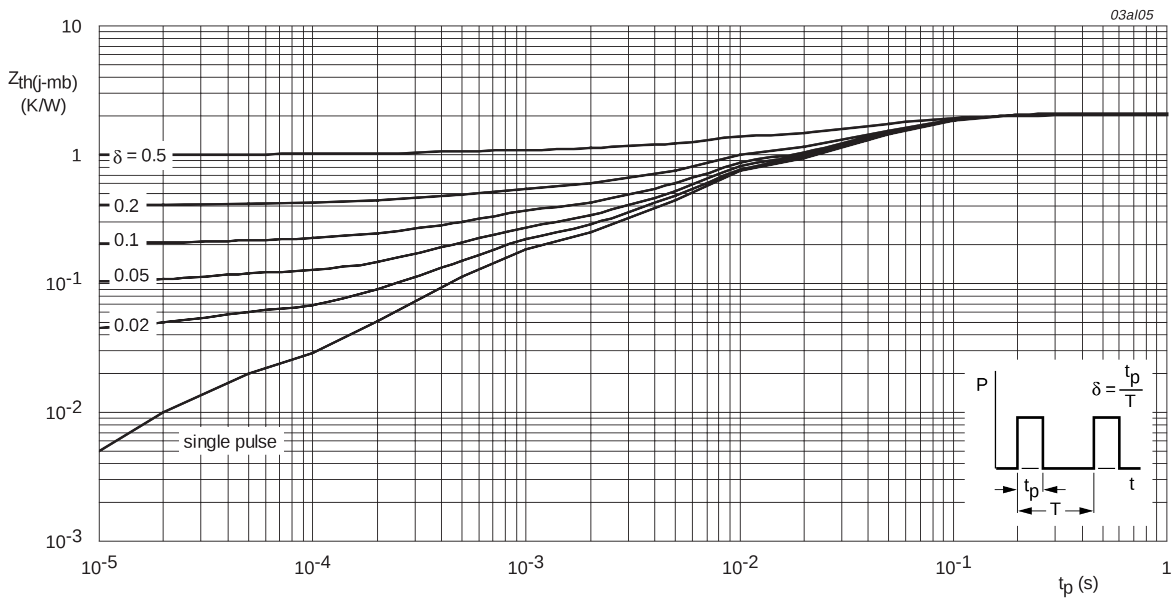


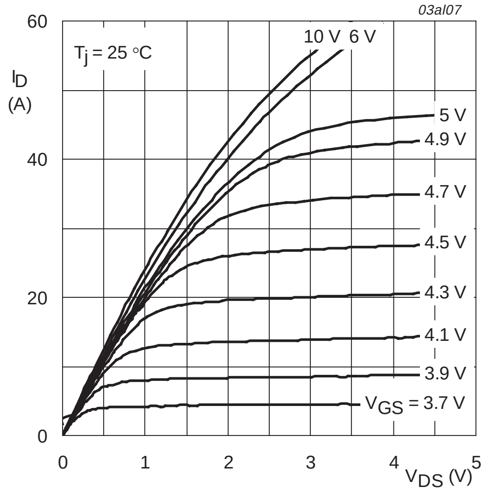
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

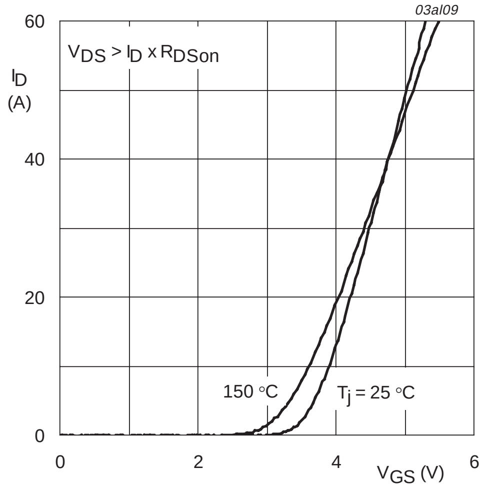
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	150	-	-	V
		T_j = –55 °C	134	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				
		T_j = 25 °C	2	3	4	V
		T_j = 150 °C	1.2	-	-	V
		T_j = –55 °C	-	-	4.4	V
I_{DSS}	drain-source leakage current	V_{DS} = 120 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	1	µA
		T_j = 150 °C	-	-	100	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A; Figure 7 and 8				
		T_j = 25 °C	-	40	55	mΩ
		T_j = 150 °C	-	92	127	mΩ
		V_{GS} = 5 V; I_D = 3 A; Figure 7 and 8	-	42	-	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 20 A; V_{DD} = 75 V; V_{GS} = 10 V; Figure 13	-	36.2	-	nC
Q_{gs}	gate-source charge		-	8	-	nC
Q_{gd}	gate-drain (Miller) charge		-	11.6	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 11	-	2080	-	pF
C_{oss}	output capacitance		-	285	-	pF
C_{rss}	reverse transfer capacitance		-	90	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 75 V; R_L = 75 Ω; V_{GS} = 10 V; R_G = 5.6 Ω	-	16	-	ns
t_r	rise time		-	12	-	ns
$t_{d(off)}$	turn-off delay time		-	50	-	ns
t_f	fall time		-	38	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 10 A; V_{GS} = 0 V; Figure 12	-	0.83	1.2	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V	-	150	-	ns
Q_r	recovered charge		-	215	-	nC



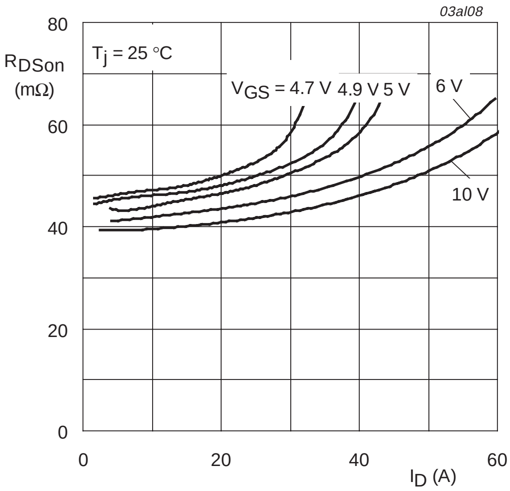
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



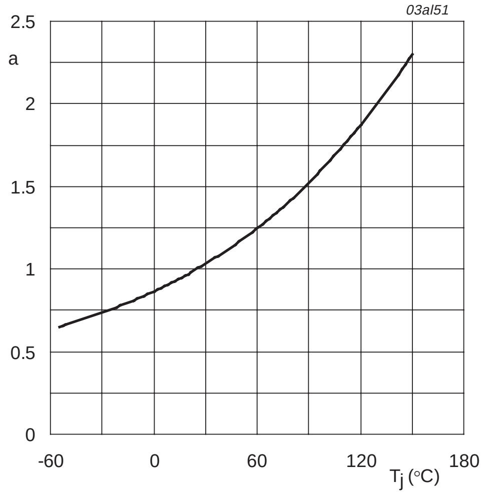
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



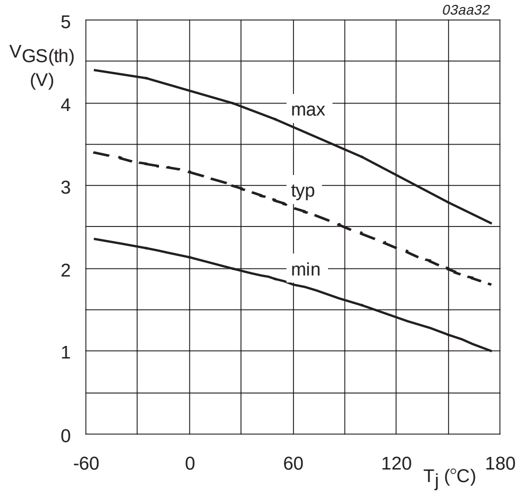
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



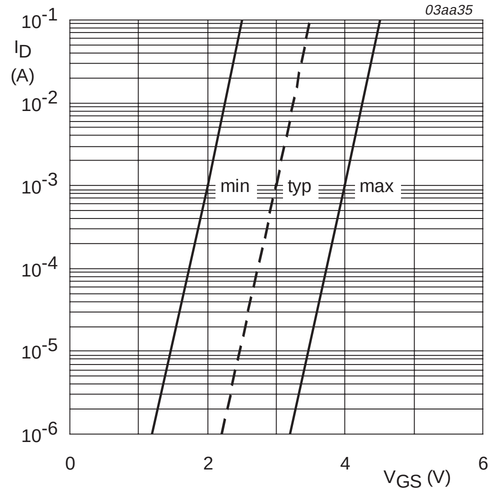
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



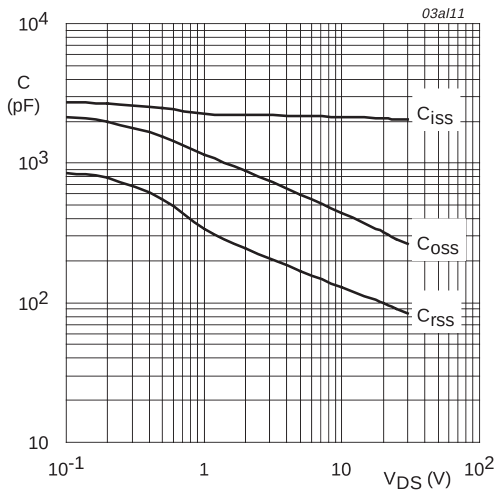
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



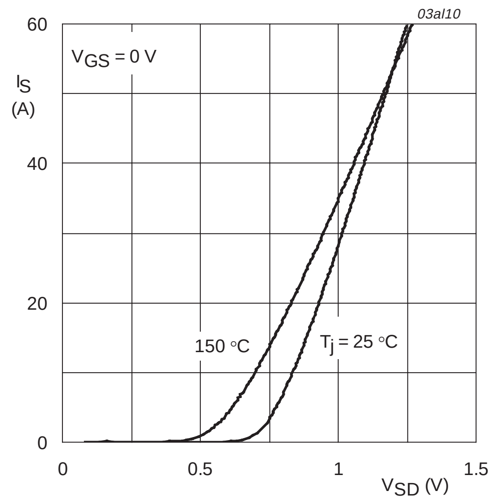
T_j = 25 °C

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



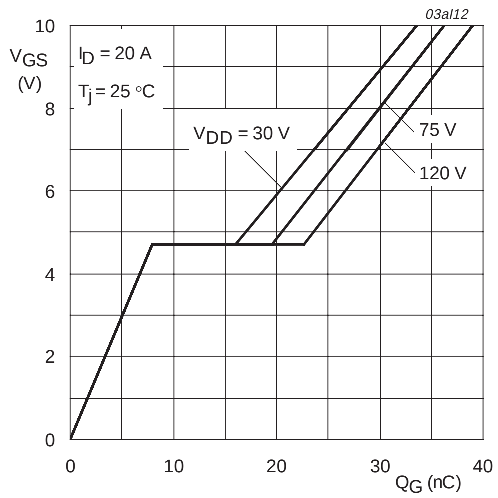
V_{GS} = 0 V; f = 1 MHz

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

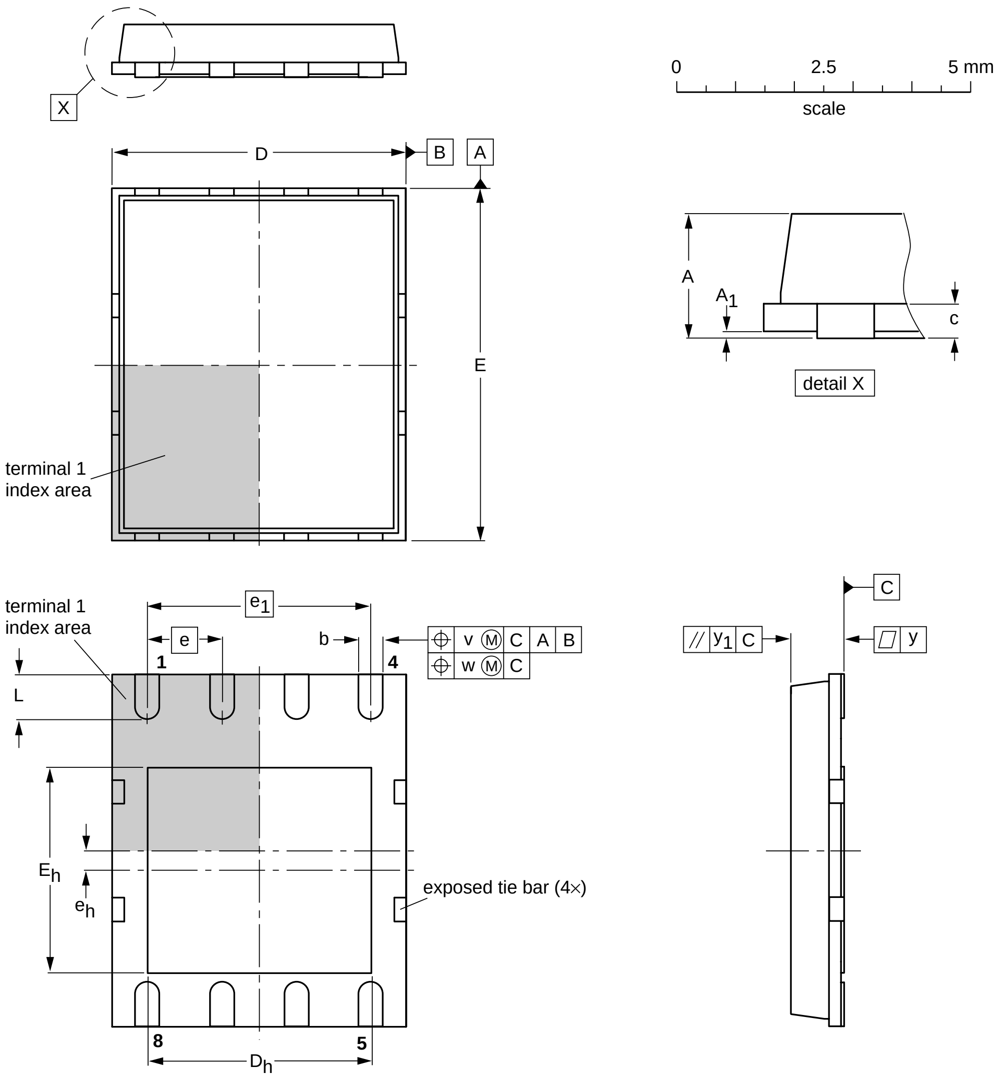


I_D = 20 A; V_{DD} = 30 V, 75 V, 120 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 6 x 5 x 0.85 mm **SOT685-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A (1) max.	A_1	b	c	D (1)	D_h	E (1)	E_h	e	e_1	e_h	L	v	w	y	y_1
mm	1	0.05 0.00	0.5 0.3	0.2	5.15 4.85	3.95 3.65	6.15 5.85	3.65 3.35	1.27	3.81	0.35	0.75 0.50	0.1	0.05	0.05	0.1

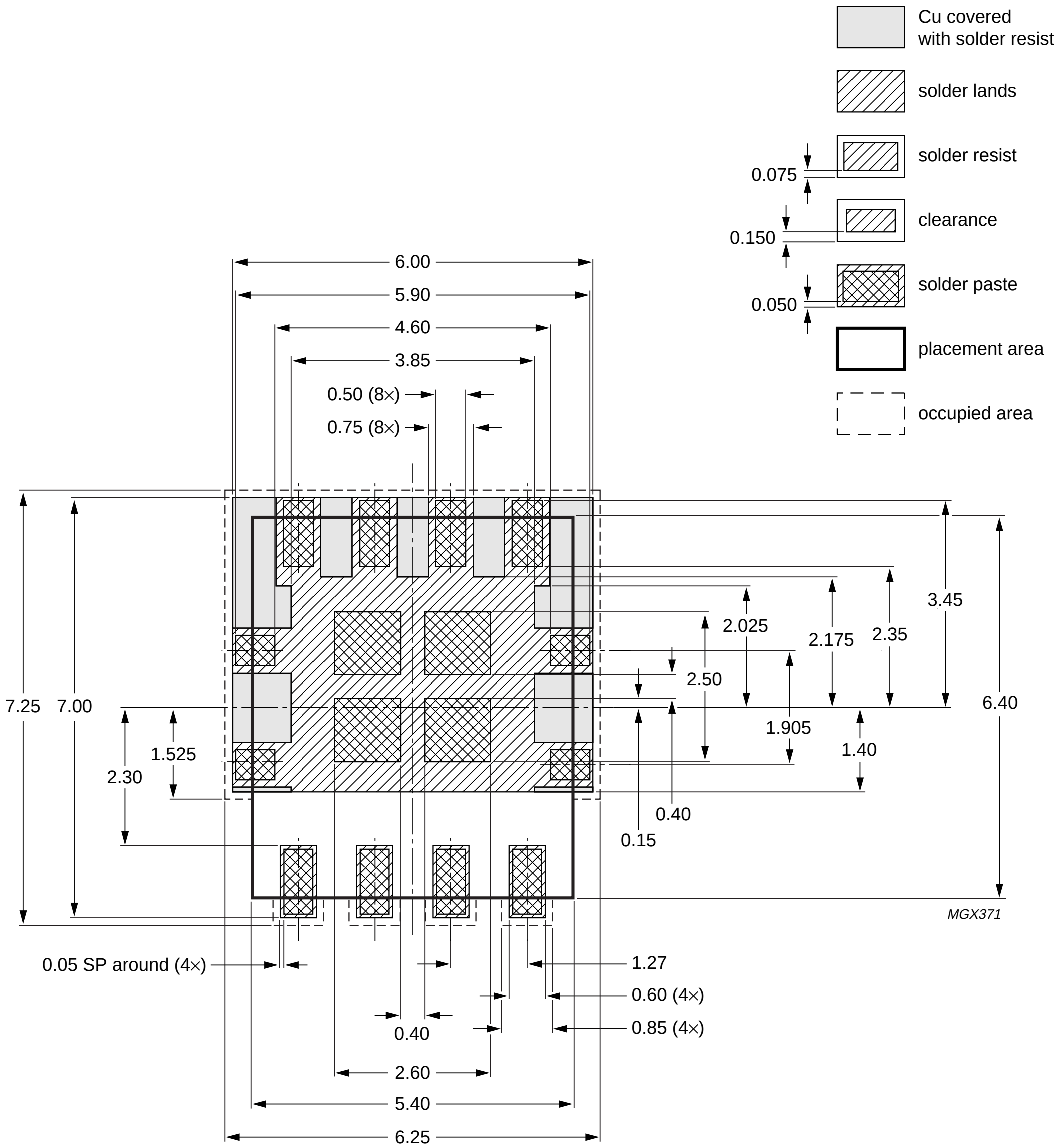
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT685-1		- - -				~~02-08-12~~ 02-11-27

Fig 14. SOT685-1 (QLPAK).

8. Soldering



Dimensions in mm.

Fig 15. Reflow soldering footprint for SOT685-1 (QLPAK).

9. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20030911	-	**Product data (9397 750 11844)** Modifications: • Section 3 “Ordering information” Addition of ordering information. • Section 4 “Limiting values” Addition of $E_{DS(AL)S}$. • Section 4 “Limiting values” Addition of $E_{DS(AL)R}$. • Section 8 “Soldering” Addition of soldering footprint.
01	20030130	-	**Preliminary data (9397 750 10882); initial version.**

10. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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