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TISP6NTP2C

**QUAD FORWARD-CONDUCTING P-GATE THYRISTORS
 PROGRAMMABLE OVERVOLTAGE PROTECTORS**



TISP6NTP2C High Voltage Ringing SLIC Protector

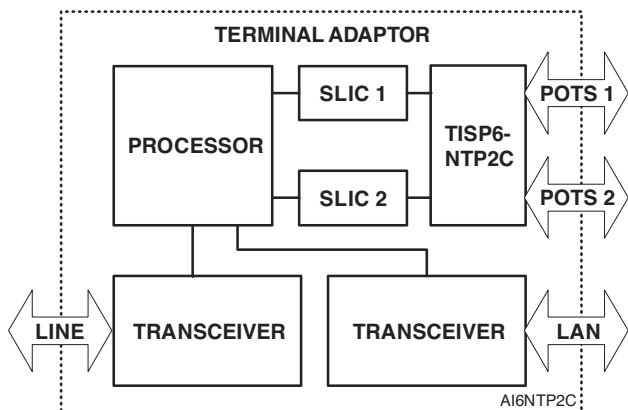
Independent Tracking Overvoltage Protection for Two SLICs:

- Dual Voltage-Programmable Protectors
- Supports Battery Voltages Down to -155 V
- Low 5 mA max. Gate Triggering Current
- High 150 mA min. (70 °C) Holding Current
- Specified 2/10 Limiting Voltage
- Small Outline Surface Mount Package
- Full 0 °C to 70 °C Temperature Range

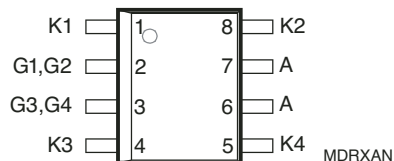
Rated for Common Impulse Waveforms

| Voltage Impulse Wave Shape | Current Impulse Wave Shape | I _{PPSM} A |
|-------------------------------|-------------------------------|------------------------|
| 10/1000 | 10/1000 | 25 |
| 10/700 | 5/310 | 40 |
| 2/10 | 2/10 | 90 |

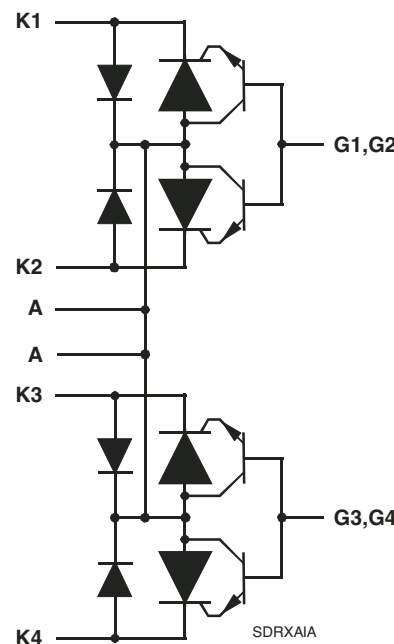
Typical TISP6NTP2C Router Application



D Package (Top View)



Device Symbol



UL **UL Recognized Components**

Description

- The TISP6NTP2C has been designed for short loop systems such as:
- WILL (Wireless In the Local Loop)
 - SOHO (Small Office Home Office)
 - FITL (Fibre In The Loop)
 - ISDN-TA (Integrated Services Digital Network - Terminal Adaptors)
 - DAML (Digital Added Main Line, Pair Gain)

How to Order

| Device | Package | Carrier | Order As |
|------------|-------------------------|--------------------------|----------------|
| TISP6NTP2C | D (8-pin Small-Outline) | R (Embossed Tape Reeled) | TISP6NTP2CDR-S |

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex
 MARCH 2002 – REVISED JULY 2008
 Specifications are subject to change without notice.
 Customers should verify actual device performance in their specific applications.

TISP6NTP2C High Voltage Ringing SLIC Protector



Description (Continued)

The systems described often have the need to source two POTS (Plain Old Telephone Service) lines, one for a telephone and the other for a facsimile machine. In a single surface mount package, the TISP6NTP2C protects the two POTS line SLICs (Subscriber Line Interface Circuits) against overvoltages caused by lightning, a.c. power contact and induction.

The TISP6NTP2C has an array of four buffered P-gate forward conducting thyristors with twin commoned gates and a common anode connection. Each thyristor cathode has a separate terminal connection. An antiparallel anode-cathode diode is connected across each thyristor. The buffer transistors reduce the gate supply current.

In use, the cathodes of an TISP6NTP2C thyristors are connected to the four conductors of two POTS lines (see applications information). Each gate is connected to the appropriate negative voltage battery feed of the SLIC driving that line pair. By having separate gates, each SLIC can be protected at a voltage level related to the negative supply voltage of that individual SLIC. The anode of the TISP6NTP2C is connected to the SLIC common. The TISP6NTP2C voltage and current ratings also make it suitable for the protection of ISDN d.c. feeds of down to -115 V (ETSI Technical Report ETR 080:1993, ranges 1 to 5).

Positive overvoltages are clipped to common by forward conduction of the TISP6NTP2C antiparallel diode. Negative overvoltages are initially clipped close to the SLIC negative supply by emitter follower action of the TISP6NTP2C buffer transistor. If sufficient clipping current flows, the TISP6NTP2C thyristor will regenerate and switch into a low voltage on-state condition. As the overvoltage subsides, the high holding current of the TISP6NTP2C helps prevent d.c. latchup.

Absolute Maximum Ratings, 0 °C ≤ T_J ≤ 70 °C (Unless Otherwise Noted)

| Rating | Symbol | Value | Unit |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|---------------------------------|------|
| Repetitive peak off-state voltage, V _{GK} = 0 | V _{DRM} | -170 | V |
| Repetitive peak gate-cathode voltage, V _{KA} = 0 | V _{GKRM} | -167 | V |
| Non-repetitive peak on-state pulse current (see Notes 1 and 2) 10/1000 (Telcordia (Bellcore) GR-1089-CORE, Issue 2, February 1999, Section 4) 5/320 (ITU-T K.20, K.21 & K.45, K.44 open-circuit voltage wave shape 10/700) 2/10 (Telcordia (Bellcore) GR-1089-CORE, Issue 2, February 1999, Section 4) | I _{PPSM} | 25 40 90 | A |
| Non-repetitive peak on-state current, 50 Hz/60 Hz (see Notes 1 and 2) 0.1 s 1 s 5 s 300 s 900 s | I _{TSM} | 7 2.7 1.5 0.45 0.43 | A |
| Non-repetitive peak gate current, 1/2 μs pulse, cathodes commoned (see Note 1) | I _{GSM} | +25 | A |
| Operating free-air temperature range | T _A | -40 to +85 | °C |
| Junction temperature | T _J | -40 to +150 | °C |
| Storage temperature range | T _{stg} | -40 to +150 | °C |

NOTES: 1. Initially, the protector must be in thermal equilibrium. The surge may be repeated after the device returns to its initial conditions. Gate voltage range is -20 V to -155 V.

2. These non-repetitive rated currents are peak values for either polarity. The rated current values may be applied to any cathode-anode terminal pair. Additionally, all cathode-anode terminal pairs may have their rated current values applied simultaneously (in this case the anode terminal current will be four times the rated current value of an individual terminal pair).

Recommended Operating Conditions

| Component | | Min | Typ | Max | Unit |
|----------------|----------------------------------------------------------------------------------------------|-----|-----|-----|------|
| C _G | Gate decoupling capacitor | 100 | 220 | | nF |
| R _S | Series resistor for GR-1089-CORE intra-building surge survival, section 4.5.9, tests 1 and 2 | 5 | 50 | | Ω |
| | Series resistor for K.20, K.21 and K.45 coordination with a 400 V primary protector | 10 | 50 | | Ω |

TISP6NTP2C High Voltage Ringing SLIC Protector



Electrical Characteristics, 0 °C ≤ T_J ≤ 70 °C (Unless Otherwise Noted)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------|------|-----|------|------|
| I _D Off-state current | V _D = V _{DRM} , V _{GK} = 0 T _J = 25 °C | | | -5 | μA |
| | | | | -50 | μA |
| V _(BO) Ramp breakover voltage | UL 497B, dv/dt ≤ ±100 V/μs, di/dt = ±10 A/μs, V _{GG} = -100 V, Maximum ramp value = ±10 A T _J = 25 °C | | | -112 | V |
| V _(BO) Impulse breakover voltage | 2/10 μs, I _{TM} = -27 A, di/dt = -27 A/μs, R _S = 50 Ω, V _{GG} = -100 V, (see Note 3) | | | -115 | V |
| V _{GK(BO)} Gate-cathode impulse breakover voltage | 2/10 μs, I _{TM} = -27 A, di/dt = -27 A/μs, R _S = 50 Ω, V _{GG} = -100 V, (see Note 3) | | | 15 | V |
| V _F Forward voltage | I _F = 5 A, t _w = 200 μs | | | 3 | V |
| V _{FRM} Ramp peak forward recovery voltage | UL 497B, dv/dt ≤ ±100 V/μs, di/dt = ±10 A/μs, Maximum ramp value = ±10 A T _J = 25 °C | | | 5 | V |
| V _{FRM} Impulse peak forward recovery voltage | 2/10 μs, I _{TM} = -27 A, di/dt = -27 A/μs, R _S = 50 Ω, (see Note 3) | | | 12 | V |
| I _H Holding current | I _T = -1 A, di/dt = 1A/ms, V _{GG} = -100 V | -150 | | | mA |
| I _{GKS} Gate reverse current | V _{GG} = V _{GK} = V _{GKRM} , V _{KA} = 0 T _J = 25 °C | | | -5 | μA |
| | | | | -50 | μA |
| I _{GT} Gate trigger current | I _T = -3 A, t _{p(g)} ≥ 20 μs, V _{GG} = -100 V T _J = 25 °C | | | 5 | mA |
| | | | | 6 | mA |
| V _{GT} Gate-cathode trigger voltage | I _T = -3 A, t _{p(g)} ≥ 20 μs, V _{GG} = -100 V | | | 2.5 | V |
| C _{KA} Cathode-anode off-state capacitance | f = 1 MHz, V _d = 1 V, I _G = 0, (see Note 4) V _D = -3 V V _D = -48 V | | | 100 | pF |
| | | | | 50 | pF |

NOTES: 3. GR-1089-CORE intra-building 2/10, 1.5 kV conditions with 20 MHz bandwidth. The diode forward recovery and the thyristor gate impulse breakover (overshoot) are not strongly dependent of the SLIC supply voltage value (V_{GG}).

4. These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

Thermal Characteristics

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|----------------------------------------------------------|-----------------------------------------------------------------------------------------------|-----|-----|-----|------|
| R _{θJA} Junction to free air thermal resistance | T _A = 70 °C, EIA/JESD51-3 PCB, EIA/JESD51-2 environment, P _{tot} = 0.52 W | | | 160 | °C/W |

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Parameter Measurement Information

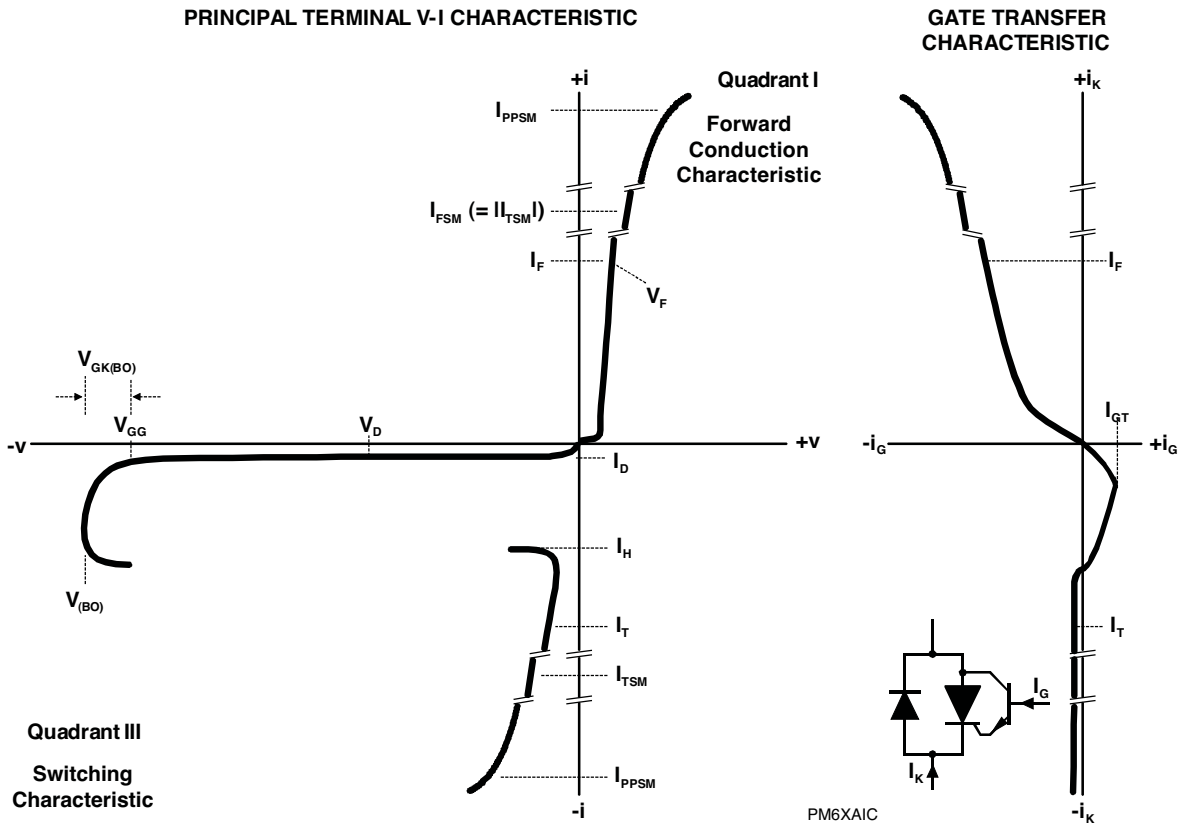


Figure 1. Principal Terminal and Gate Transfer Characteristics

TISP6NTP2C High Voltage Ringing SLIC Protector



APPLICATIONS INFORMATION

SLIC Protection

The generation of POTS lines at the customer premise normally uses a ringing SLIC. Although the lines are short, a central office ringing voltage level is often required for fax machine operation. High voltage SLICs are now available that can produce adequate ringing voltage (see table). The TISP6NTP2C has been designed to work with these SLICs which use battery voltages, V_{BATH} , down to -150 V. Figure 2 shows a typical example with one TISP6NTP2C protecting two SLICs.

The table below shows some details of HV SLICs using multiple negative supply rails.

| Manufacturer | INFINEON‡ | LEGERITY™‡ | | | | Unit |
|---------------------------|------------|------------|------------|------------|-------|------|
| SLIC Series | SLIC-P‡ | ISLIC™‡ | | | | |
| SLIC # | PEB 4266 | 79R241 | 79R101 | 79R100 | | |
| Data Sheet Issue | 14/02/2001 | -/08/2000 | -/07/2000 | -/07/2000 | | |
| Short Circuit Current | 110 | 150 | 150 | 150 | mA | |
| V_{BATH} max. | -155 | -104 | -104 | -104 | V | |
| V_{BATL} max. | -150 | -104 | V_{BATH} | V_{BATH} | V | |
| AC Ringing for: | 85 | 45† | 50† | 55† | V rms | |
| Crest Factor | 1.4 | 1.4 | 1.4 | 1.25 | | |
| V_{BATH} | -70 | -90 | -99 | -99 | V | |
| V_{BATR} | -150 | -36 | -24 | -24 | V | |
| R or T Overshoot < 250 ns | | -15 15 | -20 12 | -20 12 | V | |
| Line Feed Resistance | 20 + 30 | 50 | 50 | 50 | Ω | |

† Assumes -20 V battery voltage during ringing.

‡ Legerity, the Legerity logo and ISLIC are the trademarks of Legerity, Inc.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

ISDN Protection

For voltage feed protection, the cathodes of an TISP6NTP2C thyristors are connected to the four conductors to be protected (see Figure 3). Each gate is connected to the appropriate negative voltage feed. The anode of the TISP6NTP2C is connected to the system common. Positive overvoltages are clipped to common by forward conduction of the TISP6NTP2C antiparallel diode. Negative overvoltages are initially clipped close to the negative supply by emitter follower action of the TISP6NTP2C buffer transistor. If sufficient clipping current flows, the TISP6NTP2C thyristor will regenerate and switch into a low voltage on-state condition. As the negative overvoltage subsides, the high holding current of the TISP6NTP2C prevents d.c. latchup.

Voltage Stress Levels

Figure 4 shows the protector electrodes. The package terminal designated gate, G, is the transistor base, B, electrode connection and so is marked as B (G). The following junctions are subject to voltage stress: Transistor EB and CB, SCR AK (off state) and the antiparallel diode (reverse blocking). This clause covers the necessary testing to ensure the junctions are good.

Testing transistor CB and EB: The maximum voltage stress level for the TISP6NTP2C is V_{BATH} with the addition of the short term antiparallel diode voltage overshoot, V_{FRM} . The current flowing out of the G terminal is measured at V_{BATH} plus V_{FRM} . The SCR K terminal is shorted to the common (0 V) for this test (see Figure 4). The measured current, I_{GKS} , is the sum of the junction currents I_{CB} and I_{EB} .

Testing transistor CB, SCR AK off state and diode reverse blocking: The highest AK voltage occurs during the overshoot period of the protector. To make sure that the SCR and diode blocking junctions do not break down during this period, a d.c. test for off-state current, I_D , can be applied at the overshoot voltage value. To avoid transistor CB current amplification by the transistor gain, the transistor base-emitter is shorted during this test (see Figure 5).

Summary: Two tests are need to verify the protector junctions. Maximum current values for I_{GKS} and I_D are required at the specified applied voltage conditions.

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APPLICATIONS INFORMATION

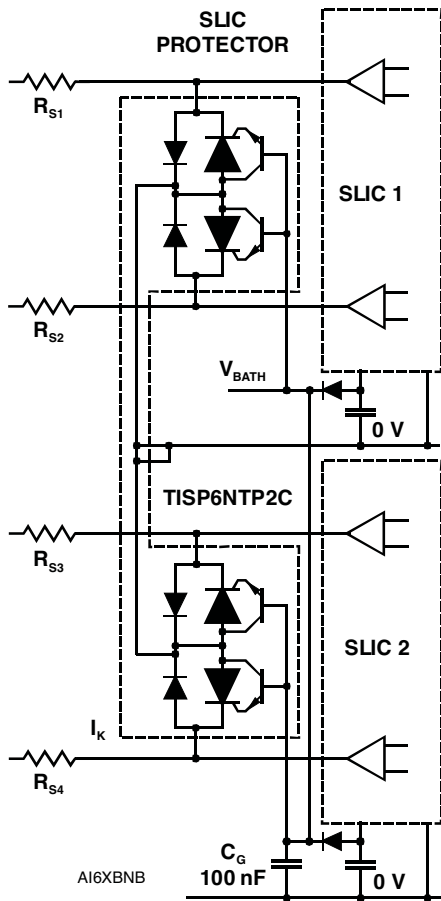
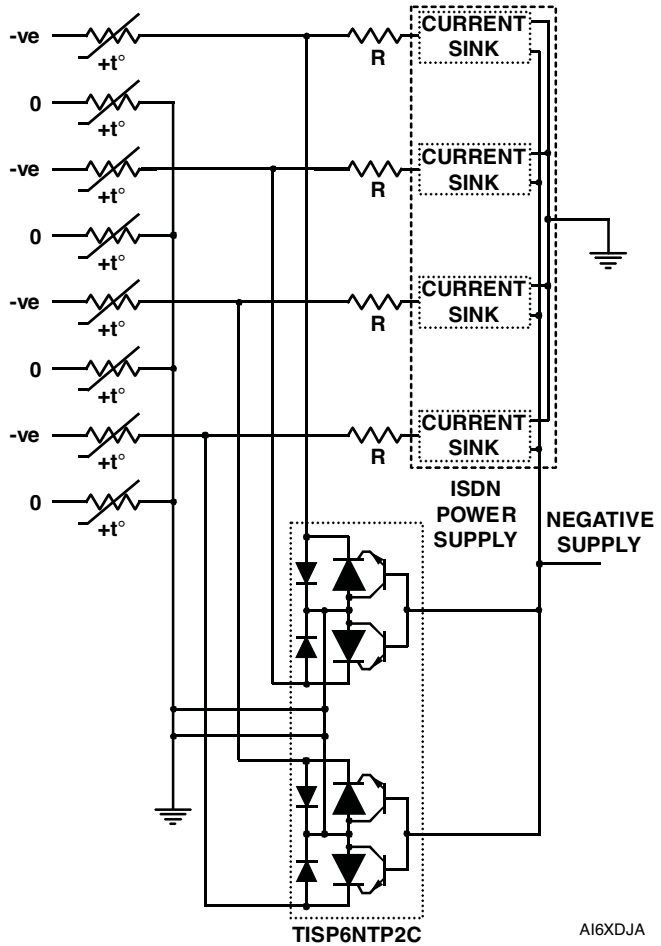


Figure 2. SLIC Protection



Resistor "R" may be needed if sink has internal clamp diode

Figure 3. Protection of Four ISDN Power Feeds

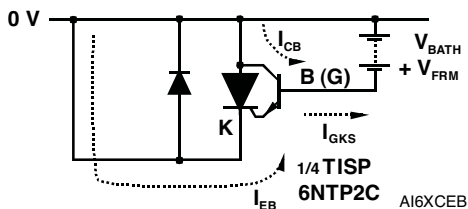


Figure 4. Transistor CB and EB Verification

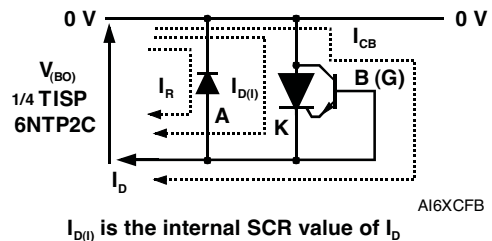


Figure 5. Off-State Current Verification

TISP6NTP2C High Voltage Ringing SLIC Protector

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MECHANICAL DATA

Device Symbolization Code

Devices will be coded as below.

| Device | Symbolization Code |
|----------------|--------------------|
| TISP6NTP2CDR-S | 6NTP2C |

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