

## Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[NXP Semiconductors/Freescale Semiconductor, Inc.](#)  
[74ALVCH16600DGG,11](#)

For any questions, you can email us directly:

[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)

# DATA SHEET

**74ALVCH16600**

**18-bit universal bus transceiver (3-State)**

Product specification  
Supersedes data of 1998 Aug  
IC24 Data Handbook

1998 Sep 24

# 18-bit universal bus transceiver (3-State)

# 74ALVCH16600

## FEATURES

- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive  $\pm 24$  mA at 3.0 V
- All inputs have bus hold circuitry
- Output drive capability 50 $\Omega$  transmission lines @ 85°C
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple  $V_{CC}$  and ground pins for minimum noise and ground bounce

## DESCRIPTION

The 74ALVCH16600 is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ( $\overline{OE}_{AB}$  and  $\overline{OE}_{BA}$ ), latch enable ( $LE_{AB}$  and  $LE_{BA}$ ), and clock ( $\overline{CP}_{AB}$  and  $\overline{CP}_{BA}$ ) inputs. For A-to-B data flow, the device operates in the transparent mode when  $LE_{AB}$  is High. When  $LE_{AB}$  is Low, the A data is latched if  $\overline{CP}_{AB}$  is held at a High or Low logic level. If  $LE_{AB}$  is Low, the A-bus data is stored in the latch/flip-flop on the High-to-Low transition of  $\overline{CP}_{AB}$ . When  $\overline{OE}_{AB}$  is Low, the outputs are active. When  $\overline{OE}_{AB}$  is High, the outputs are in the high-impedance state. The High clock can be controlled with the clock-enable inputs ( $\overline{CE}_{BA}/\overline{CE}_{AB}$ ).

Data flow for B-to-A is similar to that of A-to-B but uses  $\overline{OE}_{BA}$ ,  $LE_{BA}$  and  $\overline{CP}_{BA}$ .

To ensure the high impedance state during power up or power down,  $\overline{OE}_{BA}$  and  $\overline{OE}_{AB}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

## QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f = 2.5\text{ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT	
$t_{PHL}/t_{PLH}$	Propagation delay An, Bn to Bn, An	$V_{CC} = 2.5\text{V}, C_L = 30\text{pF}$ $V_{CC} = 3.3\text{V}, C_L = 50\text{pF}$	3.1 2.8	ns	
$C_{I/O}$	Input/Output capacitance		8.0	pF	
$C_I$	Input capacitance		4.0	pF	
$C_{PD}$	Power dissipation capacitance per latch	$V_I = \text{GND to } V_{CC}^1$	Outputs enabled	21	pF
			Outputs disabled	3	

### NOTES:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

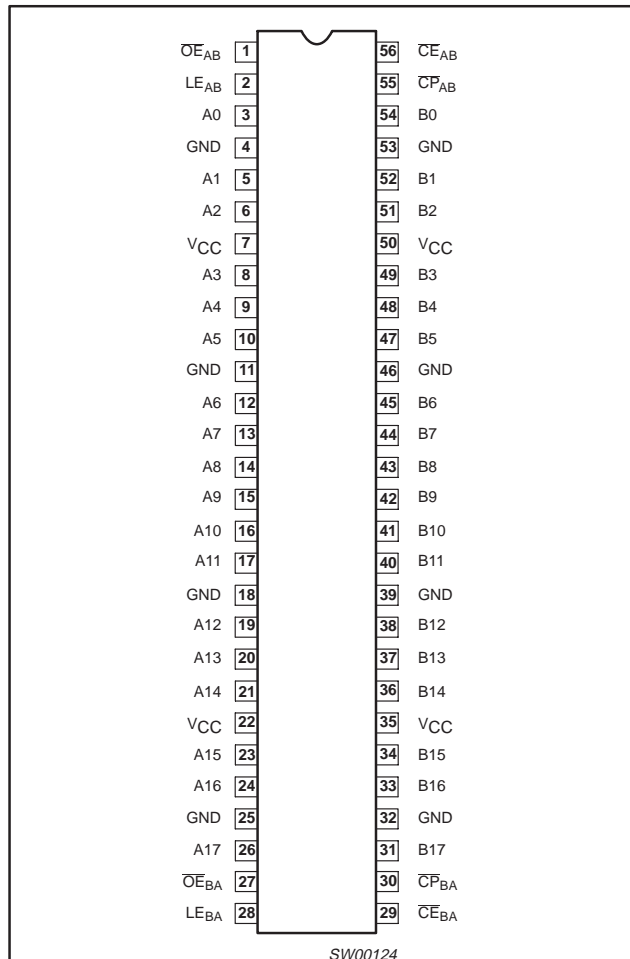
## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74ALVCH16600 DGG	SOT364-1

18-bit universal bus transceiver (3-State)

74ALVCH16600

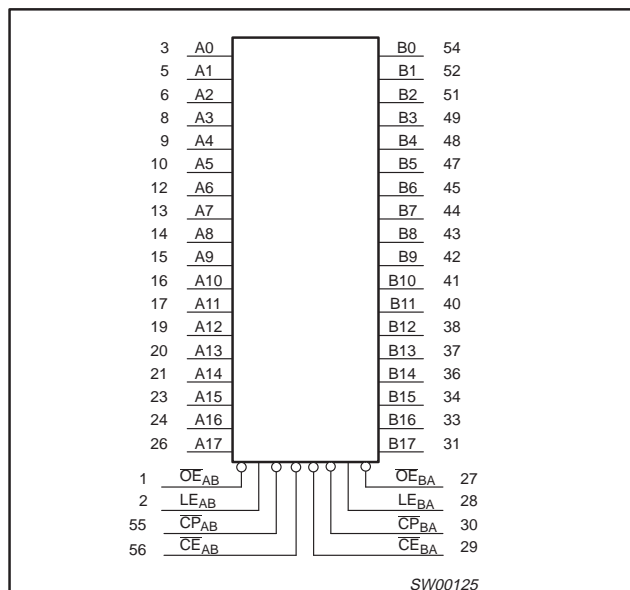
**PIN CONFIGURATION**



**PIN DESCRIPTION**

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_{AB}$	Output enable A-to-B
2	$LE_{AB}$	Latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0 to A17	Data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	$V_{CC}$	Positive supply voltage
27	$\overline{OE}_{BA}$	Output enable B-to-A
28	$LE_{BA}$	Latch enable B-to-A
29	$\overline{CE}_{BA}$	Clock enable B-to-A
30	$\overline{CP}_{BA}$	Clock input B-to-A
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0 to B17	Data inputs/outputs
55	$\overline{CP}_{AB}$	Clock input A-to-B
56	$\overline{CE}_{AB}$	Clock enable A-to-B

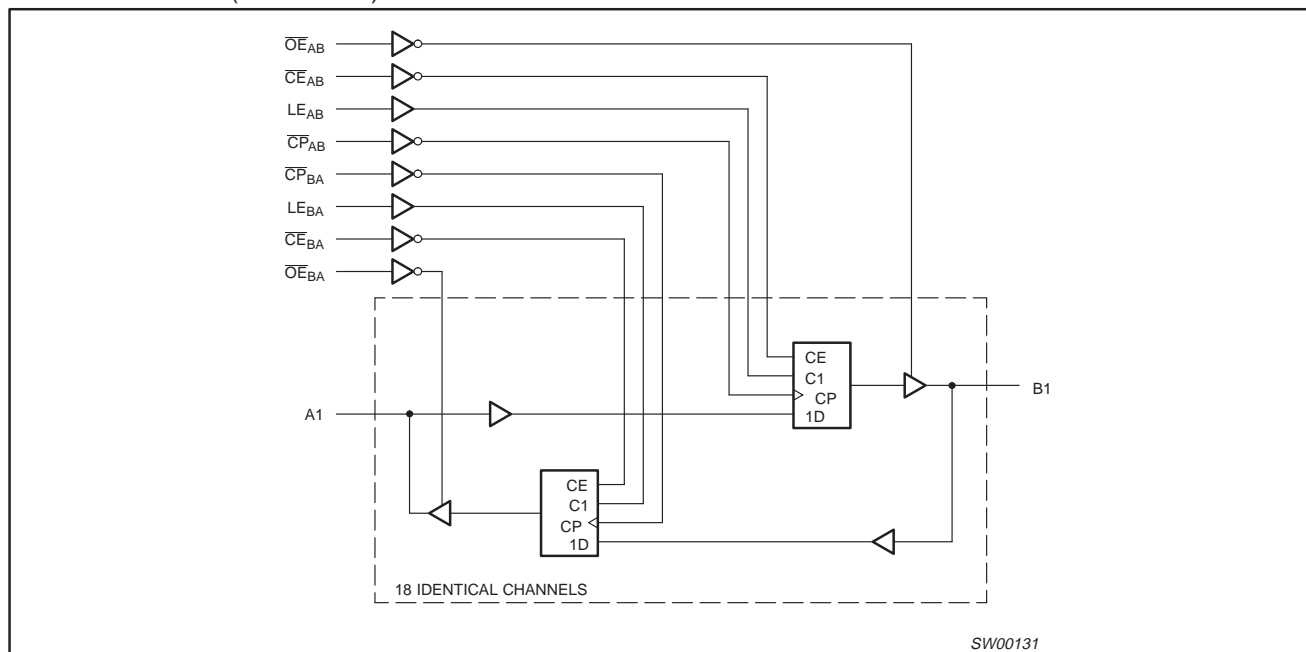
**LOGIC SYMBOL**



18-bit universal bus transceiver (3-State)

74ALVCH16600

LOGIC DIAGRAM (one section)



FUNCTION TABLE

INPUTS					OUTPUTS	STATUS
$\overline{CE}_{XX}$	$\overline{OE}_{XX}$	$LE_{XX}$	$\overline{CP}_{XX}$	DATA		
X	H	X	X	X	Z	Disabled
X	L	H	X	H	H	Transparent
X	L	H	X	L	L	
H	L	L	X	X	NC	Hold
L	L	L	↓	h	H	Clock + display
L	L	L	↓	l	L	
L	L	L	H	X	NC	Hold
L	L	L	L	X		

XX = AB for A-to-B direction, BA for B-to-A direction

H = HIGH voltage level

L = LOW voltage level

h = HIGH state must be present one setup time before the LOW-to-HIGH transition of  $\overline{CP}_{XX}$

l = LOW state must be present one setup time before the LOW-to-HIGH transition of  $\overline{CP}_{XX}$

X = Don't care

↓ = HIGH-to-LOW level transition

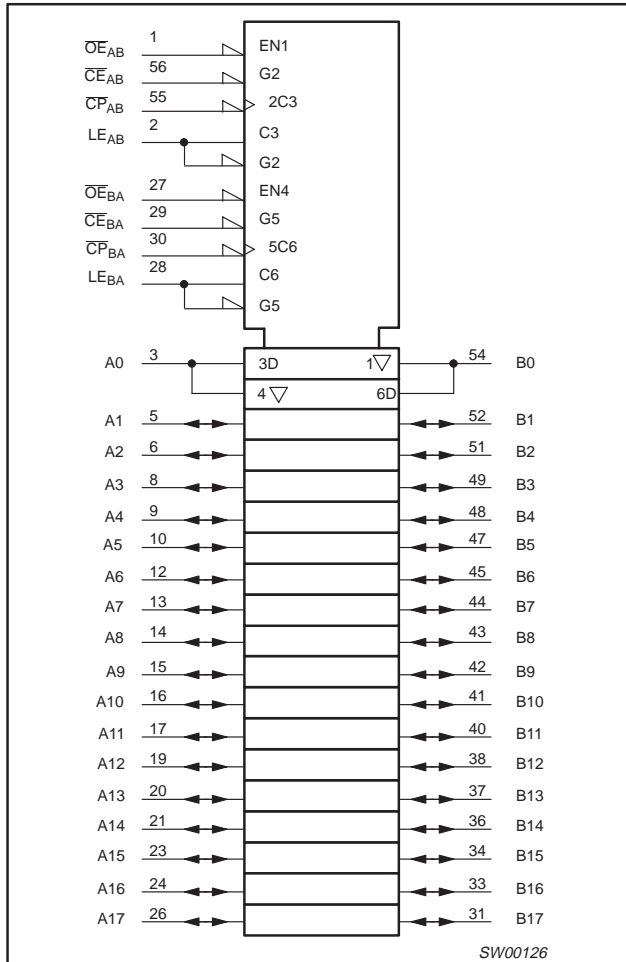
NC = No change

Z = High impedance "off" state

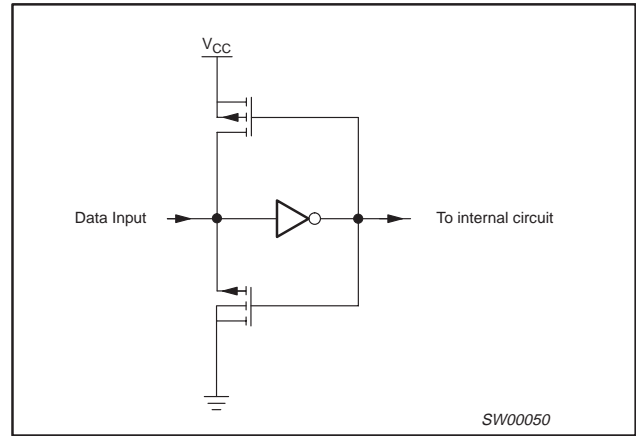
18-bit universal bus transceiver (3-State)

74ALVCH16600

LOGIC SYMBOL (IEEE/IEC)



BUSHOLD CIRCUIT



# 18-bit universal bus transceiver (3-State)

# 74ALVCH16600

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V <sub>CC</sub>	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V <sub>I</sub>	DC Input voltage range		0	V <sub>CC</sub>	V
V <sub>O</sub>	DC output voltage range		0	V <sub>CC</sub>	V
T <sub>amb</sub>	Operating free-air temperature range		-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	Input rise and fall times	V <sub>CC</sub> = 2.3 to 3.0V V <sub>CC</sub> = 3.0 to 3.6V	0 0	20 10	ns/V

## ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
V <sub>I</sub>	DC input voltage	For control pins <sup>1</sup>	-0.5 to +4.6	V
		For data inputs <sup>1</sup>	-0.5 to V <sub>CC</sub> +0.5	
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	± 50	mA
V <sub>O</sub>	DC output voltage	Note 1	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>O</sub>	DC output source or sink current	V <sub>O</sub> = 0 to V <sub>CC</sub>	± 50	mA
I <sub>GND</sub> , I <sub>CC</sub>	DC V <sub>CC</sub> or GND current		± 100	mA
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C
P <sub>TOT</sub>	Power dissipation per package -plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C above +55°C derate linearly with 8 mW/K	600	mW

### NOTE:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 18-bit universal bus transceiver (3-State)

## 74ALVCH16600

**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 2.3 to 2.7V	1.7	1.2		V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0	1.5		
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 2.3 to 2.7V		1.2	0.7	V
		V <sub>CC</sub> = 2.7 to 3.6V		1.5	0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -6mA	V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.08		
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.26		
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.14		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.09		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 1.0	V <sub>CC</sub> - 0.28		
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA		GND	0.20	V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA		0.07	0.40	V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.15	0.70	V
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.14	0.40	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA		0.27	0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND		0.1	5	μA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 2.7 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND		0.1	10	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.2	40	μA
ΔI <sub>CC</sub>	Additional quiescent supply current	V <sub>CC</sub> = 2.3V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		150	750	μA
I <sub>BHL</sub>	Bus hold LOW sustaining current	V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 0.7V <sup>2</sup>	45	-		μA
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 0.8V <sup>2</sup>	75	150		
I <sub>BHH</sub>	Bus hold HIGH sustaining current	V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 1.7V <sup>2</sup>	-45			μA
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 2.0V <sup>2</sup>	-75	-175		
I <sub>BHLO</sub>	Bus hold LOW overdrive current	V <sub>CC</sub> = 3.6V <sup>2</sup>	500			μA
I <sub>BHHO</sub>	Bus hold HIGH overdrive current	V <sub>CC</sub> = 3.6V <sup>2</sup>	-500			μA

**NOTES:**

1. All typical values are at T<sub>amb</sub> = 25°C.
2. Valid for data inputs of bus hold parts.



18-bit universal bus transceiver (3-State)

74ALVCH16600

**AC CHARACTERISTICS FOR  $V_{CC} = 2.3V$  TO  $2.7V$  RANGE**

GND = 0V;  $t_r = t_f \leq 2.0ns$ ;  $C_L = 30pF$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 2.5V \pm 0.2V$			
			MIN	TYP <sup>1</sup>	MAX	
$t_{PHL}/t_{PLH}$	Propagation delay An, Bn to Bn, An	1, 2	1.0	3.1	5.2	ns
	Propagation delay LE <sub>AB</sub> , LE <sub>BA</sub> to Bn, An		1.0	3.6	6.2	
	Propagation delay $\overline{CP}_{AB}$ , $\overline{CP}_{BA}$ to Bn, An		1.0	3.8	7.3	
$t_{PZH}/t_{PZL}$	3-State output enable time OE <sub>BA</sub> , OE <sub>AB</sub> to An, Bn	3	1.0	3.1	6.5	ns
$t_{PHZ}/t_{PLZ}$	3-State output enable time OE <sub>BA</sub> , OE <sub>AB</sub> to An, Bn	3	1.0	2.8	5.1	ns
$t_w$	Pulse width HIGH LE <sub>AB</sub> , LE <sub>BA</sub>	2	3.3	1.6	–	ns
	Pulse width HIGH or LOW $\overline{CP}_{AB}$ , $\overline{CP}_{BA}$		3.3	2.0	–	
$t_{SU}$	Set-up time An, Bn to $\overline{CP}_{AB}$ , $\overline{CP}_{BA}$	4	1.3	–0.1	–	ns
	Set-up time An, Bn to LE <sub>AB</sub> , LE <sub>BA</sub>	4	1.2	0.1	–	
	Set-up time CE <sub>AB</sub> , CE <sub>BA</sub> to $\overline{CP}_{AB}$ , $\overline{CP}_{BA}$	4	0.7	–0.4	–	
$t_h$	Hold time An, Bn to $\overline{CP}_{AB}$ , $\overline{CP}_{BA}$	4	1.5	0.6	–	ns
	Hold time An, Bn to LE <sub>AB</sub> , LE <sub>BA</sub>		1.2	0.6	–	
	Hold time CE <sub>AB</sub> , CE <sub>BA</sub> to $\overline{CP}_{AB}$ , $\overline{CP}_{BA}$	4	1.4	2.0	–	
$f_{MAX}$	Maximum clock frequency		150	335	–	MHz

**NOTE:**

1. All typical values are at  $V_{CC} = 2.5V$  and  $T_{amb} = 25^\circ C$ .

18-bit universal bus transceiver (3-State)

74ALVCH16600

**AC CHARACTERISTICS FOR  $V_{CC} = 3.0V$  TO  $3.6V$  RANGE AND  $V_{CC} = 2.7V$**

GND = 0V;  $t_r = t_f = 2.5ns$ ;  $C_L = 50pF$

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$			
			MIN	TYP <sup>1</sup>	MAX	MIN	TYP	MAX	
$t_{PHL}/t_{PLH}$	Propagation delay An, Bn to Bn, An	1, 2	1.0	2.8	4.2		3.1	4.7	ns
	Propagation delay $LE_{AB}, LE_{BA}$ to Bn, An		1.0	3.1	4.9		3.4	5.5	
	Propagation delay $\overline{CP}_{AB}, \overline{CP}_{BA}$ to Bn, An		1.3	2.9	5.7		3.8	6.8	
$t_{PZH}/t_{PZL}$	3-State output enable time $\overline{OE}_{BA}$ to An	3	1.1	2.8	5.2		3.3	6.3	ns
$t_{PHZ}/t_{PLZ}$	3-State output disable time $\overline{OE}_{BA}$ to An	3	1.2	3.2	4.4		3.3	4.7	ns
$t_W$	LE pulse width $LE_{AB}, LE_{BA}$ to $\overline{CP}_{AB}, \overline{CP}_{BA}$	2	3.3	1.0		3.3	1.0		ns
	LE pulse width HIGH or LOW $\overline{CP}_{AB}, \overline{CP}_{BA}$		3.3	1.1		3.3	1.4		
$t_{SU}$	Set-up time An, Bn to $\overline{CP}_{AB}, \overline{CP}_{BA}$	4	1.2	-0.1		1.3	-0.4		ns
	Set-up time An, Bn to $LE_{AB}, LE_{BA}$	4	1.1	0.3		1.1	-0.2		
	Set-up time $CE_{AB}, CE_{BA}$ to $\overline{CP}_{AB}, \overline{CP}_{BA}$	4	0.8	-0.2		0.7	-0.7		
$t_H$	Hold time An, Bn to $\overline{CP}_{AB}, \overline{CP}_{BA}$	4	1.5	0.4		1.8	0.4		ns
	Hold time An, Bn to $LE_{AB}, LE_{BA}$		1.3	0.1		1.6	0.1		
	Hold time $CE_{AB}, CE_{BA}$ to $\overline{CP}_{AB}, \overline{CP}_{BA}$	4	1.4	0.4		1.7	0.6		
$f_{MAX}$	Maximum clock frequency		150	362		150	350		MHz

**NOTE:**

1. All typical values are at  $V_{CC} = 3.3V$  and  $T_{amb} = 25^\circ C$ .

18-bit universal bus transceiver (3-State)

74ALVCH16600

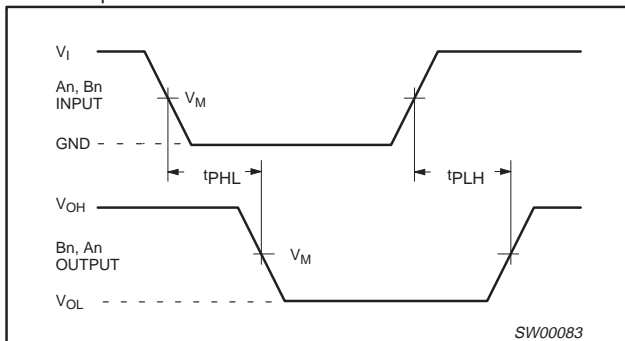
**AC WAVEFORMS**

**V<sub>CC</sub> = 2.3 TO 2.7 V RANGE**

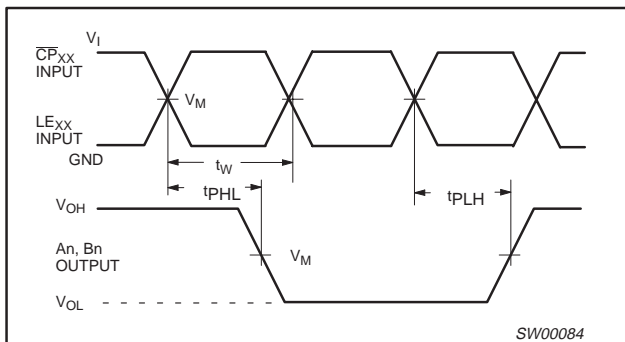
1. V<sub>M</sub> = 0.5 V
2. V<sub>X</sub> = V<sub>OL</sub> + 0.15V
3. V<sub>Y</sub> = V<sub>OH</sub> - 0.15V
4. V<sub>I</sub> = V<sub>CC</sub>
5. V<sub>OL</sub> and V<sub>OH</sub> are the typical output voltage drop that occur with the output load.

**V<sub>CC</sub> = 3.0 TO 3.6 V RANGE AND V<sub>CC</sub> = 2.7 V**

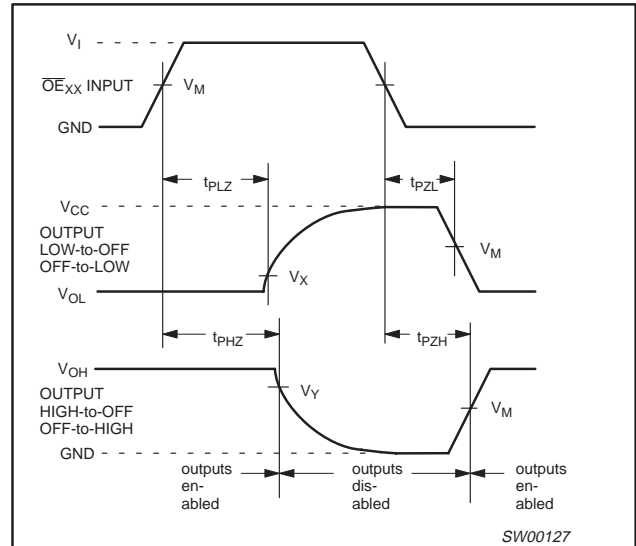
1. V<sub>M</sub> = 1.5 V
2. V<sub>X</sub> = V<sub>OL</sub> + 0.3V
3. V<sub>Y</sub> = V<sub>OH</sub> - 0.3V
4. V<sub>I</sub> = 2.7 V
5. V<sub>OL</sub> and V<sub>OH</sub> are the typical output voltage drop that occur with the output load.



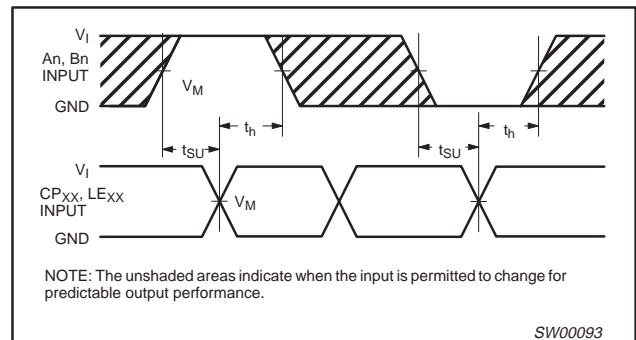
Waveform 1. Input (An, Bn) to output (Bn, An) propagation delay times



Waveform 2. Latch enable input (LE<sub>AB</sub>, LE<sub>BA</sub>) and clock pulse input (CP<sub>AB</sub>, CP<sub>BA</sub>) to output (An, Bn) propagation delays and latch enable pulse width



Waveform 3. 3-State enable and disable times

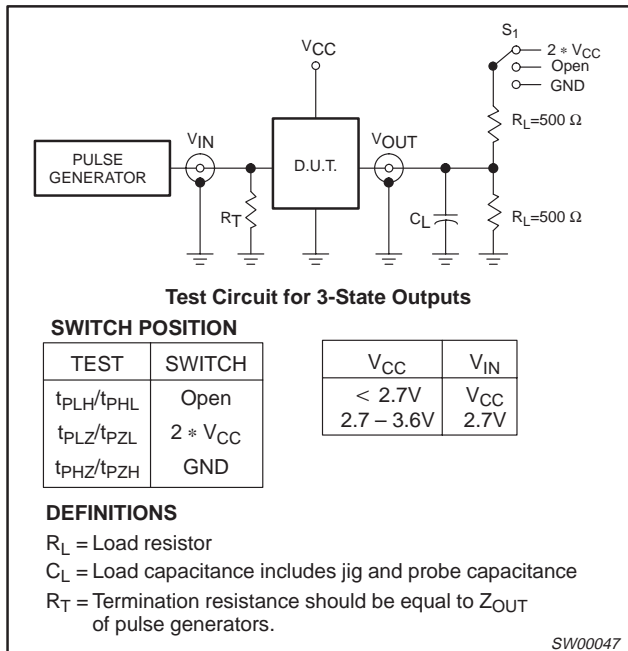


Waveform 4. Data set-up and hold times for the An and Bn inputs to the LE<sub>AB</sub>, LE<sub>BA</sub>, CP<sub>AB</sub> and CP<sub>BA</sub> inputs

18-bit universal bus transceiver (3-State)

74ALVCH16600

TEST CIRCUIT



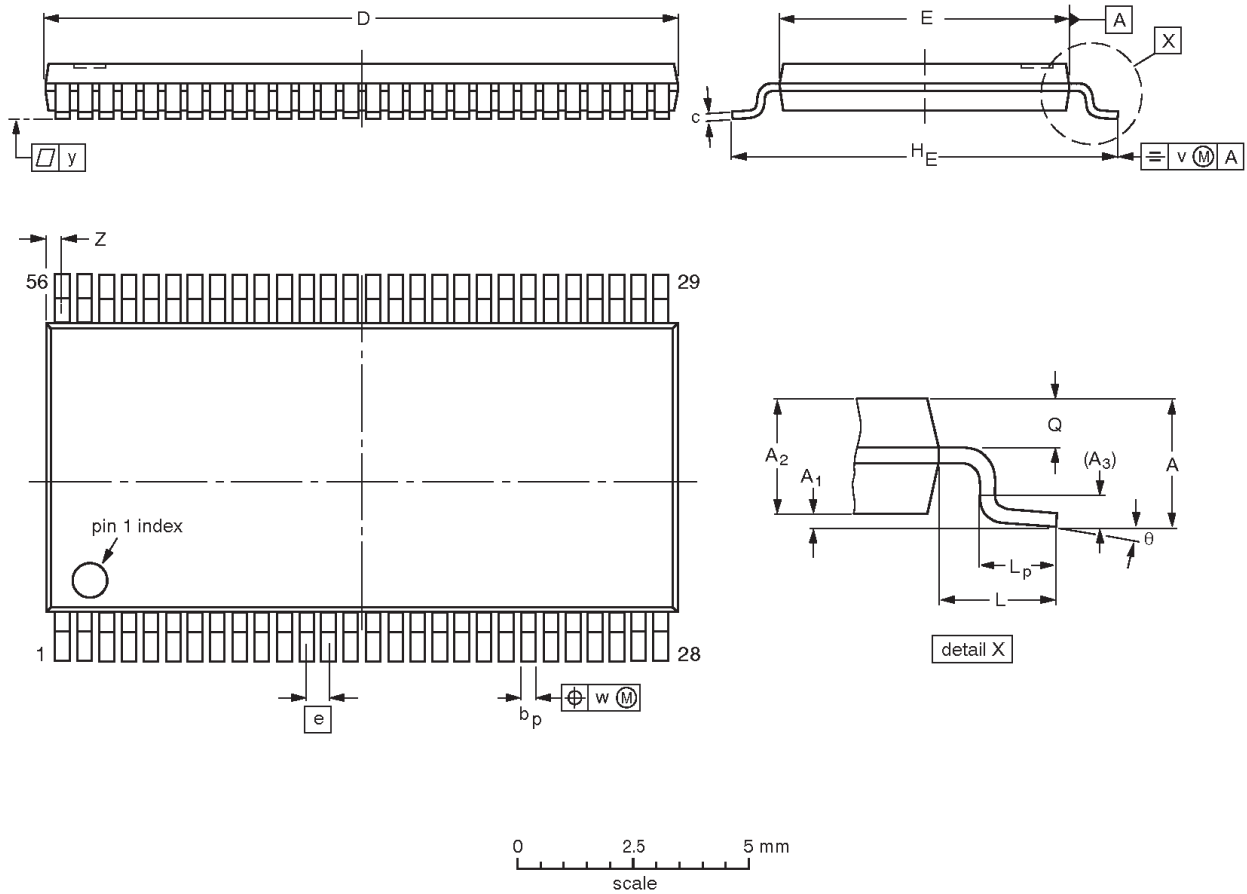
Load circuitry for switching times

18-bit universal bus transceiver (3-State)

74ALVCH16600

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153EE				93-02-03 95-02-10

---

18-bit universal bus transceiver (3-State)

74ALVCH16600

---

**NOTES**

18-bit universal bus transceiver (3-State)

74ALVCH16600

**DEFINITIONS**

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	<b>Full Production</b>	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Philips Semiconductors and Philips Electronics North America Corporation reserve the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**LIFE SUPPORT APPLICATIONS**

Philips Semiconductors and Philips Electronics North America Corporation Products are not designed for use in life support appliances, devices, or systems where malfunction of a Philips Semiconductors and Philips Electronics North America Corporation Product can reasonably be expected to result in a personal injury. Philips Semiconductors and Philips Electronics North America Corporation customers using or selling Philips Semiconductors and Philips Electronics North America Corporation Products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors and Philips Electronics North America Corporation for any damages resulting from such improper use or sale.

**Philips Semiconductors**  
**811 East Arques Avenue**  
**P.O. Box 3409**  
**Sunnyvale, California 94088-3409**  
**Telephone 800-234-7381**

© Copyright Philips Electronics North America Corporation 1998  
 All rights reserved. Printed in U.S.A.

Date of release: 06-98

Document order number:

9397-750-04799

*Let's make things better.*

