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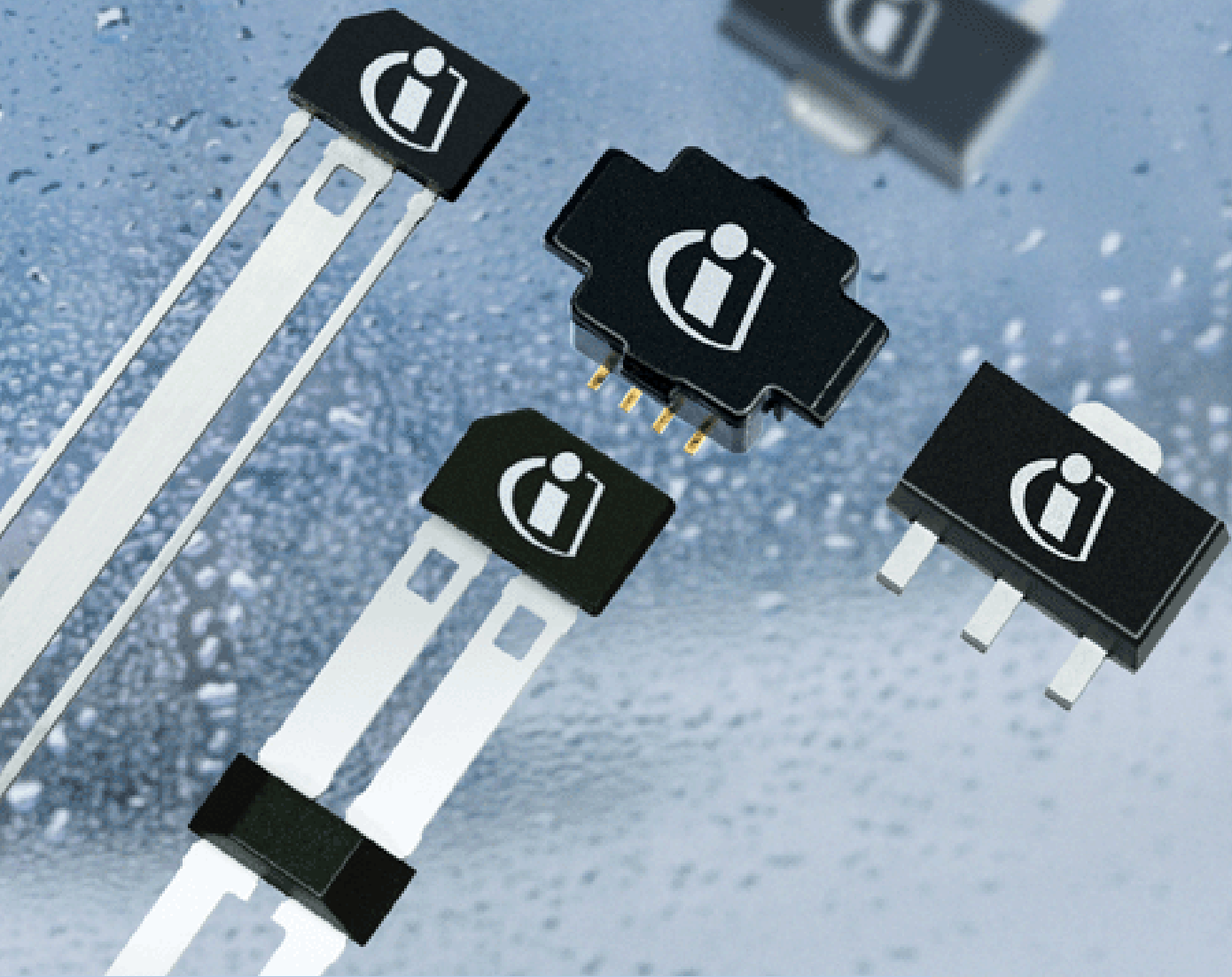
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Data Sheet, V 2.0, February 2009

# TLE4966L

High Precision Hall-Effect Switch with  
Direction Detection



Sensors

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## TLE4966L

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V 2.0

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Previous Version:            V 1.2

Page	Subjects (major changes since last revision)
	TLE4966H removed

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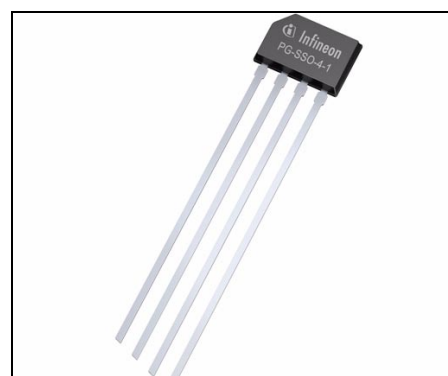
## High Precision Hall-Effect Switch with Direction Detection

**TLE4966L**

### 1 Overview

#### 1.1 Features

- 2.7 V to 24 V supply voltage operation
- Operation from unregulated power supply
- High sensitivity and high stability of the magnetic switching points
- High resistance to mechanical stress by Active Error Compensation
- Reverse battery protection (-18 V)
- Superior temperature stability
- Peak temperatures up to 195°C without damage
- Low jitter (typ. 1  $\mu$ s)
- Digital output signals
- Bipolar version
- Excellent matching between the 2 Hall probes
- Hall plate distance 1.45 mm
- Direction & speed information
- Direction signal switches before the speed signal

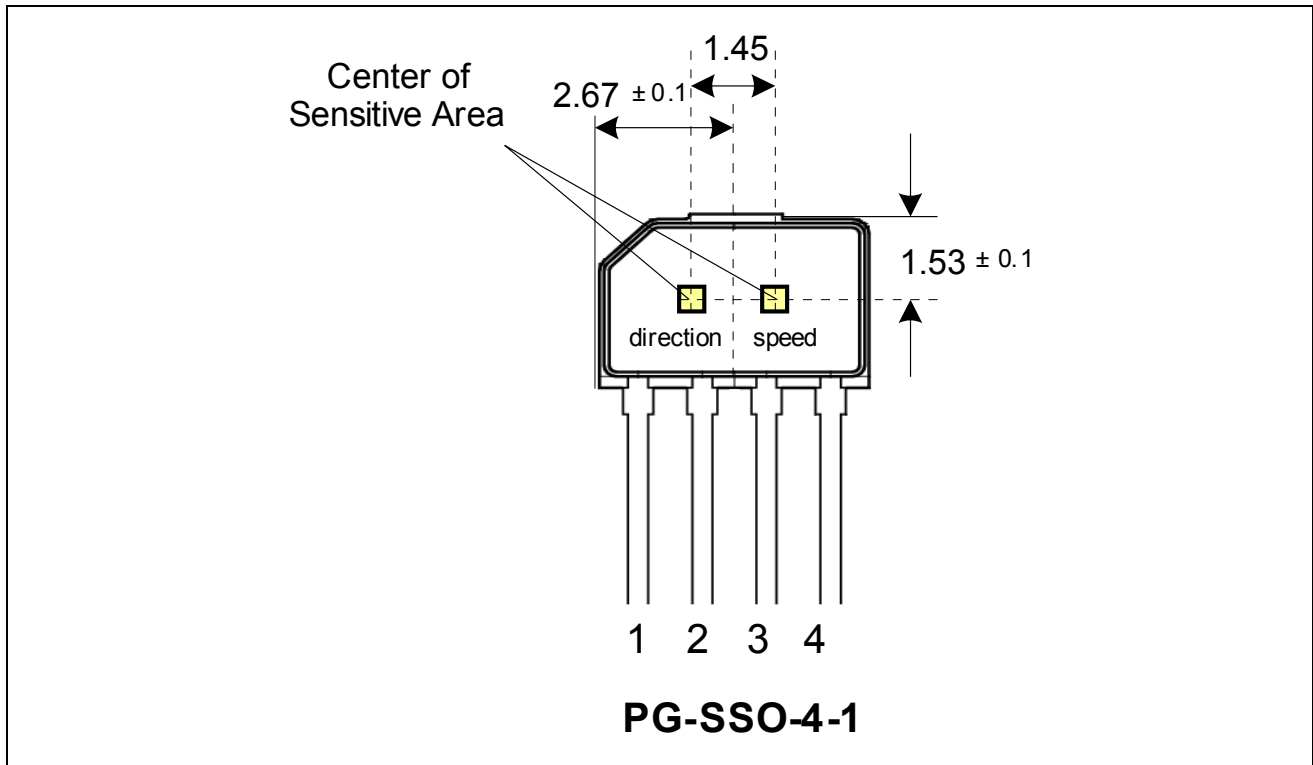


#### 1.2 Functional Description

The TLE4966L is an integrated circuit double Hall-effect sensor designed specifically for highly accurate applications. Precise magnetic switching points and high temperature stability are achieved by active compensation circuits and chopper techniques on chip. The IC provides a speed signal at Q2 for every magnetic pole pair and a direction information at Q1, which is provided before the speed signal.

Type	Package
TLE4966L	PG-SSO-4-1

**1.3 Pin Configuration (top view)**



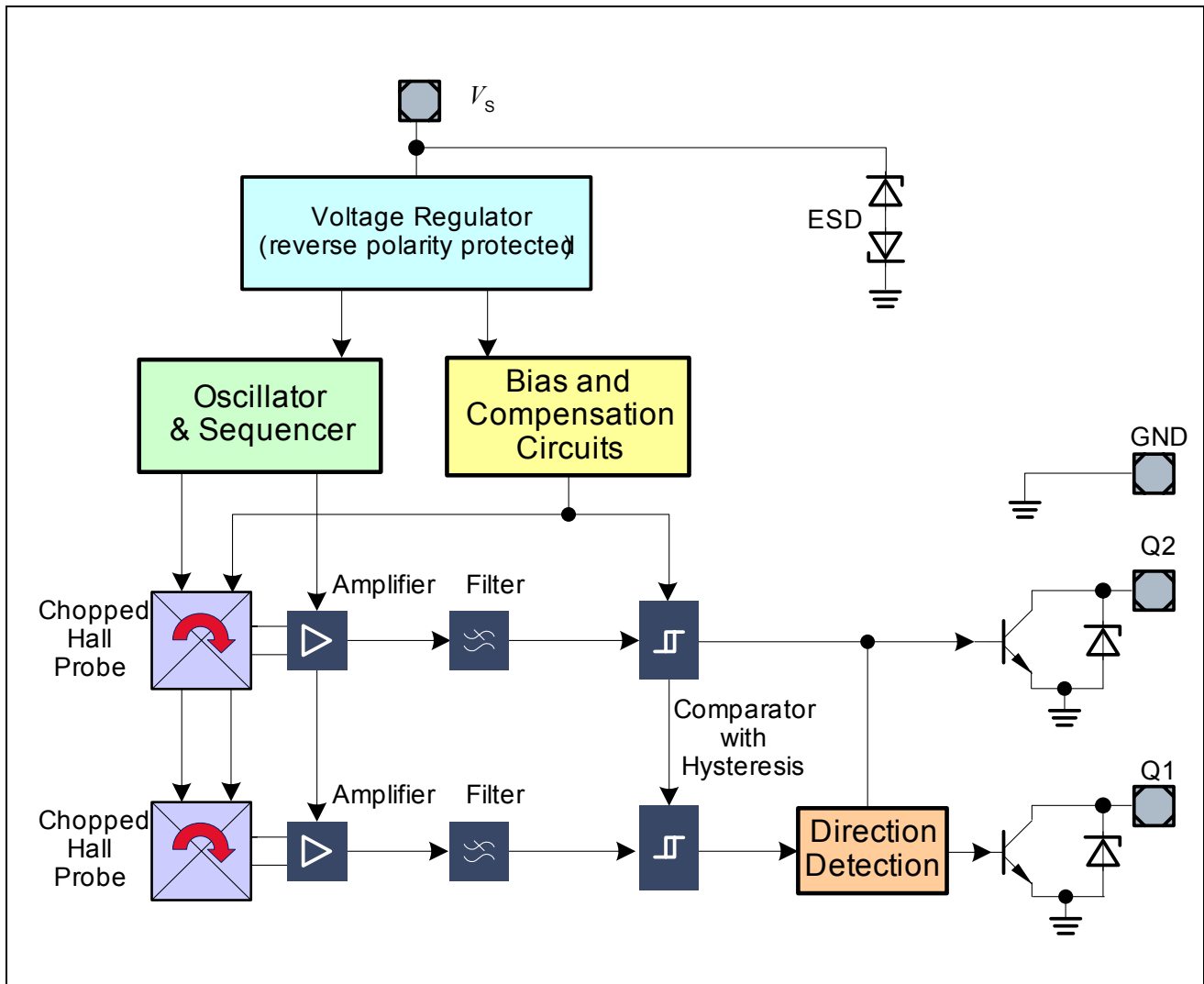
**Figure 1 Pin Definition and Center of Sensitive Area**

**Table 1 Pin Definitions and Functions**

Pin No.	Symbol	Function
1	$V_S$	Supply voltage
2	Q1	Direction
3	Q2	Speed
4	GND	Ground

## 2 General

### 2.1 Block Diagram



**Figure 2 Block Diagram**

### 2.2 Circuit Description

The chopped Double Hall Switch comprises two Hall probes, bias generator, compensation circuits, oscillator, and output transistors.

The bias generator provides currents for the Hall probes and the active circuits. Compensation circuits stabilize the temperature behavior and reduce technology variations.

The Active Error Compensation rejects offsets in signal stages and the influence of mechanical stress to the Hall probes caused by molding and soldering processes and other thermal stresses in the package. This chopper technique together with the threshold generator and the comparator ensures high accurate magnetic switching points.



Maximum Ratings

### 3 Maximum Ratings

**Table 2 Absolute Maximum Ratings**  
 $T_j = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$

Parameter	Symbol	Limit Values		Unit	Conditions
		min.	max.		
Supply voltage	$V_S$	-18	18	V	for 1 h, $R_S \geq 200 \Omega$ for 5 min, $R_S \geq 200 \Omega$
		-18	24		
		-18	26		
Supply current through protection device	$I_S$	-50	50	mA	
Output voltage	$V_Q$	-0.7 -0.7	18 26	V	for 5 min @ 1.2 k $\Omega$ pull up
Continuous output current	$I_Q$	-50	50	mA	
Junction temperature	$T_j$	–	155	$^{\circ}\text{C}$	for 2000 h (not additive) for 1000 h (not additive) for 168 h (not additive) for 3 x 1 h (additive)
		–	165		
		–	175		
		–	195		
Storage temperature	$T_S$	-40	150	$^{\circ}\text{C}$	
Magnetic flux density	$B$	–	unlimited	mT	

*Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**Table 3 ESD Protection <sup>1)</sup>**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
ESD voltage	$V_{\text{ESD}}$	–	$\pm 4$	kV	HBM, $R = 1.5 \text{ k}\Omega$ , $C = 100 \text{ pF}$ $T_A = 25^{\circ}\text{C}$

1) Human Body Model (HBM) tests according to: EOS/ESD Association Standard S5.1-1993 and Mil. Std. 883D method 3015.7

## 4 Operating Range

Table 4 Operating Range

Parameter	Symbol	Limit Values			Unit	Conditions
		min.	typ.	max.		
Supply voltage	$V_S$	2.7	–	18	V	1 h with $R_S \geq 200 \Omega$ for 5 min $R_S \geq 200 \Omega$
		–	–	24		
		–	–	26		
Output voltage	$V_Q$	-0.7	–	18	V	
Junction temperature	$T_j$	-40	–	150	°C	for 168 h
		–	–	175		
Output current	$I_Q$	0	–	10	mA	

Electrical and Magnetic Parameters

## 5 Electrical and Magnetic Parameters

Table 5 Electrical Characteristics <sup>1)</sup>

Parameter	Symbol	Limit Values			Unit	Conditions
		min.	typ.	max.		
Supply current	$I_S$	4	5.2	7	mA	$V_S = 2.7 \text{ V} \dots 18 \text{ V}$
Reverse current	$I_{SR}$	0	0.2	1	mA	$V_S = -18 \text{ V}$
Output saturation voltage	$V_{QSAT}$	–	0.3	0.6	V	$I_Q = 10 \text{ mA}$
Output leakage current	$I_{QLEAK}$	–	0.05	10	$\mu\text{A}$	for $V_Q = 18 \text{ V}$
Output fall time	$t_f$	–	0.2	1	$\mu\text{s}$	$R_L = 1.2 \text{ k}\Omega$ ; $C_L < 50 \text{ pF}$ see: <a href="#">Figure 3 on Page 12</a>
Output rise time	$t_r$	–	0.2	1	$\mu\text{s}$	
Chopper frequency	$f_{OSC}$	–	320	–	kHz	
Switching frequency	$f_{SW}$	0	–	15 <sup>2)</sup>	kHz	
Delay time <sup>3)</sup>	$t_d$	–	13	–	$\mu\text{s}$	
Count Signal Delay	$t_{dc}$	50	200	1000	ns	
Output jitter <sup>4)</sup>	$t_{QJ}$	–	1	–	$\mu\text{s}_{RMS}$	Typ. value for square-wave signal 1 kHz
Repeatability of magnetic thresholds <sup>5)</sup>	$B_{REP}$	–	40	–	$\mu\text{T}_{RMS}$	Typ. value for $\Delta B/\Delta t > 12 \text{ mT/ms}$
Power-on time <sup>6)</sup>	$t_{PON}$	–	13	–	$\mu\text{s}$	$V_S \geq 2.7 \text{ V}$
Distance of hall plates	$d_{HALL}$	–	1.45	–	mm	
Thermal resistance <sup>7)</sup>	$R_{thJA}$	–	–	–190	K/W	PG-SSO-4-1

1) over operating range, unless otherwise specified. Typical values correspond to  $V_S = 12 \text{ V}$  and  $T_A = 25^\circ\text{C}$

2) To operate the sensor at the max. switching frequency, the magnetic signal amplitude must be 1.4 times higher than for static fields. This is due to the -3 dB corner frequency of the low pass filter in the signal path.

3) Systematic delay between magnetic threshold reached and output switching

4) Jitter is the unpredictable deviation of the output switching delay

5)  $B_{REP}$  is equivalent to the noise constant

6) Time from applying  $V_S \geq 2.7 \text{ V}$  to the sensor until the output state is valid

7) Thermal resistance from junction to ambient

Electrical and Magnetic Parameters

Calculation of the ambient temperature:

e.g. for  $V_S = 12.0\text{ V}$ ,  $I_{Styp} = 5.5\text{ mA}$ ,  $V_{QSATtyp} = 0.3\text{ V}$  and  $2 \times I_Q = 10\text{ mA}$  :

Power Dissipation:  $P_{DIS} = 72.0\text{ mW}$ .

In  $T_A = T_j - (R_{thJA} \times P_{DIS}) = 175^\circ\text{C} - (190\text{ K/W} \times 0.072\text{ W})$

Resulting max. ambient temperature:  $T_A = 161.3^\circ\text{C}$

Table 6 Magnetic Characteristics <sup>1)</sup>.

Parameter	Symbol	$T_j$ [°C]	Limit Values			Unit	Conditions
			min.	typ.	max.		
Operate point	$B_{OP}$	-40	5.2	7.7	10.3	mT	
		25	5.0	7.5	10.0		
		150	4.7	7.1	9.5		
Release point	$B_{RP}$	-40	-10.3	-7.7	-5.2	mT	
		25	-10.0	-7.5	-5.0		
		150	-9.5	-7.1	-4.7		
Hysteresis	$B_{HYS}$	-40	–	–	–	mT	
		25	10.0	15.0	20.0		
		150	–	–	–		
Magnetic matching	$B_{MATCH}$	-40	–	–	–	mT	Valid for $B_{OP1} - B_{OP2}$ and $B_{RP1} - B_{RP2}$
		25	-2.0	0	2.0		
		150	–	–	–		
Magnetic offset	$B_{OFF}$	-40	–	–	–	mT	$(B_{OP} + B_{RP})/2$
		25	-2.0	0	2.0		
		150	–	–	–		
Temperature compensation of magnetic thresholds	$TC$	–	–	-350	–	ppm/°C	

1) over operating range, unless otherwise specified. Typical values correspond to  $V_S = 12\text{ V}$

*Note: Typical characteristics specify mean values expected over the production spread.*

Field Direction Definition

Positive magnetic fields related with south pole of magnet to the branded side of package.

Timing Diagrams for the Speed and Direction Outputs

6 Timing Diagrams for the Speed and Direction Outputs

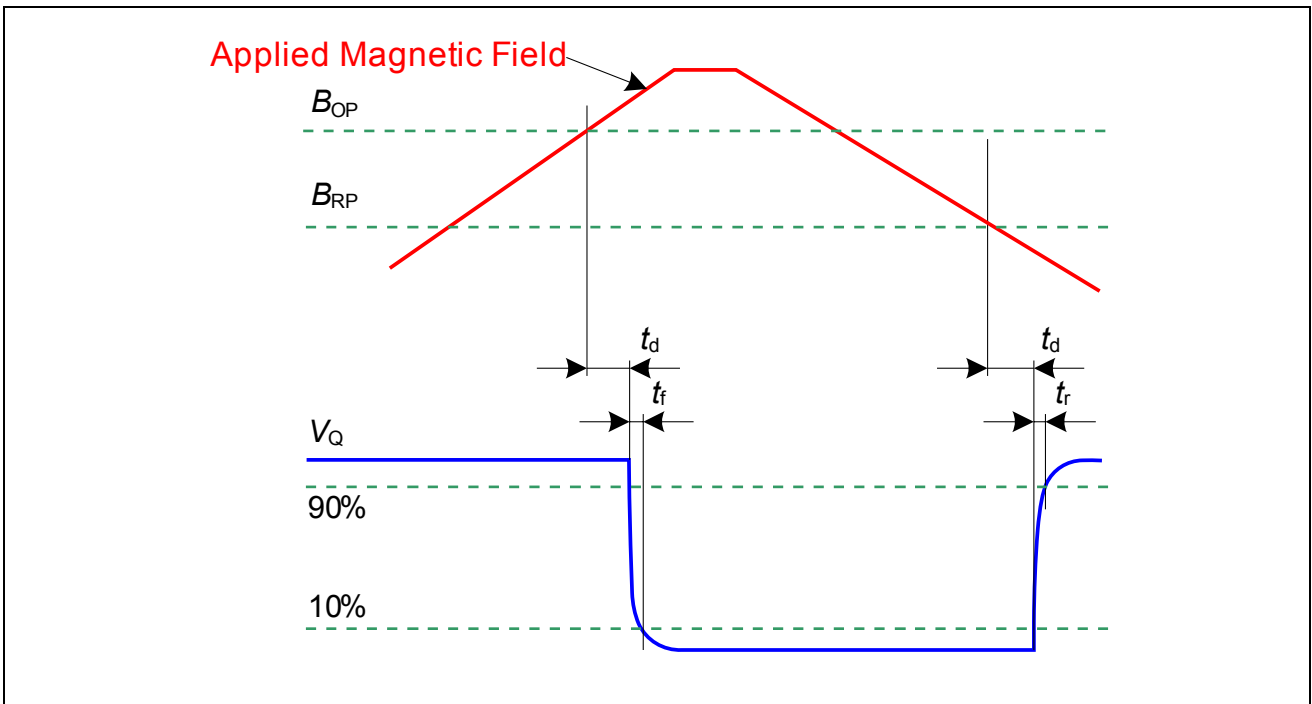


Figure 3 Timing Definition of the Speed Signal

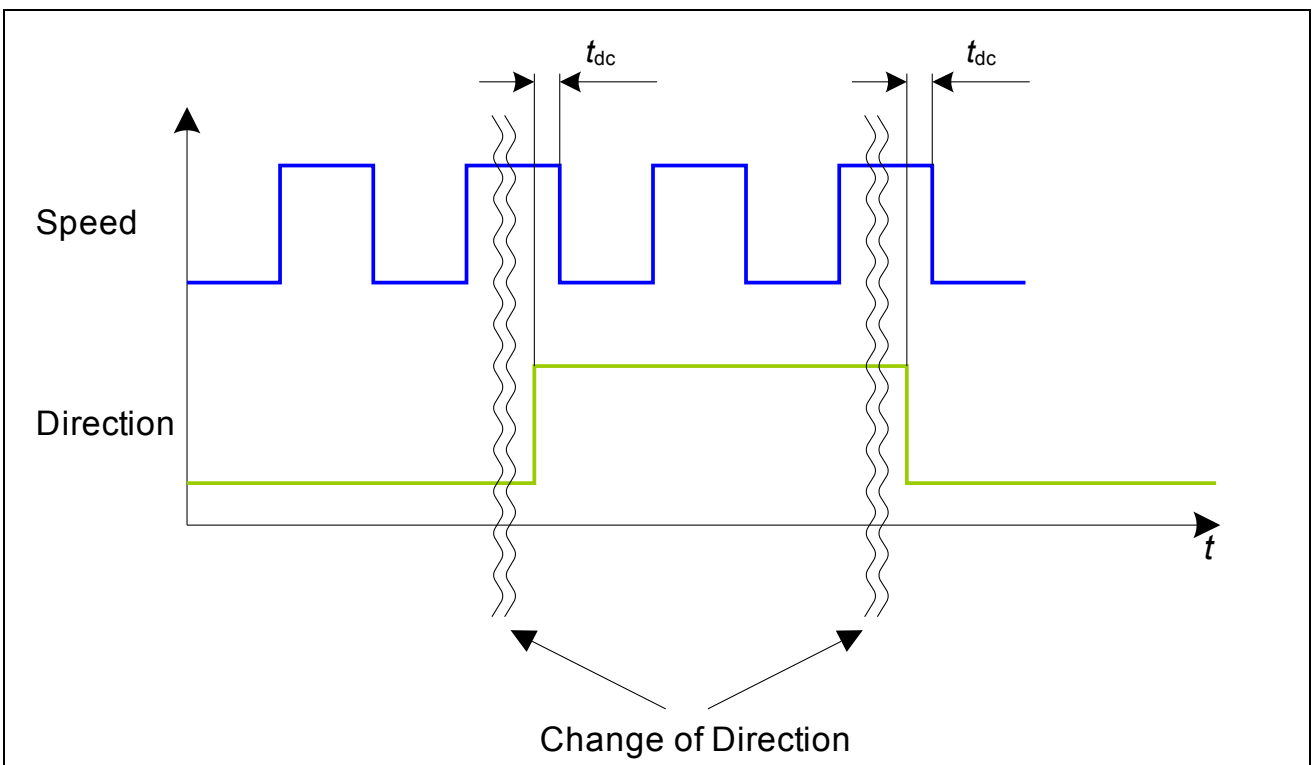
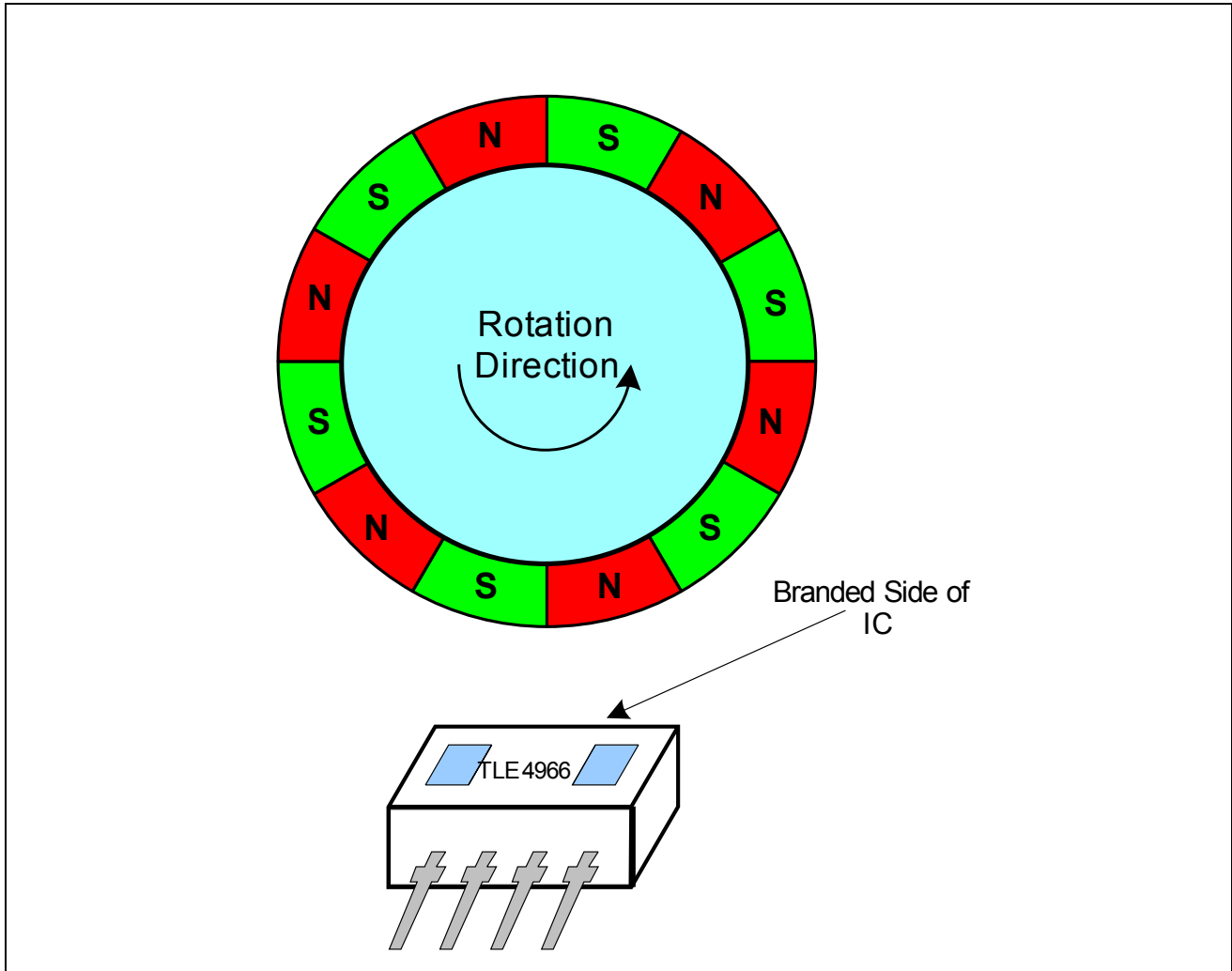


Figure 4 Timing Definition of the Direction Signal

**Timing Diagrams for the Speed and Direction Outputs**



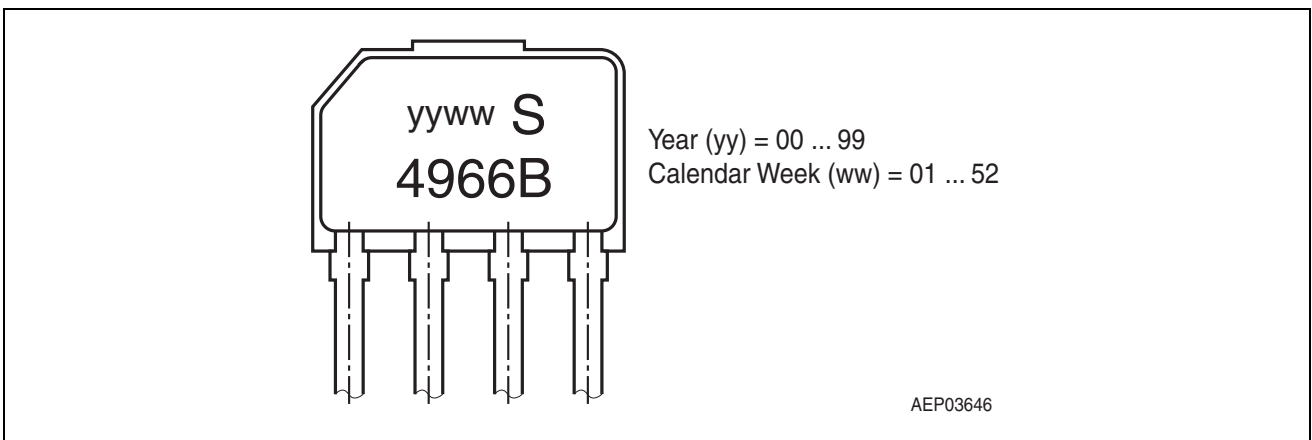
**Figure 5 Definition of the Direction Signal**

Rotation Direction	State of Direction Output $V_{Q1}$
Left to right	Low
Right to left	High

## 7 Package Information

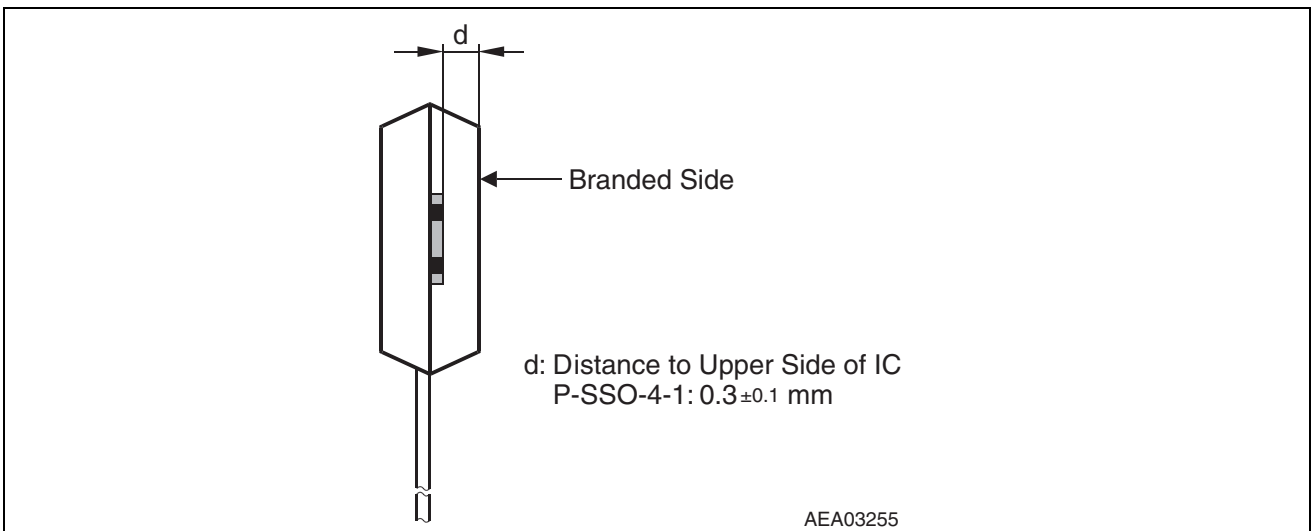
### 7.1 Package Marking

**Figure 6 Marking PG-SSO-4-1**



**Figure 7 Marking**

### 7.2 Distance between Chip and Package Surface



**Figure 8 Distance Chip to Upper Side of IC**

Package Information

7.3 Package Outlines

Figure 9 PG-SSO-4-1

