FAIRCHILD™

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FDD4685
40V P-Channel PowerTrench® MOSFET
–40V, –32A, 27mΩ

Features

- Max $r_{DS(on)}$ = 27mΩ at V_{GS} = –10V, I_D = –8.4A
- Max $r_{DS(on)}$ = 35mΩ at V_{GS} = –4.5V, I_D = –7A
- High performance trench technology for extremely low $r_{DS(on)}$
- RoHS Compliant

General Description

This P-Channel MOSFET has been produced using Fairchild Semiconductor's proprietary PowerTrench® technology to deliver low $r_{DS(on)}$ and good switching characteristic offering superior performance in application.

Application

- Inverter
- Power Supplies

D-PAK (TO-252)
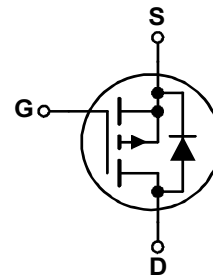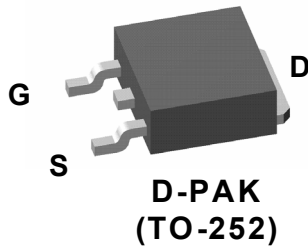
MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		–40	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current -Continuous(Package Limited)	T_C= 25°C	–32	A
	-Continuous(Silicon Limited)	T_C= 25°C (Note 1)	–40	
	-Continuous	T_A= 25°C (Note 1a)	–8.4	
	-Pulsed		–100	
E_{AS}	Drain-Source Avalanche Energy	(Note 3)	121	mJ
P_D	Power Dissipation	T_C= 25°C	69	W
	Power Dissipation	(Note 1a)	3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD4685	FDD4685	D-PAK(TO-252)	13''	16mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = –250μA, V_{GS} = 0V	–40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250μA, referenced to 25°C		–33		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –32V, V_{GS} = 0V			–1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{GS} = 0V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = –250μA	–1	–1.6	–3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = –250μA, referenced to 25°C		4.9		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = –10V, I_D = –8.4A		23	27	mΩ
		V_{GS} = –4.5V, I_D = –7A		30	35	
		V_{GS} = –10V, I_D = –8.4A, T_J=125°C		33	42	
g_{FS}	Forward Transconductance	V_{DS} = –5V, I_D = –8.4A		23		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –20V, V_{GS} = 0V, f = 1MHz		1790	2380	pF
C_{oss}	Output Capacitance			260	345	pF
C_{rss}	Reverse Transfer Capacitance			140	205	pF
R_g	Gate Resistance	f = 1MHz		4		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = –20V, I_D = –8.4A V_{GS} = –10V, R_{GEN} = 6Ω		8	16	ns
t_r	Rise Time			15	27	ns
$t_{d(off)}$	Turn-Off Delay Time			34	55	ns
t_f	Fall Time			14	26	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{DD} =–20V, I_D = –8.4A V_{GS} = –5V		19	27	nC
Q_{gs}	Gate to Source Gate Charge			5.6		nC
Q_{gd}	Gate to Drain "Miller" Charge			6.1		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = –8.4A (Note 2)		–0.85	–1.2	V
t_{rr}	Reverse Recovery Time	I_F = –8.4A, di/dt = 100A/μs		30	45	ns
Q_{rr}	Reverse Recovery Charge			31	47	nC

Notes:
1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to- ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

a. 40°C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 96°C/W when mounted on a minimum pad.

2: Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.
3: Starting T_J = 25°C, L = 3mH, I_{AS} = 9A, V_{DD} = 40V, V_{GS} = 10V.

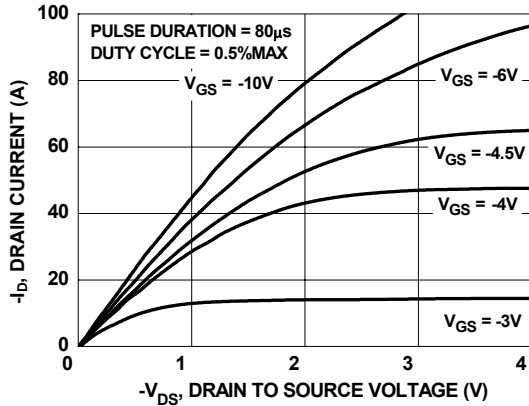**Typical Characteristics** T_J = 25°C unless otherwise noted
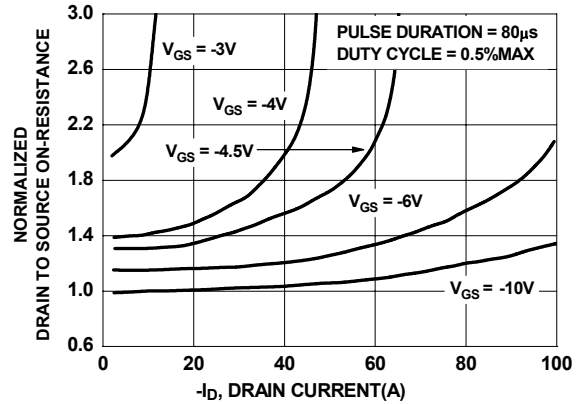
Figure 1. On Region Characteristics

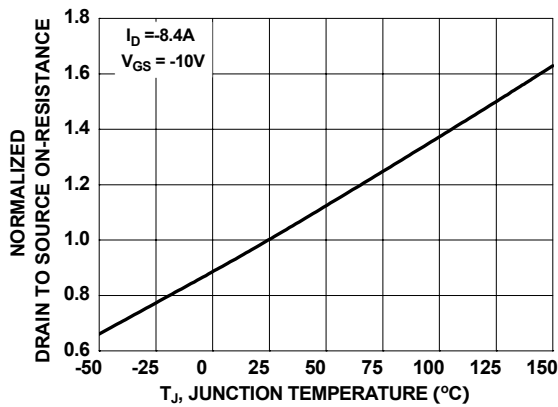**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

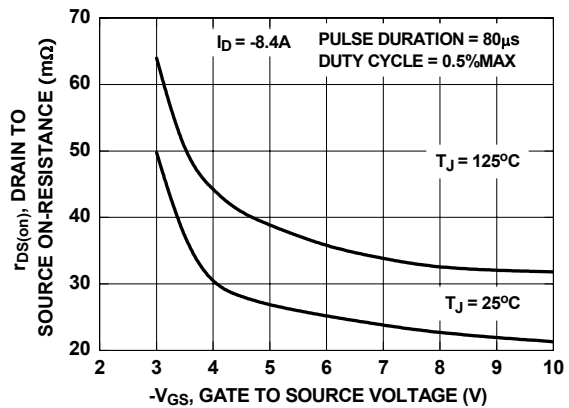**Figure 3. Normalized On Resistance vs Junction Temperature**

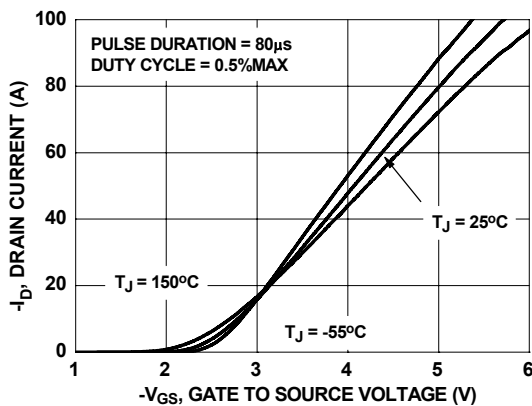**Figure 4. On-Resistance vs Gate to Source Voltage**

Figure 5. Transfer Characteristics
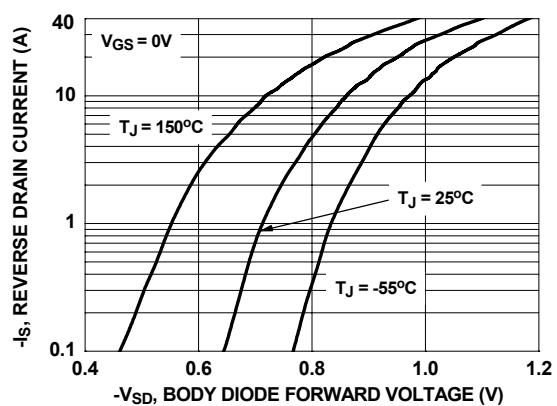
Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

Figure 7. Gate Charge Characteristics
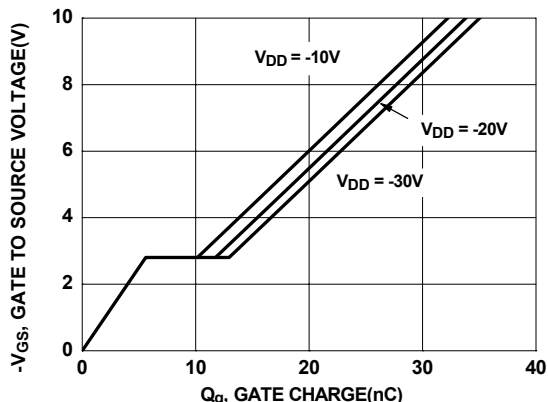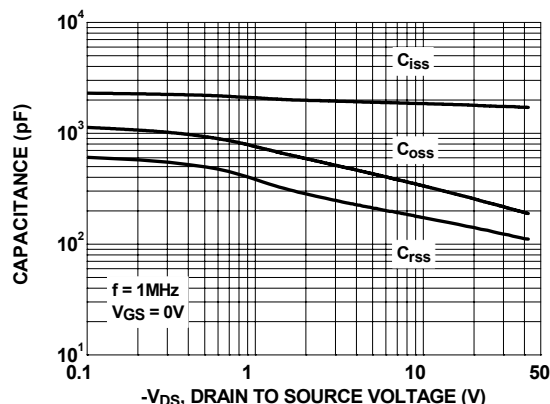

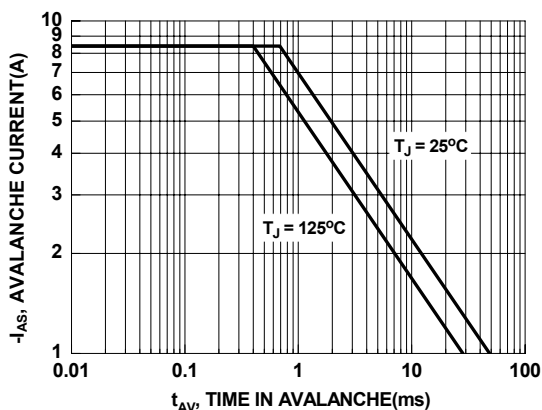Figure 8. Capacitance vs Drain to Source Voltage

Figure 9. Unclamped Inductive Switching Capability

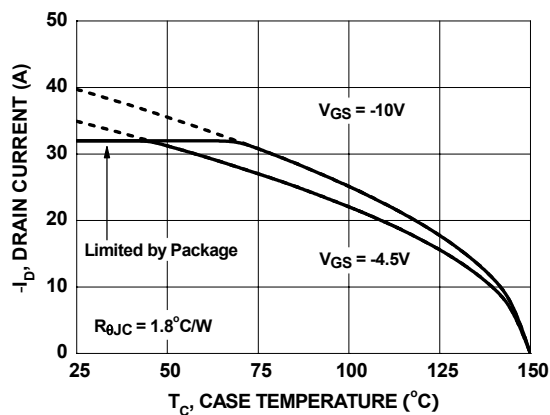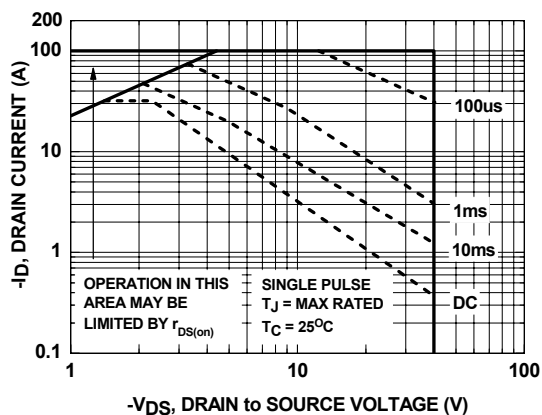Figure 10. Maximum Continuous Drain Current vs Case Temperature
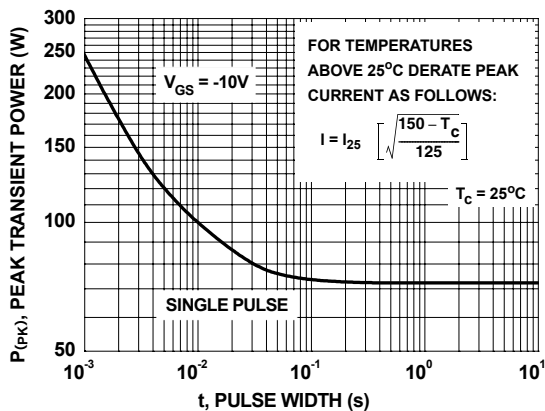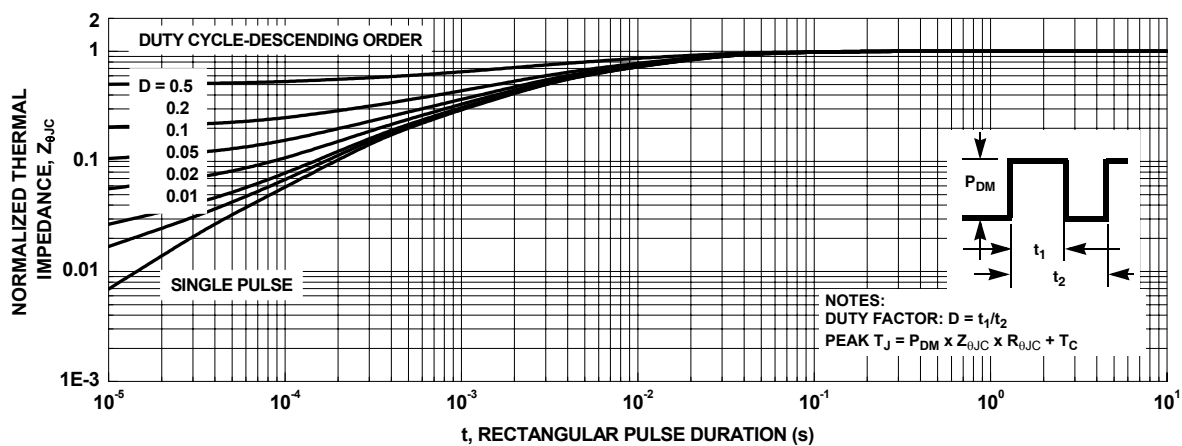

Figure 11. Forward Bias Safe Operating Area

Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

Figure 13. Transient Thermal Response Curve

6.73
6.35

5.46
5.21

[A]

1.27
0.89

6.22
5.97

[E]
1.02 MAX

[C]

1   2   3

0.25 MAX

ISOLATED PLASTIC
BODY STUB

(0.59)

1.14
0.76

0.89
0.64

2.29

⌖ 0.25 Ⓜ AⓂ C

DIODE
PRODUCTS VERSION

4.57

NON-DIODE
PRODUCTS VERSION

5.55 MIN

4

6.50 MIN

6.40

1   3

2.85 MIN

1.25 MIN

2.28

4.56

LAND PATTERN
RECOMMENDATION

SEE
NOTE D

4.32 MIN

4

5.21 MIN

3   2   [E]   1

NON-DIODE
PRODUCTS VERSION

3   2   1

DIODE
PRODUCTS VERSION

[B]

2.39
2.18

0.58
0.45

10.41
9.40

SEE DETAIL A

⌓ 0.10 B

GAGE PLANE

0.51

0.61
0.45

10°
0°

(1.54)

1.78
1.40

0.127 MAX

(2.90)

SEATING PLANE

DETAIL A
(ROTATED -90°)
SCALE: 12X

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NOTES: UNLESS OTHERWISE SPECIFIED
  A) THIS PACKAGE CONFORMS TO JEDEC, TO-252,
     ISSUE C, VARIATION AA.
  B) ALL DIMENSIONS ARE IN MILLIMETERS.
  C) DIMENSIONING AND TOLERANCING PER
     ASME Y14.5M-2009.
  D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED
     CORNERS OR EDGE PROTRUSION.
  E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
  F) DIMENSIONS ARE EXCLUSIVE OF BURS,
     MOLD FLASH AND TIE BAR EXTRUSIONS.
  G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD
     TO228P991X239-3N.
  H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11

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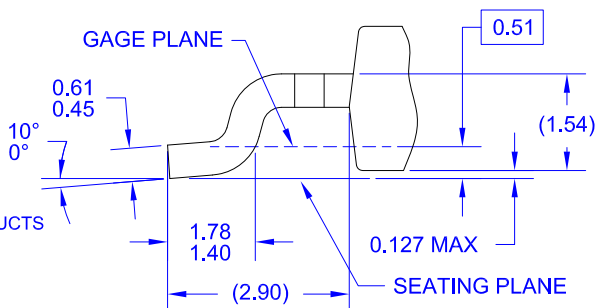|			
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