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STW29NK50ZD

N-CHANNEL 500 V - 0.095Ω - 29A TO-247
Fast Diode SuperMESH™ MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _W
STW29NK50ZD	500 V	< 0.13 Ω	29 A	350 W

- TYPICAL R_{DS(on)} = 0.095 Ω
- HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY
- FAST INTERNAL RECOVERY TIME

DESCRIPTION

The Fast SuperMesh™ series associates all advantages of reduced on-resistance, zener gate protection and very good dv/dt capability with a Fast body-drain recovery diode. Such series complements the "FDmesh™" Advanced Technology.

APPLICATIONS

- HID BALLAST
- ZVS PHASE-SHIFT FULL BRIDGE

Figure 1: Package

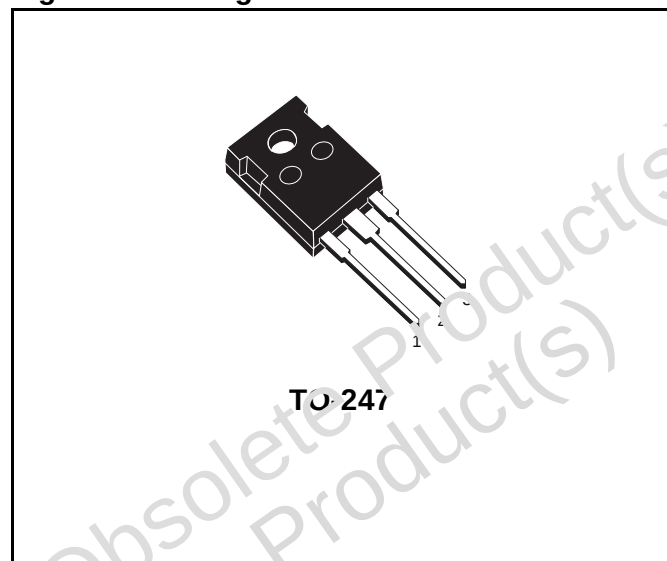


Figure 2: Internal Schematic Diagram

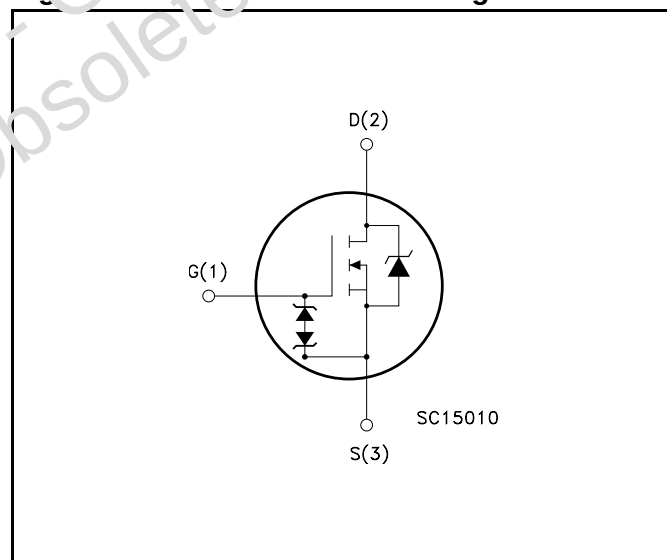


Table 2: Order Codes

PART NUMBER	MARKING	PACKAGE	PACKAGING
STW29NK50ZD	W29NK50ZD	TO-247	TUBE

STW29NK50ZD

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	500	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20\text{ K}\Omega$)	500	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	29	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	18.27	A
$I_{DM}^{(*)}$	Drain Current (pulsed)	116	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	350	W
	Derating Factor	2.77	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD (HBM-C = 100pF, R = 1.5 K Ω)	6000	V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5	V/ μs
T_{stg} T_j	Storage Temperature Operating Junction Temperature	-55 to 150	$^\circ\text{C}$

(*) Pulse width limited by safe operating area

(1) $I_{SD} \leq 29\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq 400\text{ V}$

Table 4: Thermal Data

Rthj-case	Thermal Resistance Junction-case Max	0.36	$^\circ\text{C}/\text{W}$
Rthj-amb T_I	Thermal Resistance Junction-ambient Max Maximum Lead Temperature For Soldering Purpose	50 300	$^\circ\text{C}/\text{W}$ $^\circ\text{C}$

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Non-Repetitive (pulse width limited by T_j max)	29	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	500	mJ

Table 6: Gate-Source Zener Diode

Symbol	Parameter	Test Condition	Min.	Typ.	Max	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1\text{ mA}$ (Open Drain)	30			A

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

TABLE 7: ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ UNLESS OTHERWISE SPECIFIED)

On /Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}$, $V_{GS} = 0$	500			S
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 150 \mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 14.5 \text{ A}$		0.095	0.13	Ω

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15 \text{ V}$, $I_D = 14.5 \text{ A}$		28		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$		6450 710 165		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	$V_{DD} = 400 \text{ V}$, $I_D = 14.5 \text{ A}$, $R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$ (d see Figure 17)		45 43 133 25		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 400 \text{ V}$, $I_D = 14.5 \text{ A}$, $V_{GS} = 10 \text{ V}$		180 33 108	200	nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (2)$	Source-Drain Current Source-Drain Current (pulsed)				29 116	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 29 \text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 29 \text{ A}$, $di/dt = 100 \text{ A}/\mu s$ $V_{DD} = 30 \text{ V}$, $T_J = 25^{\circ}C$ (see Figure 18)		264 2.08 15.7		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 29 \text{ A}$, $di/dt = 100 \text{ A}/\mu s$ $V_{DD} = 30 \text{ V}$, $T_J = 150^{\circ}C$ (see Figure 18)		395 4.164 21.1		ns μC A

(1) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

STW29NK50ZD

Figure 3: Safe Operating Area

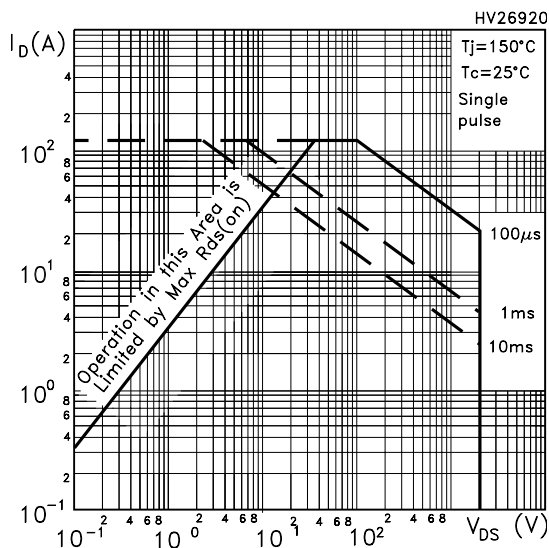


Figure 4: Output Characteristics

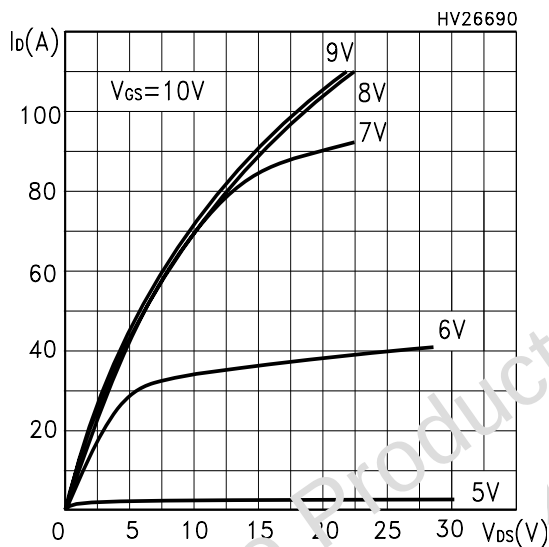


Figure 5: Transconductance

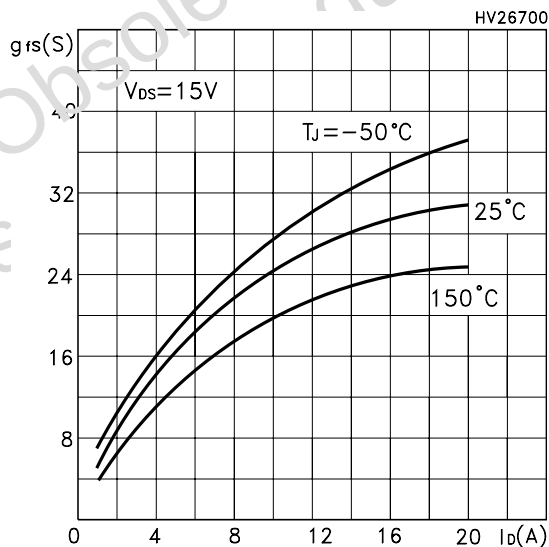


Figure 6: Thermal Impedance

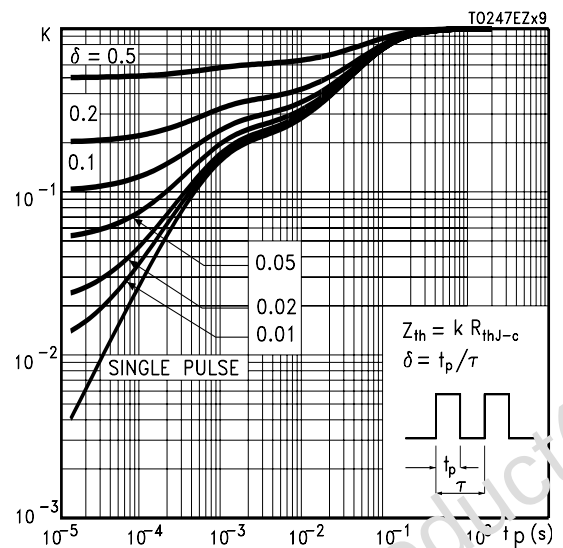


Figure 7: Transfer Characteristics

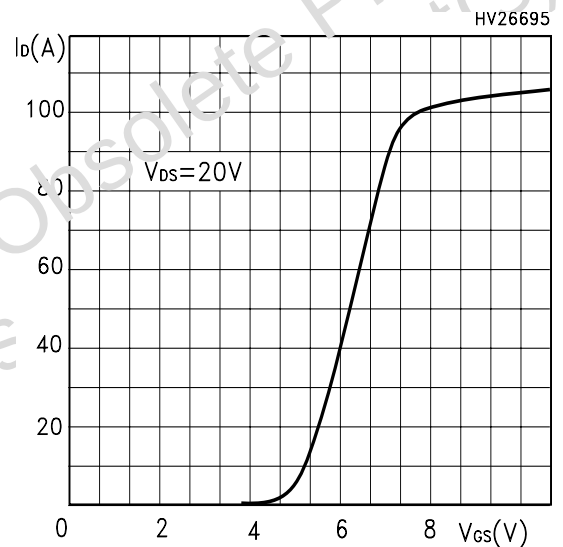


Figure 8: Static Drain-source On Resistance

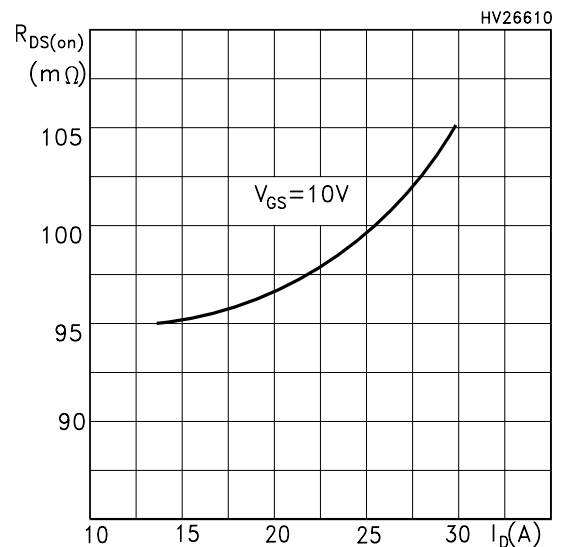


Figure 9: Gate Charge vs Gate-source Voltage

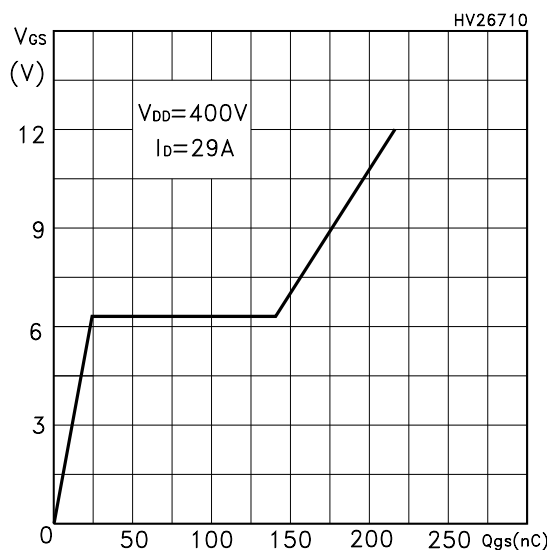


Figure 10: Normalized Gate Threshold Voltage vs Temperature

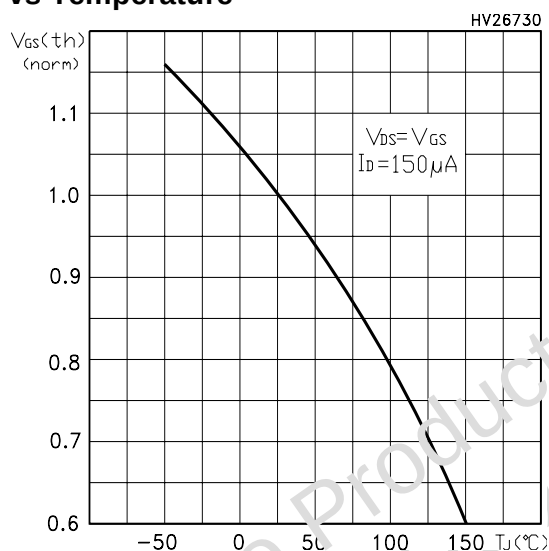


Figure 11: Source-Drain Diode Forward Characteristics

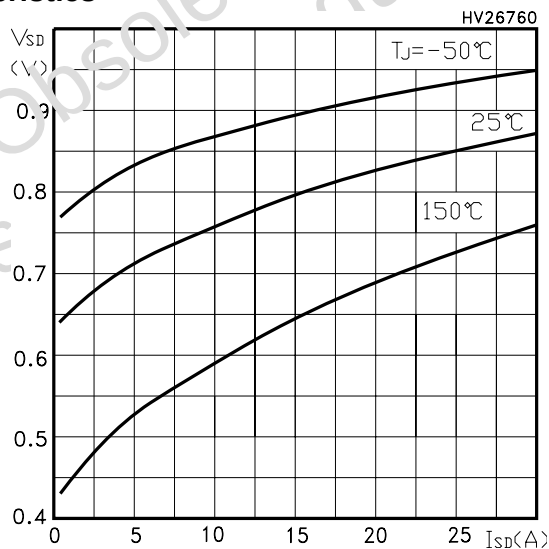


Figure 12: Capacitance Variations

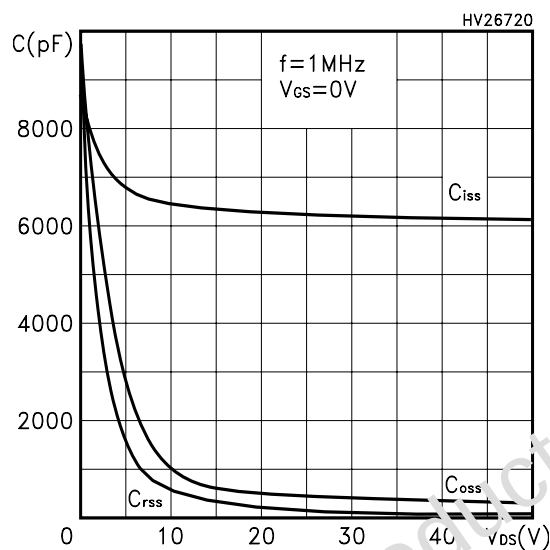


Figure 13: Normalized On Resistance vs Temperature

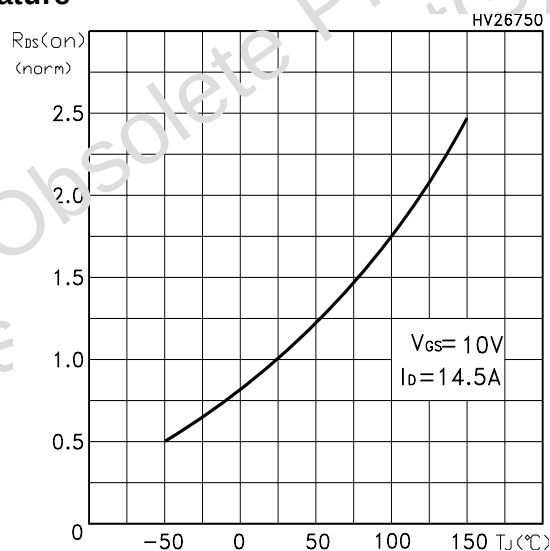
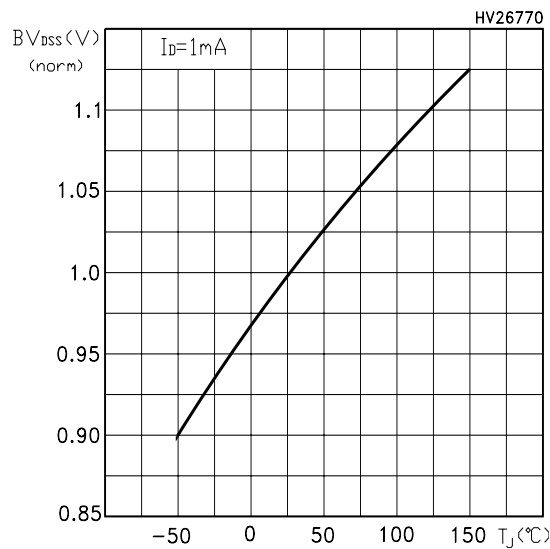
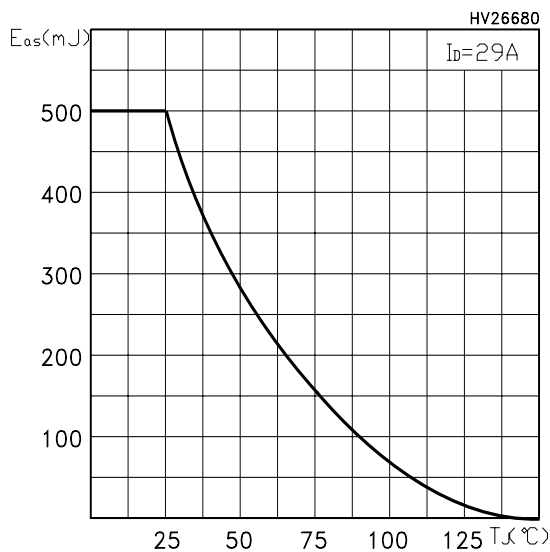


Figure 14: Normalized BVdss vs Temperature



STW29NK50ZD

Figure 15: Avalanche Energy vs Starting T_j



Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

Figure 16: Unclamped Inductive Load Test Circuit

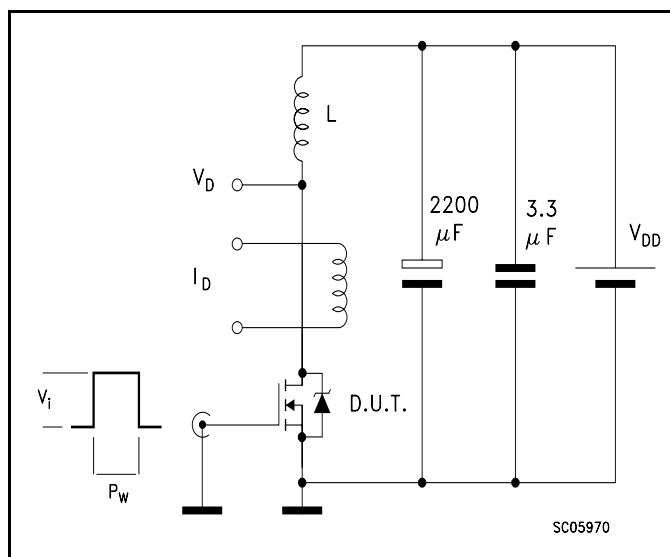


Figure 17: Switching Times Test Circuit For Resistive Load

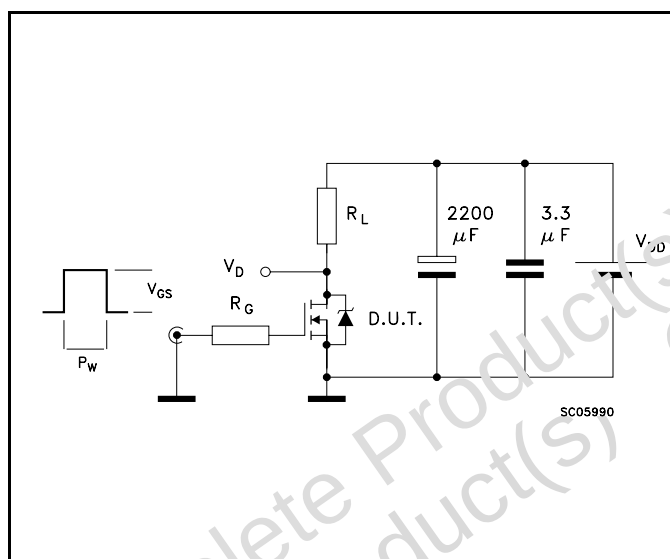


Figure 18: Test Circuit For Inductive Load Switching and Diode Recovery Times

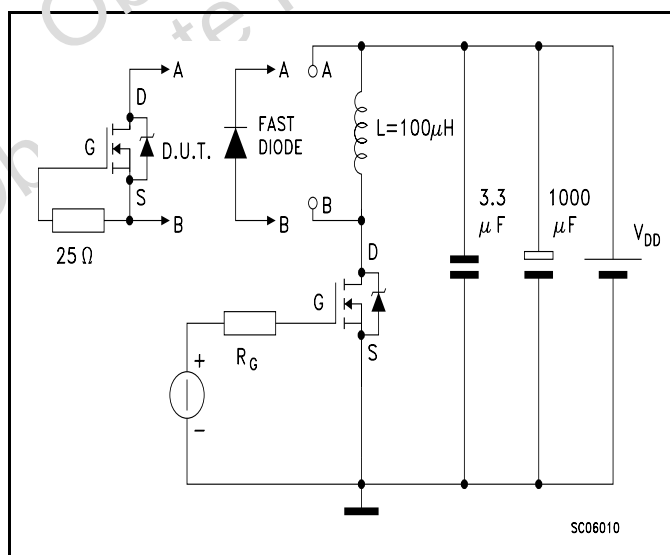


Figure 19: Unclamped Inductive Wafeform

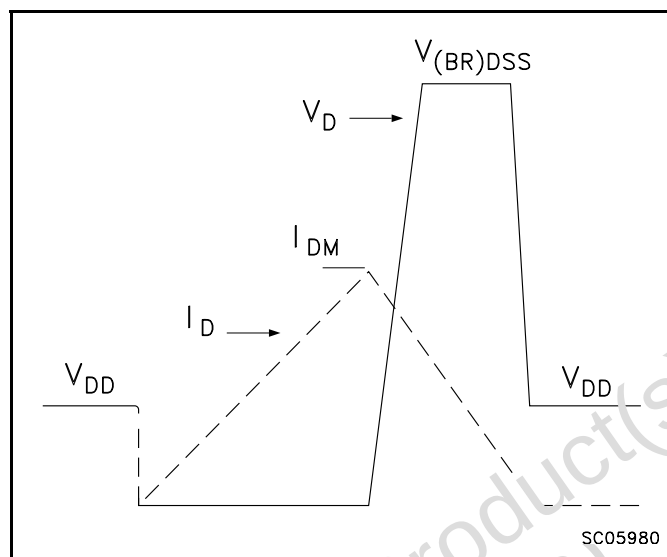
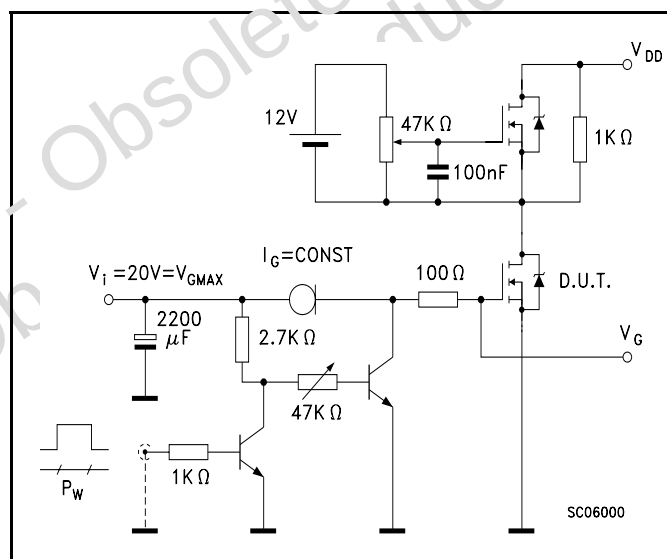


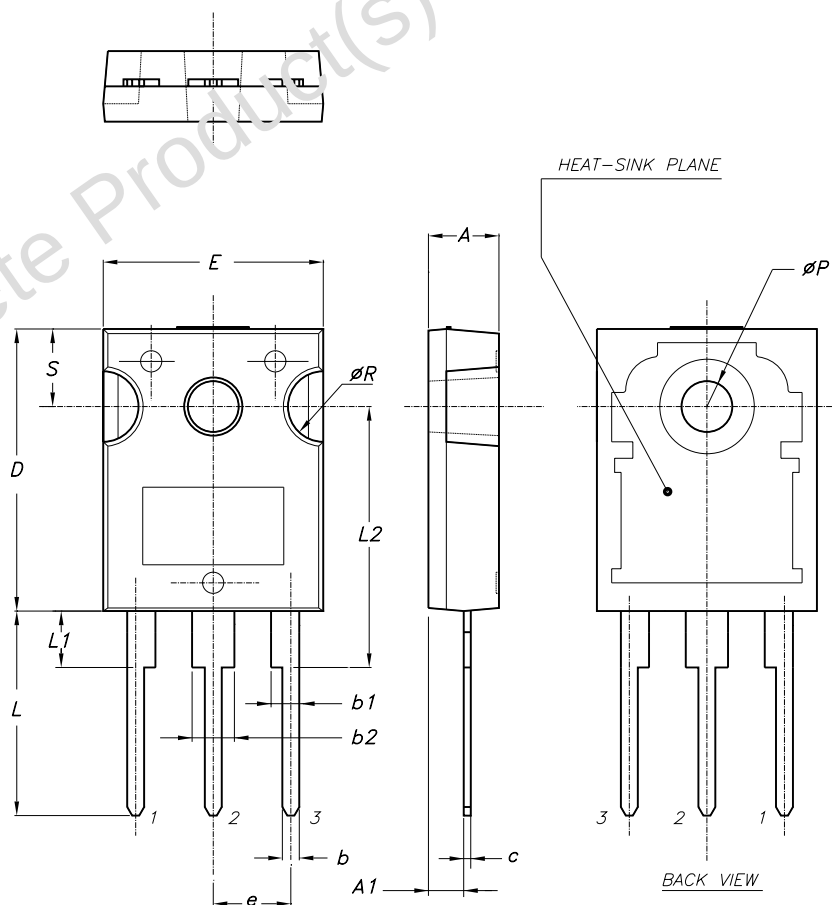
Figure 20: Gate Charge Test Circuit



STW29NK50ZD

TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.031
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



Rev.E

Table 10: Revision History

Date	Revision	Description of Changes
05-Feb-2004	1	First Release.
06-Dec-2004	2	Some electrical value changed
20-Jul-2005	3	Complete version

Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

STW29NK50ZD

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