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ON Semiconductor MC10H175FN

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MC10H175

Quint Latch

Description

The MC10H175 is a quint D type latch with common reset and clock lines. This MECL 10KH part is a functional/pinout duplication of the standard MECL $10K^{TM}$ family part, with 100% improvement in propagation delay and no increase in power–supply current.

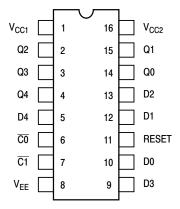
Features

- Propagation Delay, 1.2 ns Typical
- Power Dissipation, 400 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K Compatible
- Pb-Free Packages are Available*

TRUTH TABLE

D	C0	C1	Reset	Q _{n+1}
L	L	L	Х	L
Н	L	L	Х	Н
Х	Н	Х	L	Qn
Х	Х	Н	L	Qn
Х	Н	Х	Н	L
Х	Х	Н	Н	L

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



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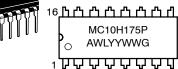
MARKING DIAGRAMS*







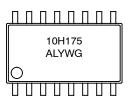
L SUFFIX

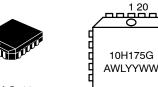


PDIP-16 P SUFFIX CASE 648



SOEIAJ-16 CASE 966





PLLC-20 FN SUFFIX CASE 775

 $\begin{array}{ll} \mathsf{A} & = \mathsf{Assembly\ Location} \\ \mathsf{WL},\, \mathsf{L} & = \mathsf{Wafer\ Lot} \end{array}$

YY, Y = Year WW, W = Work Week G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

^{*}For additional marking information, refer to Application Note AND8002/D.

Datasheet of MC10H175FN - IC DTYPE LATCH QUINT 20PLCC

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MC10H175

Table 1. MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V _{EE}	Power Supply (V _{CC} = 0)	-8.0 to 0	Vdc
VI	Input Voltage (V _{CC} = 0)	0 to V _{EE}	Vdc
l _{out}	Output Current - Continuous - Surge	50 100	mA
T _A	Operating Temperature Range	0 to +75	°C
T _{stg}	Storage Temperature Range - Plastic - Ceramic	-55 to +150 -55 to +165	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

Table 2. ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V $\pm 5\%$) (Note 1)

		O)°	2	5°	7	75°	
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
Ι _Ε	Power Supply Current	_	107	-	97	-	107	mA
linH	Input Current High Pins 5,6,7,9,10,12,13 Pin 11	- -	565 1120	- -	335 660	- -	335 660	μΑ
I _{inL}	Input Current Low	0.5	-	0.5	-	0.3	-	μΑ
V _{OH}	High Output Voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V _{OL}	Low Output Voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V _{IH}	High Input Voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V _{IL}	Low Input Voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Each MECL 10H™ series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been
established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is
maintained. Outputs are terminated through a 50 Ω resistor to −2.0 V.

Table 3. AC PARAMETERS

		()°	2	5°	7	75°	
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
t _{pd}	Propagation Delay							ns
•	Data	0.6	1.6	0.6	1.6	0.6	1.7	
	Clock	0.7	1.9	0.7	2.0	8.0	2.1	
	Reset	1.0	2.2	1.0	2.3	1.0	2.4	
t _{set}	Set-up Time	1.5	-	1.5	-	1.5	-	ns
t _{hold}	Hold Time	0.8	-	0.8	-	0.8	-	ns
t _r	Rise Time	0.5	1.8	0.5	1.9	0.5	2.0	ns
t _f	Fall Time	0.5	1.8	0.5	1.9	0.5	2.0	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Datasheet of MC10H175FN - IC DTYPE LATCH QUINT 20PLCC

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MC10H175

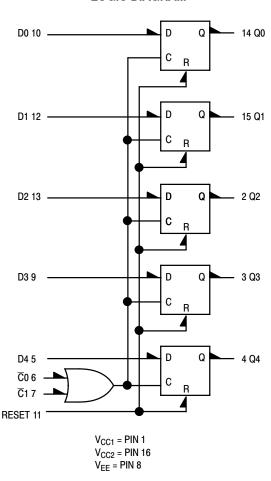
APPLICATION INFORMATION

The MC10H175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the

positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. THE RESET INPUT IS ENABLED ONLY WHEN THE CLOCK IS IN THE HIGH STATE.

LOGIC DIAGRAM





Datasheet of MC10H175FN - IC DTYPE LATCH QUINT 20PLCC

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MC10H175

ORDERING INFORMATION

Device	Package	Shipping [†]
MC10H175FN	PLLC-20	46 Units / Rail
MC10H175FNG	PLLC-20 (Pb-Free)	46 Units / Rail
MC10H175FNR2	PLLC-20	500 / Tape & Reel
MC10H175FNR2G	PLLC-20 (Pb-Free)	500 / Tape & Reel
MC10H175L	CDIP-16	25 Unit / Rail
MC10H175M	SOEIAJ-16	50 Unit / Rail
MC10H175MG	SOEIAJ-16 (Pb-Free)	50 Unit / Rail
MC10H175P	PDIP-16	25 Unit / Rail
MC10H175PG	PDIP-16 (Pb-Free)	25 Unit / Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

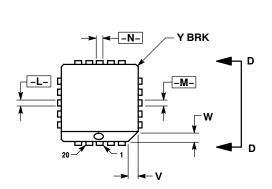
Datasheet of MC10H175FN - IC DTYPE LATCH QUINT 20PLCC

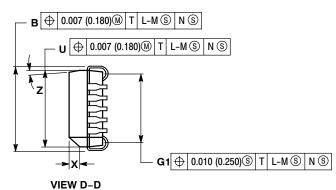
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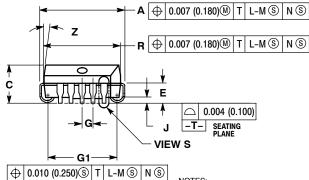
MC10H175

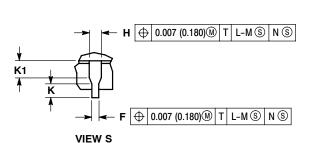
PACKAGE DIMENSIONS

20 LEAD PLLC CASE 775-02 **ISSUE E**









- NOTES:
 1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M,

- DIMENSIONS AND TOLERANGING FER ANSI T14.5M, 1982.
 DIMENSIONS IN INCHES.
 DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
 DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
 DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
 DIMENSIONS IN THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE
- BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
 DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INC	HES	MILLIM	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.385	0.395	9.78	10.03
В	0.385	0.395	9.78	10.03
ဂ	0.165	0.180	4.20	4.57
Е	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050	BSC	1.27	BSC
H	0.026	0.032	0.66	0.81
J	0.020	-	0.51	
K	0.025		0.64	
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
٧	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
Х	0.042	0.056	1.07	1.42
Υ		0.020		0.50
Ζ	2°	10°	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040		1.02	

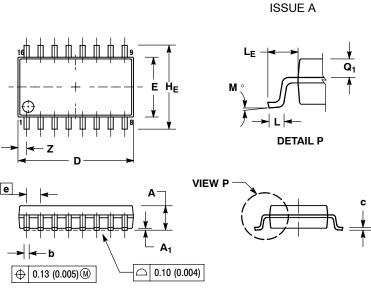
Datasheet of MC10H175FN - IC DTYPE LATCH QUINT 20PLCC

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MC10H175

PACKAGE DIMENSIONS

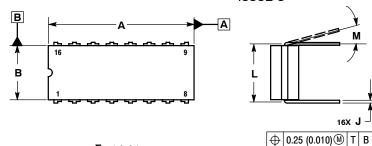
SOEIAJ-16 CASE 966-01

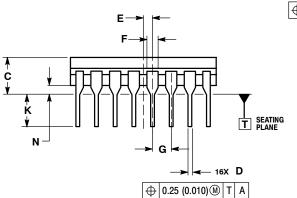


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 TERMINAL NUMBERS ARE SHOWN FOR
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003)
 TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018). TO BE 0.46 (0.018).

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
С	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
Ε	5.10	5.45	0.201	0.215
е	1.27	BSC	0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10°	0°	10 °
Q_1	0.70	0.90	0.028	0.035
Z		0.78		0.031

CDIP-16 **L SUFFIX** CERAMIC DIP PACKAGE CASE 620A-01 ISSUE O





- NOTES: 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCH.
 DIMENSION L TO CENTER OF LEAD WHEN
 FORMED PARALLEL.
- FORMED PARALLEL.
 DIMENSION F MAY NARROW TO 0.76 (0.030)
 WHERE THE LEAD ENTERS THE CERAMIC
 BODY.
 THIS DRAWING REPLACES OBSOLETE
 CASE OUTLINE 620-10.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
С		0.200		5.08	
D	0.015	0.020	0.39	0.50	
Е	0.050	BSC	1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100	BSC	2.54 BSC		
Η	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300 BSC		7.62 BSC		
M	0°	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	

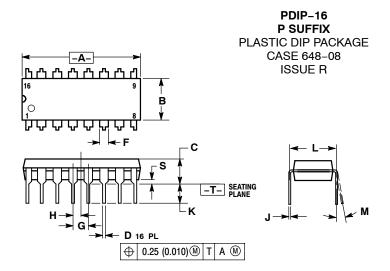


Datasheet of MC10H175FN - IC DTYPE LATCH QUINT 20PLCC

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PACKAGE DIMENSIONS



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
 DIMENSION L TO CENTER OF LEADS WHEN
 FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.740	0.770	18.80	19.55
В	0.250	0.270	6.35	6.85
С	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54 BSC	
Н	0.050	BSC	1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10 °
S	0.020	0.040	0.51	1.01

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