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Fairchild Semiconductor DM74ALS645AN

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SEMICONDUCTORIM

March 1987 Revised February 2000

DM74ALS645A **Octal Bus Transceivers**

General Description

These octal bus transceivers are designed for asynchronous two-way communication between data busses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G) can be used to disable the device so the busses are effectively

Features

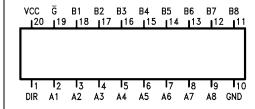
- Advanced Oxide-isolated Ion-implanted Schottky TTL process
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Switching performance specified at 50 pF
- PNP input design reduces input loading

Ordering Code:

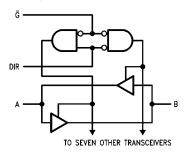
Order Number	Package Number	Package Description
DM74ALS645AWM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74ALS645AN	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Logic Diagram



Function Table

	ontrol puts	Operation
G	DIR	
L	L	B Data to A Bus
L	Н	A Data to B Bus
Н	Х	Isolation

L = LOW Logic Level

H = HIGH Logic Level X = Either LOW or HIGH Logic Level



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Datasheet of DM74ALS645AN - IC TRANSCVR TRI-ST 8BIT 20DIP

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DM74ALS645A

Absolute Maximum Ratings(Note 1)

Supply Voltage 7V

Input Voltage;

 Control Inputs
 7V

 I/O Ports
 5.5V

Operating Free Air Temperature Range $0^{\circ}\text{C to } +70^{\circ}\text{C}$ Storage Temperature Range $-65^{\circ}\text{C to } +150^{\circ}\text{C}$

Typical θ_{JA}

N Package $$53.0^{\circ}\text{C/W}$$ M Package $$72.0^{\circ}\text{C/W}$$

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Min Typ		Units
V _{CC}	Supply Voltage	4.5	5	5.5	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-15	mA
I _{OL}	LOW Level Output Current			24	mA
T _A	Operating Free Air Temperature Range	0		70	°C

Electrical Characteristics

Over Recommended Free Air Temperature Range

Symbol	Parameter	Test	Min	Тур	Max −1.5	Units V		
V _{IC}	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$						
V _{OH}	HIGH Level Output Voltage	$V_{CC} = 4.5 \text{ to } 5.5 \text{V}$	5 to 5.5V $I_{OH} = -0.4 \text{ mA}$					
		V _{CC} = Max	$I_{OH} = -3 \text{ mA}$	2.4	3.2		V	
			I _{OH} = Max	2				
V _{OL}	LOW Level Output Voltage	V _{CC} = Min	I _{OL} = 12 mA		0.25	0.4	V	
			$I_{OL} = 24 \text{ mA}$		0.35	0.5		
I _I	Input Current at	V _{CC} = Max	I/O Ports, V _I = 5.5V			100		
	Maximum Input Voltage		Control Inputs, $V_I = 7V$			100	μА	
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V (Note 2)				20	μΑ	
I _{IL}	LOW Level Input Current	$V_{CC} = Max, V_I = 0.4V (N$			-100	μΑ		
Io	Output Drive Current	$V_{CC} = Max, V_O = 2.25V$		-30		-112	mA	
I _{CC}	Supply Current	V _{CC} = Max	Outputs HIGH		30	45		
			Outputs LOW		36	55	mA	
			Outputs Disabled		38	58	1	

 $\textbf{Note 2:} \ \, \text{For I/O ports, I}_{\text{IH}} \ \, \text{and I}_{\text{IL}} \ \, \text{parameters include the 3-STATE output current (I}_{\text{OZL}} \ \, \text{and I}_{\text{OZH}}).$

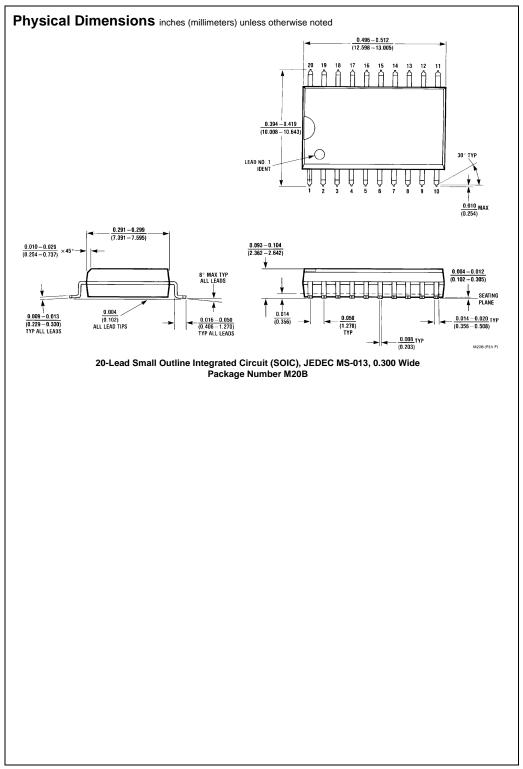
Switching Characteristics

Over Recommended Operating Free Air Temperature Range

Symbol	Parameter	From (Input)	To (Output)	Conditions	Min	Max	Units
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	A or B	B or A	$V_{CC} = 4.5 \text{ to } 5.5 \text{V},$ $C_L = 50 \text{ pF},$	3	10	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	A or B	B or A	R1 = R2 = 500Ω	3	10	ns
t _{PZH}	Output Enable Time to HIGH Level Output	G	A or B		5	20	ns
t _{PZL}	Output Enable Time to LOW Level Output	G	A or B		5	20	ns
t _{PHZ}	Output Disable Time from HIGH Level Output	G	A or B		2	10	ns
t _{PLZ}	Output Disable Time from LOW Level Output	G	A or B		4	15	ns

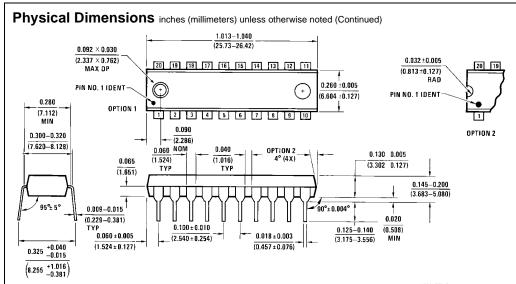
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DM74ALS645A Octal Bus Transceivers



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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