

Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[ON Semiconductor](#)
[NUS1204MNT1G](#)

For any questions, you can email us directly:

sales@integrated-circuit.com

NUS1204MN

Overvoltage Protection IC with Integrated MOSFET

This device represents a new level of safety and integration by combining the NCP304 overvoltage protection circuit (OVP) with a -12 V P-Channel power MOSFET. It is specifically designed to protect sensitive electronic circuitry from overvoltage transients and power supply faults. During such hazardous events, the IC quickly disconnects the input supply from the load, thus protecting the load before any damage can occur.

The OVP IC is optimized for applications using an external AC-DC adapter or a car accessory charger to power a portable product or recharge its internal batteries. It has a nominal overvoltage threshold of 4.725 V which makes it ideal for single cell Li-Ion as well as 3/4 cell NiCD/NiMH applications.

Features

- Overvoltage Turn-Off Time of Less Than 20 μ s
- Accurate Voltage Threshold of 4.725 V, Nominal
- High Accuracy Undervoltage Threshold of 2.0%
- -12 V Integrated P-Channel Power MOSFET
- Low $R_{DS(on)}$ = 75 m Ω @ -4.725 V
- Low Profile 2.0 x 2.0 mm WDFN Package Suitable for Portable Applications
- Maximum Solder Reflow Temperature @ 260°C
- This device is manufactured with a Pb-Free external lead finish only.

Benefits

- Provide Battery Protection
- Integrated Solution Offers Cost and Space Savings
- Integrated Solution Improves System Reliability

Applications

- Portable Computers and PDAs
- Cell Phones and Handheld Products
- Digital Cameras



ON Semiconductor®

<http://onsemi.com>



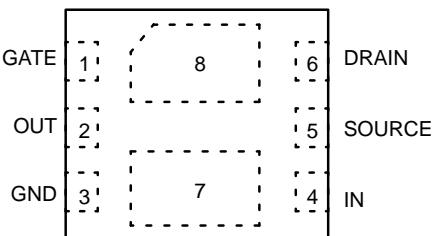
WDFN6
CASE 506AN

MARKING DIAGRAM



U2 = Specific Device Code
 M = Date Code
 ▀ = Pb-Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping [†]
NUS1204MNT1G	WDFN6 (Pb-Free)	3000 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NUS1204MN

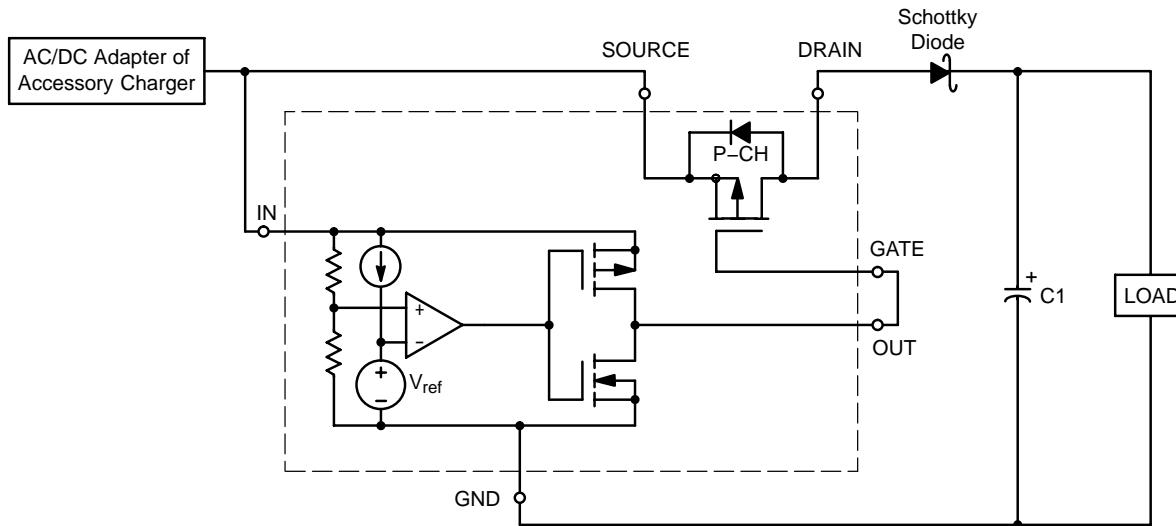


Figure 1. Simplified Schematic

PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	GATE	Gate pin of the P-Channel Power MOSFET
2	OUT	This signal drives the gate of a P-Channel Power MOSFET. It is controlled by the voltage level on the IN pin. When an overvoltage event is detected, the OUT pin is driven to within 1.0 V of V_{IN} in less than 20 μ sec provided that gate and stray capacitance is less than 12 nF.
3, 7	GND	Circuit Ground
4	IN	This pin senses an external voltage point. If the voltage on this input rises above the overvoltage threshold (V_{TH}), the OUT pin will be driven to within 1.0 V of V_{IN} , thus disconnecting the P-Channel Power MOSFET. The nominal threshold level is 4.725 V and this threshold level can be increased with the addition of an external resistor between the IN pin and the adapter.
5	SOURCE	Source pin of the P-Channel Power MOSFET
6, 8	DRAIN	Drain pin of the P-Channel Power MOSFET

OVERVOLTAGE PROTECTION CIRCUIT TRUTH TABLE

IN	OUT
$<V_{th}$	GND
$>V_{th}$	V_{IN}

NUS1204MN

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise stated)

Rating	Pin	Symbol	Min	Max	Unit
OUT Voltage to GND	2	V_O	-0.3	12	V
Input Pin Voltage to GND	4	V_{input}	-0.3	12	V
Maximum Power Dissipation (Note 1)	-	P_D	-	0.96	W
Thermal Resistance Junction-to-Air (Note 1) OVP IC P-Channel FET	-	$R_{\theta JA}$	-	130 130	°C/W
Junction Temperature	-	T_J	-	150	°C
Operating Ambient Temperature	-	T_A	-40	85	°C
Storage Temperature Range	-	T_{stg}	-65	150	°C
ESD Performance (HBM) (Note 2)	2,3,4	-	2.5	-	kV
Drain-to-Source Voltage		V_{DSS}		-12	V
Gate-to-Source Voltage		V_{GS}	-8	8	V
Continuous Drain Current, Steady State, $T_A = 25^\circ\text{C}$ (Note 1)		I_D		-0.6	A

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Human body model (HBM): MIL STD 883C Method 3015-7, ($R = 1500 \Omega$, $C = 100 \text{ pF}$, $F = 3$ pulses delay 1 s).

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{\text{cc}} = 6.0 \text{ V}$, unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Threshold (Pin 4, V_{in} Increasing)	V_{TH}	4.630	4.725	4.820	V
Input Threshold Hysteresis (Pin 4, V_{in} Decreasing)	V_{HYS}	0.135	0.225	0.315	V
Supply Current (Pin 4) ($V_{\text{in}} = 4.34 \text{ V}$) ($V_{\text{in}} = 6.5 \text{ V}$)	I_{in}	- -	- -	3.0 3.9	μA
Minimum Operating Voltage (Pin 4) (Note 3) ($T_A = 25^\circ\text{C}$) ($T_A = -40^\circ\text{C}$ to 85°C)	$V_{\text{in(min)}}$	- -	0.55 0.65	0.70 0.80	V
Output Voltage High ($V_{\text{in}} = 8.0 \text{ V}$; $I_{\text{Source}} = 1.0 \text{ mA}$) Output Voltage High ($V_{\text{in}} = 8.0 \text{ V}$; $I_{\text{Source}} = 0.25 \text{ mA}$) Output Voltage High ($V_{\text{in}} = 8.0 \text{ V}$; $I_{\text{Source}} = 0 \text{ mA}$)	V_{oh}	$V_{\text{in}}-1.0$ $V_{\text{in}}-0.25$ $V_{\text{in}}-0.1$	-	-	V
Output Voltage Low (Input $< 4.5 \text{ V}$; $I_{\text{Sink}} = 0 \text{ mA}$; CNTRL = 0 V)	V_{ol}	-	-	0.1	V
Propagation Delay Input to Output Complementary Output NCP304 Series Output Transition, High to Low Output Transition, Low to High	t_{pHL} t_{plH}	- -	10 21	- 60	μs

3. Guaranteed by design.

NUS1204MN

P-CHANNEL MOSFET ($T_A = 25^\circ\text{C}$, unless otherwise specified)

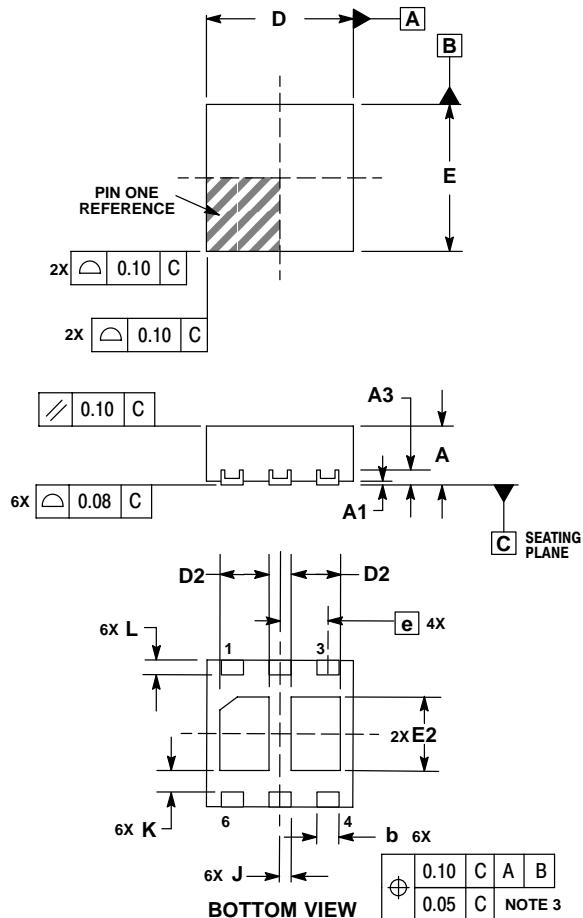
Parameter	Symbol	Min	Typ	Max	Units
Drain to Source On Resistance $V_{GS} = -4.5 \text{ V}$, $I_D = 600 \text{ mA}$ $V_{GS} = -4.5 \text{ V}$, $I_D = 1.0 \text{ A}$	$R_{DS(on)}$		75 75	100 100	$\text{m}\Omega$
Zero Gate Voltage Drain Current $V_{GS} = -4.5 \text{ V}$, $V_{GS} = 0 \text{ V}$, $V_{DS} = -10 \text{ V}$	I_{DSS}			-1.0	μA
Turn On Delay (Note 4) $V_{GS} = -4.5 \text{ V}$	t_{on}		5.5		ns
Turn Off Delay (Note 4) $V_{GS} = -4.5 \text{ V}$	t_{off}		20		ns
Input Capacitance $V_{GS} = 0 \text{ V}$, $f = 1.0 \text{ MHz}$, $V_{DS} = -10 \text{ V}$	C_{in}		531		pF
Gate to Source Leakage Current $V_{GS} = 8.0 \text{ V}$, $V_{DS} = 0 \text{ V}$	I_{GSS}		± 10		nA
Drain to Source Breakdown Voltage $V_{GS} = 0 \text{ V}$, $I_D = -250 \mu\text{A}$	$V_{(BR)DSS}$	-12			V
Gate Threshold Voltage $V_{GS} = V_{DS}$, $I_D = -250 \mu\text{A}$	$V_{(GS)th}$	-0.4	-0.7	-1.0	V

4. Switching characteristics are independent of operating junction temperature.

NUS1204MN

PACKAGE DIMENSIONS

WDFN6, 2x2
CASE 506AN-01
ISSUE B

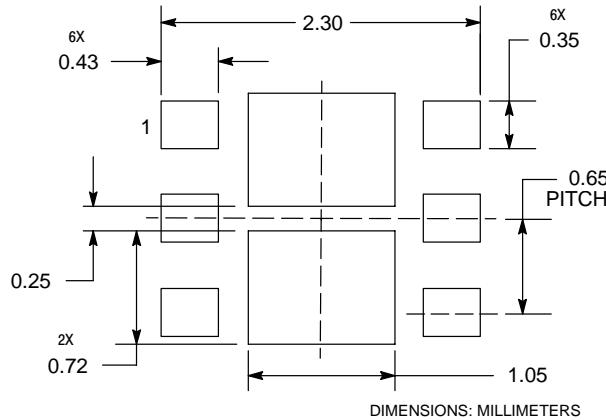


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION *b* APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
K	0.25 REF	
L	0.20	0.30
J	0.15 REF	

SOLDERMASK DEFINED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
 P.O. Box 5163, Denver, Colorado 80217 USA
 Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
 Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
 Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
 USA/Canada

Europe, Middle East and Africa Technical Support:

Phone: 421 33 790 2910

Japan Customer Focus Center

Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
 Sales Representative