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TXB0101 1-Bit Bidirectional Level-Shifting and Voltage Translator With Auto Direction-Sensing and ± 15 -kv ESD Protection

1 Features

- Available in the Texas Instruments NanoFree™ Package
- 1.2 V to 3.6 V on A Port and 1.65 V to 5.5 V on B Port ($V_{CCA} \leq V_{CCB}$)
- V_{CC} Isolation Feature – If Either V_{CC} Input is at GND, All Outputs are in the High-Impedance State
- OE Input Circuit Referenced to V_{CCA}
- Low Power Consumption, 5 μ A Maximum I_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - A Port
 - 2000 V Human Body Model (A114-B)
 - 250 V Machine Model (A115-A)
 - 1500 V Charged-Device Model (C101)
 - B Port
 - 15 kV Human Body Model (A114-B)
 - 250 V Machine Model (A115-A)
 - 1500 V Charged-Device Model (C101)

2 Applications

- Handsets
- Smartphones
- Tablets
- Desktop PCs

3 Description

This 1-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes. V_{CCA} should not exceed V_{CCB} .

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

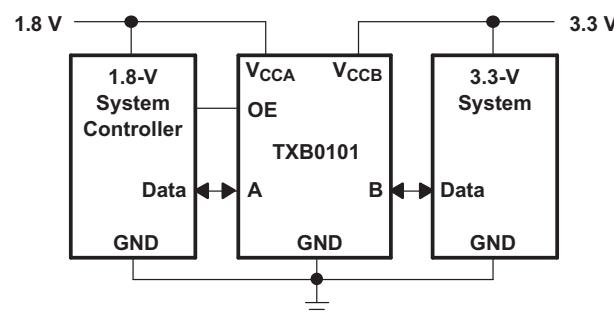
NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TXB0101	SOT-23 (6)	2.90 mm x 1.60 mm
	SC70 (6)	2.00 mm x 1.25 mm
	SOT (6)	1.60 mm x 1.20 mm
	DSBGA (6)	1.1 mm x 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Operating Circuit



An **IMPORTANT NOTICE** at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. **PRODUCTION DATA**.

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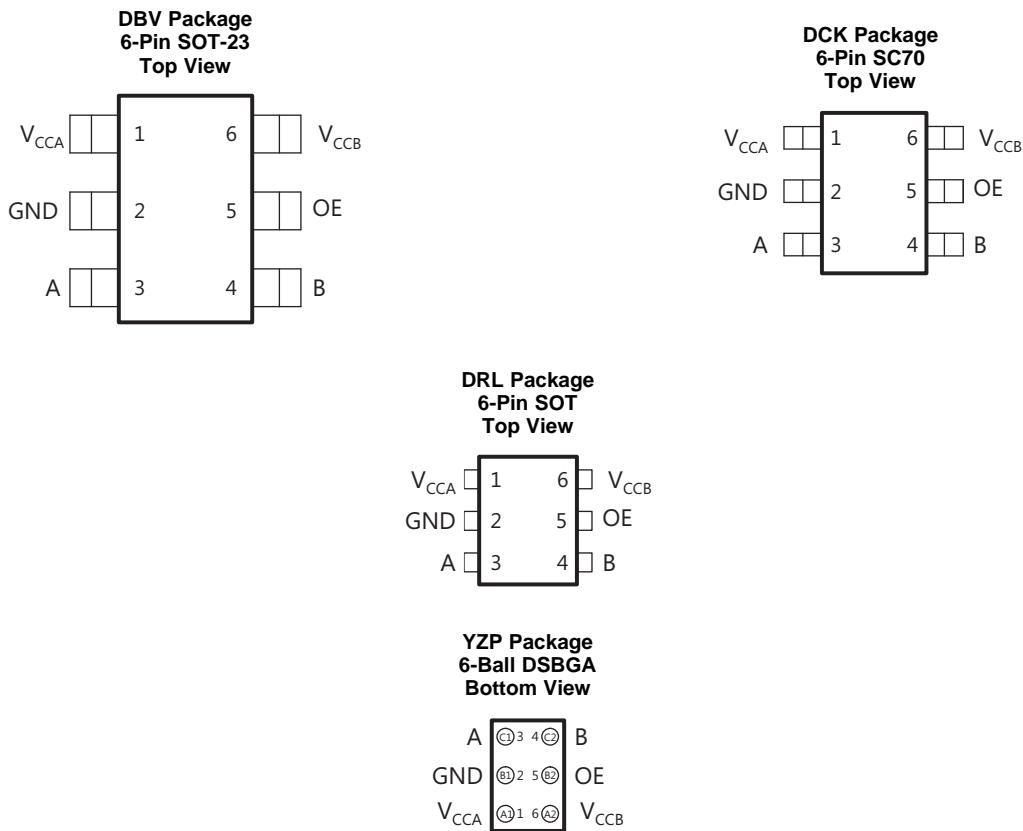
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2012) to Revision C	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Removed <i>Ordering Information</i> table	1

Changes from Revision A (November 2008) to Revision B	Page
• Added notes to pin out graphics	3

5 Pin Configuration and Functions



- A. See mechanical drawings for dimensions.
- B. Pullup resistors are not required on both sides for Logic I/O.
- C. If pullup or pulldown resistors are needed, the resistor value must be over 50 kΩ.
- D. 50 kΩ is a safe recommended value, if the customer can accept higher V_{OL} or lower V_{OH}, smaller pullup or pulldown resistor is allowed, the draft estimation is V_{OL} = V_{CCout} × 4.5 k / (4.5 k + R_{pu}) and V_{OH} = V_{CCout} × R_{dw} / (4.5 k + R_{dw}).
- E. If pull up resistors are needed, please refer to the TXS0101 or contact TI.
- F. For detailed information, please refer to application note [SCEA043](#).

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	V _{CCA}	—	A-port supply voltage. 1.2 V ≤ V _{CCA} ≤ 3.6 V and V _{CCA} ≤ V _{CCB}
2	GND	—	Ground
3	A	I/O	Input/output A. Referenced to V _{CCA} .
4	B	I/O	Input/output B. Referenced to V _{CCB} .
5	OE	I	3-state output enable. Pull OE low to place all outputs in 3-state mode. Referenced to V _{CCA} .
6	V _{CCB}	—	B-port supply voltage. 1.65 V ≤ V _{CCB} ≤ 5.5 V

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6 Specification

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CCA}	Supply voltage	-0.5	4.6	V
V_{CCB}	Supply voltage	-0.5	6.5	
V_I	Input voltage ⁽²⁾	-0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V_O	Voltage applied to any output in the high or low state ^{(2) (3)}	A port B port	-0.5 -0.5	$V_{CCA} + 0.5$ $V_{CCB} + 0.5$
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		± 50	mA
	Continuous current through V_{CCA} , V_{CCB} , or GND		± 100	mA
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative Voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 15	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 1500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See ⁽¹⁾ ⁽²⁾.

		V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage			1.2	3.6	V
				1.65	5.5	
V_{IH}	High-level input voltage	Data inputs	1.2 V to 3.6 V	$V_{CCI} \times 0.65$ ⁽³⁾	V_{CCI}	V
		OE	1.2 V to 3.6 V	$V_{CCA} \times 0.65$	5.5	
V_{IL}	Low-level input voltage	Data inputs	1.2 V to 5.5 V	0	$V_{CCI} \times 0.35$ ⁽³⁾	V
		OE	1.2 V to 3.6 V	$V_{CCA} \times 0.35$	0	
$\Delta t/\Delta v$	Input transition rise or fall rate	A-port inputs	1.2 V to 3.6 V	1.65 V to 5.5 V	40	ns/V
		B-port inputs	1.2 V to 3.6 V	1.65 V to 3.6 V	40	
				4.5 V to 5.5 V	30	
T_A	Operating free-air temperature			-40	85	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at V_{CCI} or both at GND.

(2) V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.

(3) V_{CCI} is the supply voltage associated with the input port.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TXB0101				UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	YZP (DSBGA)	
		6 PINS	6 PINS	6 PINS	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	192.3	266.9	204.2	105.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	164.8	80.4	76.4	1.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	38.6	99.1	38.7	10.8	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	43.7	1.5	3.4	3.1	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	38.1	98.3	38.5	10.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

PARAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}	T _A = 25°C			-40°C to 85°C			UNIT			
				MIN	TYP	MAX	MIN	TYP	MAX				
V _{OHA}	I _{OH} = -20 μA	1.2 V		1.1			V _{CCA} – 0.4			V			
		1.4 V to 3.6 V											
V _{OLO}	I _{OL} = 20 μA	1.2 V		0.9			0.4			V			
		1.4 V to 3.6 V											
V _{OHB}	I _{OH} = -20 μA		1.65 V to 5.5 V				V _{CCB} – 0.4			V			
V _{OLB}	I _{OL} = 20 μA		1.65 V to 5.5 V				0.4			V			
I _I	OE	1.2 V to 3.6 V	1.65 V to 5.5 V	±1			±2			μA			
I _{off}	A port	0 V	0 V to 5.5 V	±1			±2			μA			
	B port	0 V to 3.6 V	0 V	±1			±2						
I _{OZ}	A or B port	OE = GND	1.2 V to 3.6 V	1.65 V to 5.5 V	±1			±2		μA			
I _{CCA}	V _I = V _{CC1} or GND, I _O = 0	1.2 V	1.65 V to 5.5 V	0.06			3			μA			
		1.4 V to 3.6 V	1.65 V to 5.5 V										
		3.6 V	0 V				2						
		0 V	5.5 V				-2						
I _{CCB}	V _I = V _{CC1} or GND, I _O = 0	1.2 V	1.65 V to 5.5 V	3.4			5			μA			
		1.4 V to 3.6 V	1.65 V to 5.5 V										
		3.6 V	0 V				-2						
		0 V	5.5 V				2						
I _{CCA} + I _{CCB}	V _I = V _{CC1} or GND, I _O = 0	1.2 V	1.65 V to 5.5 V	3.5			8			μA			
		1.4 V to 3.6 V	1.65 V to 5.5 V										
I _{CCZA}	V _I = V _{CC1} or GND, I _O = 0, OE = GND	1.2 V	1.65 V to 5.5 V	0.05			3			μA			
		1.4 V to 3.6 V	1.65 V to 5.5 V										
I _{CCZB}	V _I = V _{CC1} or GND, I _O = 0, OE = GND	1.2 V	1.65 V to 5.5 V	3.3			5			μA			
		1.4 V to 3.6 V	1.65 V to 5.5 V										
C _i	OE	1.2 V to 3.6 V	1.65 V to 5.5 V	2.5			3			pF			
C _{io}	A port	1.2 V to 3.6 V	1.65 V to 5.5 V	5			6			pF			
				11			13						

(1) V_{CC1} is the supply voltage associated with the input port.

(2) V_{CC0} is the supply voltage associated with the output port.

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6.6 Timing Requirements, $V_{CCA} = 1.2 \text{ V}$
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.2 \text{ V}$

		$V_{CCB} = 1.8 \text{ V}$	$V_{CCB} = 2.5 \text{ V}$	$V_{CCB} = 3.3 \text{ V}$	$V_{CCB} = 5 \text{ V}$	UNIT
		TYP	TYP	TYP	TYP	
Data rate		20	20	20	20	Mbps
t_w	Pulse duration	50	50	50	50	ns

6.7 Timing Requirements, $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$ (unless otherwise noted)

		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$	UNIT
		MIN	MAX	MIN	MAX	
Data rate		40	40	40	40	Mbps
t_w	Pulse duration	25	25	25	25	ns

6.8 Timing Requirements, $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$ (unless otherwise noted)

		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$	UNIT
		MIN	MAX	MIN	MAX	
Data rate		60	60	60	60	Mbps
t_w	Pulse duration	17	17	17	17	ns

6.9 Timing Requirements, $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)

		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$	UNIT	
		MIN	MAX	MIN	MAX	
Data rate		100	100	100	100	Mbps
t_w	Pulse duration	10	10	10	10	ns

6.10 Timing Requirements, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$	UNIT
		MIN	MAX	
Data rate		100	100	Mbps
t_w	Pulse duration	10	10	ns

6.11 Switching Characteristics, $V_{CCA} = 1.2 \text{ V}$

$T_A = 25^\circ\text{C}$, $V_{CCA} = 1.2 \text{ V}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8 \text{ V}$	$V_{CCB} = 2.5 \text{ V}$	$V_{CCB} = 3.3 \text{ V}$	$V_{CCB} = 5 \text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
t_{pd}	A	B	6.9	5.7	5.3	5.5	ns
	B	A	7.4	6.4	6	5.8	
t_{en}	OE	A	1	1	1	1	μs
		B	1	1	1	1	
t_{dis}	OE	A	18	15	14	14	ns
		B	20	17	16	16	
t_{rA}, t_{fA}	A-port rise and fall times		4.2	4.2	4.2	4.2	ns
t_{rB}, t_{fB}	B-port rise and fall times		2.1	1.5	1.2	1.1	ns
Max data rate			20	20	20	20	Mbps

6.12 Switching Characteristics, $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.4	12.9	1.2	10.1	1.1	10	0.8	9.9	ns
	B	A	0.9	14.2	0.7	12	0.4	11.7	0.3	13.7	
t_{en}	OE	A		1		1		1		1	μs
		B		1		1		1		1	
t_{dis}	OE	A	5.9	31	5.7	25.9	5.6	23	5.7	22.4	ns
		B	5.4	30.3	4.9	22.8	4.8	20	4.9	19.5	
t_{rA}, t_{fA}	A-port rise and fall times		1.4	5.1	1.4	5.1	1.4	5.1	1.4	5.1	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.9	4.5	0.6	3.2	0.5	2.8	0.4	2.7	ns
Max data rate			40		40		40		40		Mbps

6.13 Switching Characteristics, $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	11	1.4	7.7	1.3	6.8	1.2	6.5	ns
	B	A	1.5	12	1.3	8.4	1	7.6	0.9	7.1	
t_{en}	OE	A		1		1		1		1	μs
		B		1		1		1		1	
t_{dis}	OE	A	5.9	31	5.1	21.3	5	19.3	5	17.4	ns
		B	5.4	30.3	4.4	20.8	4.2	17.9	4.3	16.3	
t_{rA}, t_{fA}	A-port rise and fall times		1	4.2	1.1	4.1	1.1	4.1	1.1	4.1	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.9	4.5	0.6	3.2	0.5	2.8	0.4	2.7	ns
Max data rate			60		60		60		60		Mbps

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6.14 Switching Characteristics, $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.1	6.3	1	5.2	0.9	4.7	ns
	B	A	1.2	6.6	1.1	5.1	0.9	4.4	
t_{en}	OE	A			1		1		μs
		B			1		1		
t_{dis}	OE	A	5.1	21.3	4.6	15.2	4.6	13.2	ns
		B	4.4	20.8	3.8	16	3.9	13.9	
t_{rA}, t_{fA}	A-port rise and fall times		0.8	3	0.8	3	0.8	3	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.7	3	0.5	2.8	0.4	2.7	ns
Max data rate			100		100		100		Mbps

6.15 Switching Characteristics, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

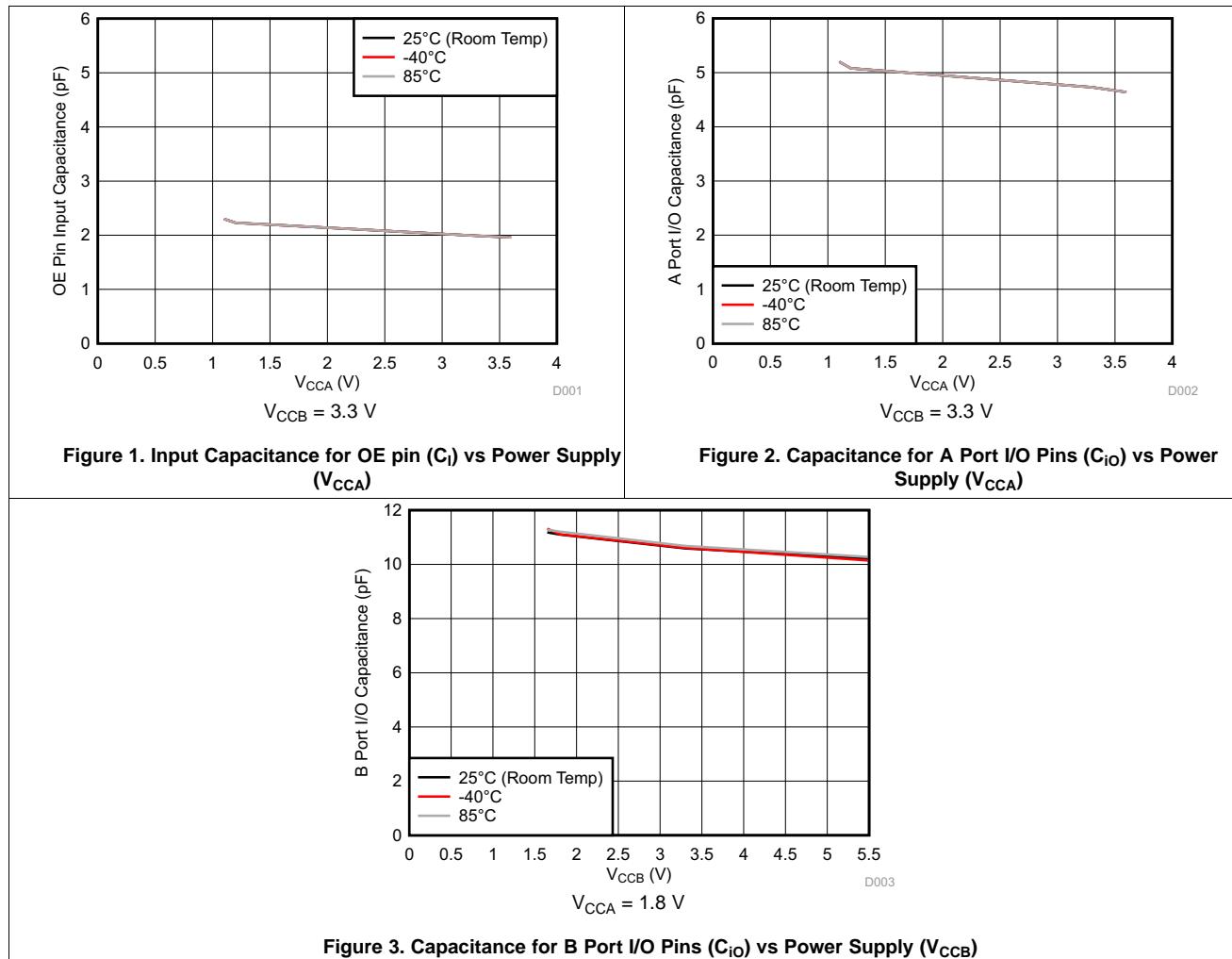
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A	B	0.9	4.7	0.8	4	ns
	B	A	1	4.9	0.9	4.5	
t_{en}	OE	A			1		μs
		B			1		
t_{dis}	OE	A	4.6	15.2	4.3	12.1	ns
		B	3.8	16	3.4	13.2	
t_{rA}, t_{fA}	A-port rise and fall times		0.7	2.5	0.7	2.5	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.5	2.3	0.4	2.7	ns
Max data rate			100		100		Mbps

6.16 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CCA}							UNIT	
		1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V		
		V_{CCB}								
		5 V	1.8 V	1.8 V	1.8 V	2.5 V	5 V	3.3 V to 5 V		
C_{pdA}	A-port input, B-port output	$C_L = 0, f = 10 \text{ MHz}, t_r = t_f = 1 \text{ ns}, OE = V_{CCA}$ (outputs enabled)	7.8	8	8	7	7	8	pF	
	B-port input, A-port output		12	11	11	11	11	11		
	A-port input, B-port output		38.1	28	29	29	29	30		
	B-port input, A-port output		25.4	18	17	17	18	20		
C_{pdA}	A-port input, B-port output	$C_L = 0, f = 10 \text{ MHz}, t_r = t_f = 1 \text{ ns}, OE = GND$ (outputs disabled)	0.01	0.01	0.01	0.01	0.01	0.01	pF	
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01		
	A-port input, B-port output		0.01	0.01	0.01	0.01	0.01	0.02		
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.03		

6.17 Typical Characteristics

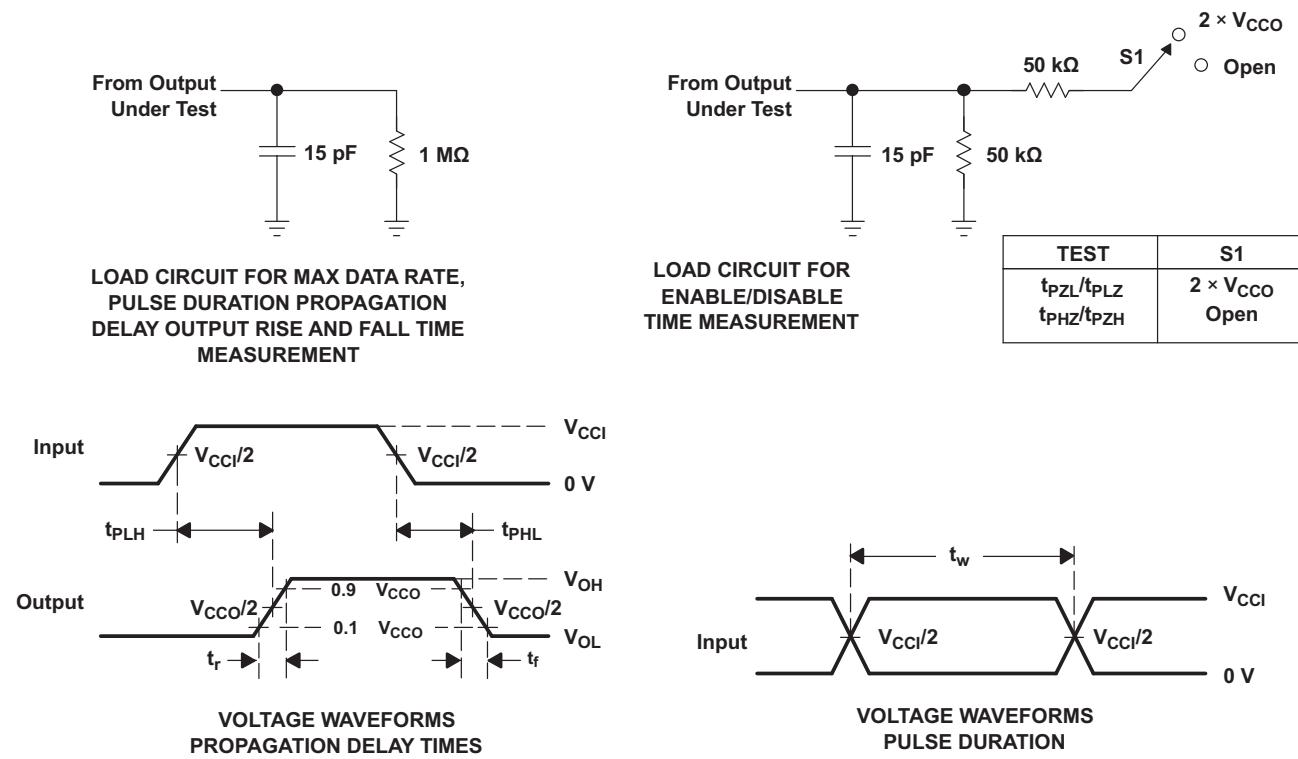


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7 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, $Z_O = 50 \Omega$, $dv/dt \geq 1 \text{ V/ns}$.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{pd} .
- E. V_{CCI} is the V_{CC} associated with the input port.
- F. V_{CCO} is the V_{CC} associated with the output port.
- G. All parameters and waveforms are not applicable to all devices.

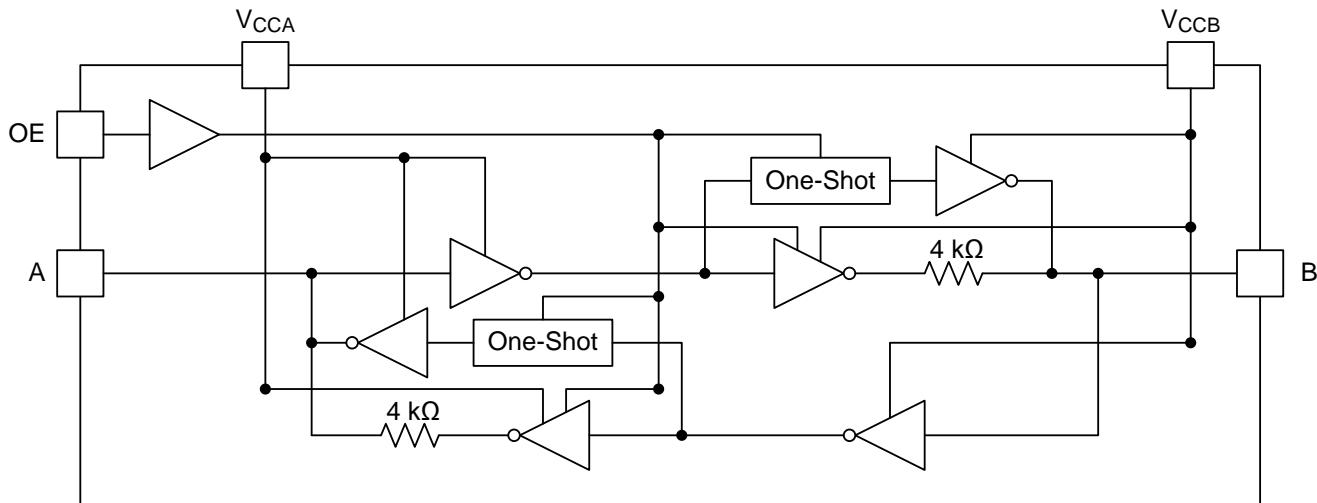
Figure 4. Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Overview

The TXB0101 device is a 1-bit directionless level-shifting and voltage translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The device is a buffered architecture with edge rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI [TXS010X](#) products.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Architecture

The TXB0101 architecture (see [Figure 5](#)) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the TXB0101 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction.

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70 Ω at $V_{CCO} = 1.2$ V to 1.8 V, 50 Ω at $V_{CCO} = 1.8$ V to 3.3 V, and 40 Ω at $V_{CCO} = 3.3$ V to 5 V.

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Feature Description (continued)

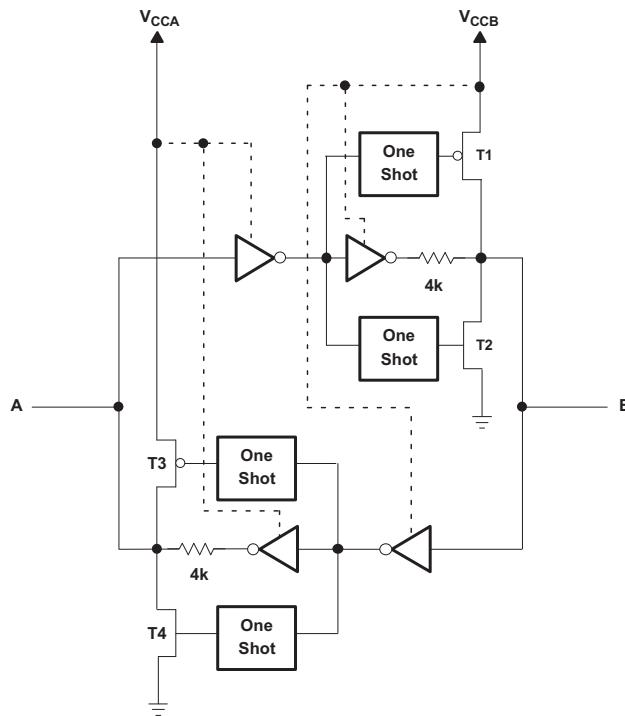


Figure 5. Architecture of TXB0101 I/O Cell

8.3.2 Power Up

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0101 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B} = 0$ V) and are placed in high-impedance state.

8.3.3 Enable and Disable

The TXB0101 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs are actually disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

8.3.4 Pullup or Pulldown Resistors on I/O Lines

The TXB0101 is designed to drive capacitive loads of up to 70 pF. The output drivers of the TXB0101 have low-DC drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 k Ω to ensure that they do not contend with the output drivers of the TXB0101.

For the same reason, the TXB0101 should not be used in applications such as I²C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI [TXS010X](#) series of level translators.

8.4 Device Functional Modes

The TXB0101 device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high-impedance state. Setting the OE input high will enable the device.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TXB0101 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI [TXS010X](#) products. Any external pulldown or pullup resistors are recommended larger than 50 k Ω .

9.2 Typical Application

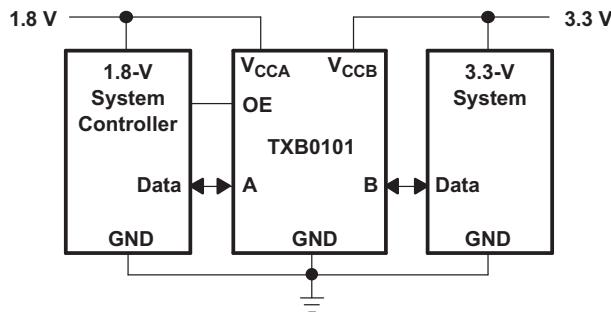


Figure 6. Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#). And make sure that $V_{CCA} \leq V_{CCB}$.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.65 V to 5.5 V

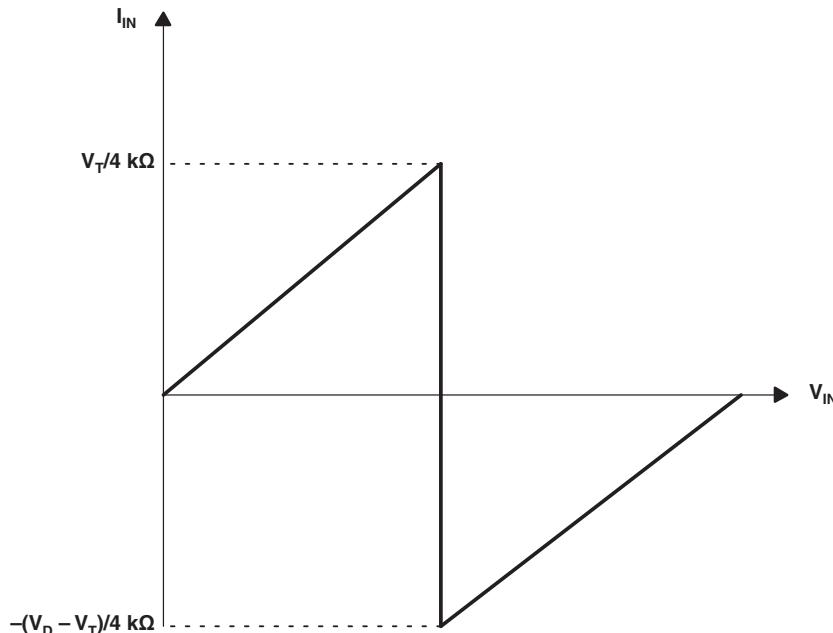
TXB0101

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9.2.1.1 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0101 are shown in [Figure 7](#). For proper operation, the device driving the data I/Os of the TXB0101 must have drive strength of at least ± 2 mA.



- A. V_T is the input threshold voltage of the TXB0101 (typically $V_{CC}/2$).
- B. V_D is the supply voltage of the external driver.

Figure 7. Typical I_{IN} vs V_{IN} Curve

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
 - Use the supply voltage of the device that is driving the TXB0101 device to determine the input voltage range. For a valid logic HIGH the value must exceed the V_{IH} of the input port. For a valid logic LOW the value must be less than the V_{IL} of the input port.
- Output voltage range
 - Use the supply voltage of the device that the TXB0101 device is driving to determine the output voltage range.
 - External pullup or pulldown resistors are not recommended. If mandatory, TI recommends the value should be larger than 50 kΩ.
- An external pulldown or pullup resistor decreases the output V_{OH} and V_{OL} . Use [Equation 1](#) and [Equation 2](#) to draft estimate the V_{OH} and V_{OL} as a result of an external pulldown and pullup resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 4.5 \text{ k}\Omega \quad (1)$$

$$V_{OL} = V_{CCx} \times 4.5 \text{ k}\Omega / (R_{PU} + 4.5 \text{ k}\Omega)$$

where

- V_{CCx} is the output port supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pulldown resistor
- R_{PU} is the value of the external pullup resistor
- 4.5 kΩ is the counting the variation of the serial resistor 4 kΩ in the I/O line. (2)

9.2.3 Application Curve

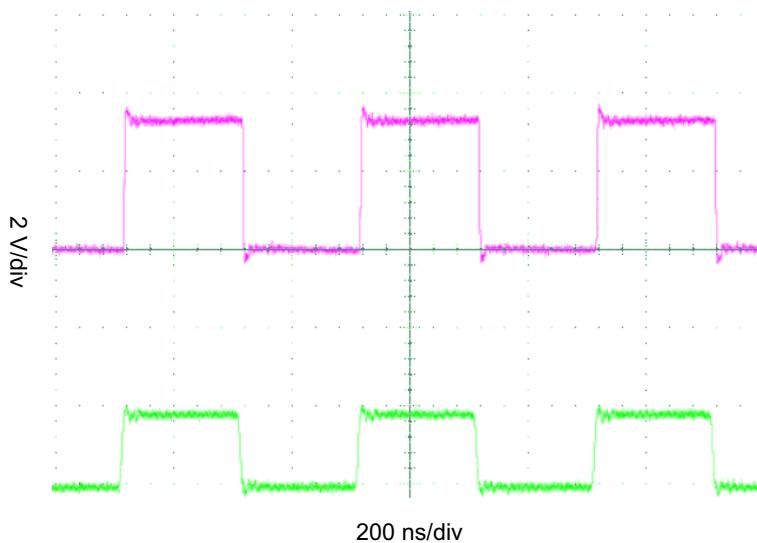
 $V_{CCA} = 1.8 \text{ V}$ (waveform captured at pin 3) $V_{CCB} = 3.3 \text{ V}$ (Waveform captured at pin 4)

Figure 8. Level-Translation of a 2.5-MHz Signal

TXB0101

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10 Power Supply Recommendations

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0101 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B} = 0$ V). The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies. And should be placed as close as possible to the V_{CCA} , V_{CCB} pin and GND pin.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 10 ns, ensuring that any reflection encounters low impedance at the source driver.

11.2 Layout Example

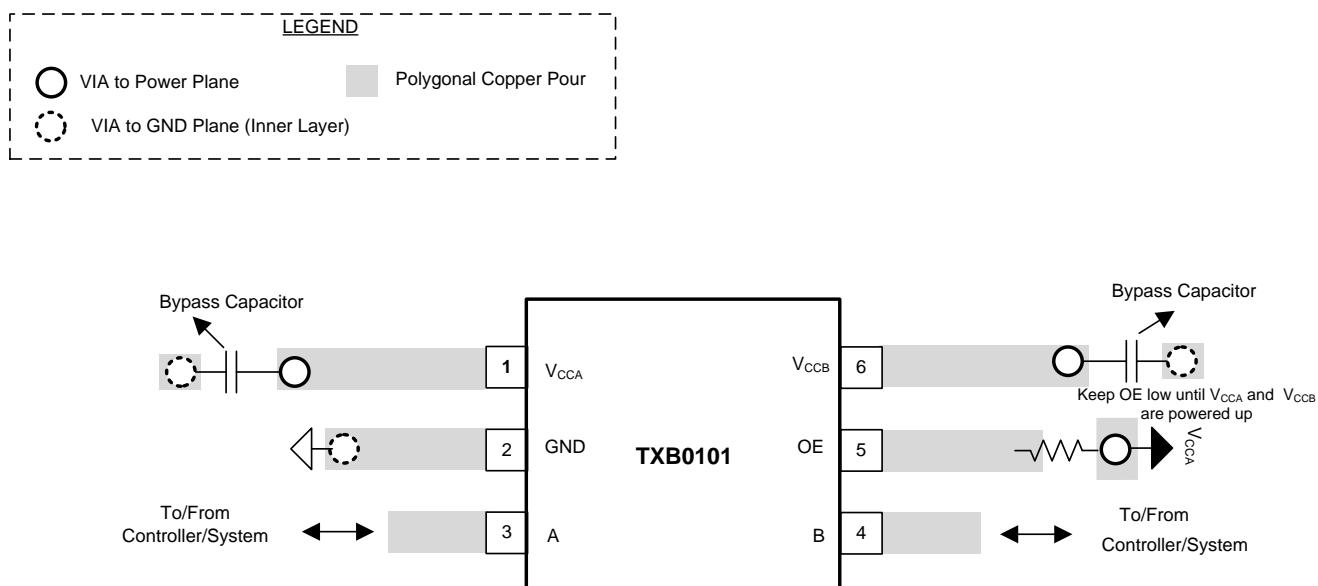


Figure 9. Layout Example Recommendation

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.

All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

 These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022](#) — *TI Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0101DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFCF ~ NFCR)	Samples
TXB0101DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFCF ~ NFCR)	Samples
TXB0101DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFCF ~ NFCR)	Samples
TXB0101DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFCF ~ NFCR)	Samples
TXB0101DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	270	Samples
TXB0101DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	270	Samples
TXB0101DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		270	Samples
TXB0101DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	270	Samples
TXB0101DRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	27R	Samples
TXB0101DRLT	ACTIVE	SOT	DRL	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	27R	Samples
TXB0101YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(277 ~ 27N)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

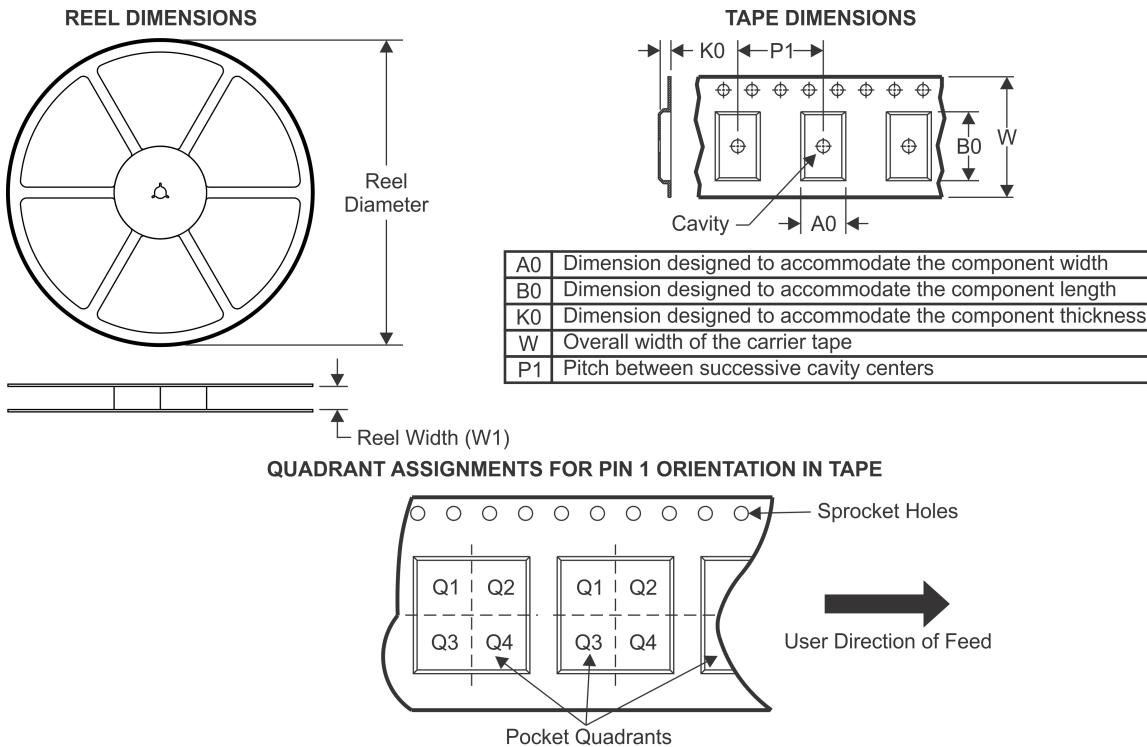
⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

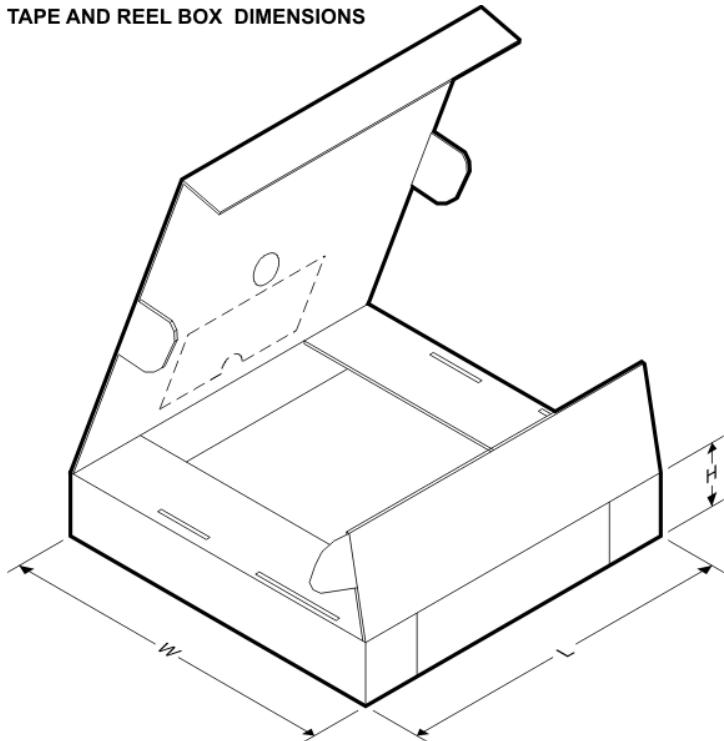
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0101DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TXB0101DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TXB0101DCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TXB0101DCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TXB0101DRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TXB0101DRLT	SOT	DRL	6	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TXB0101YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



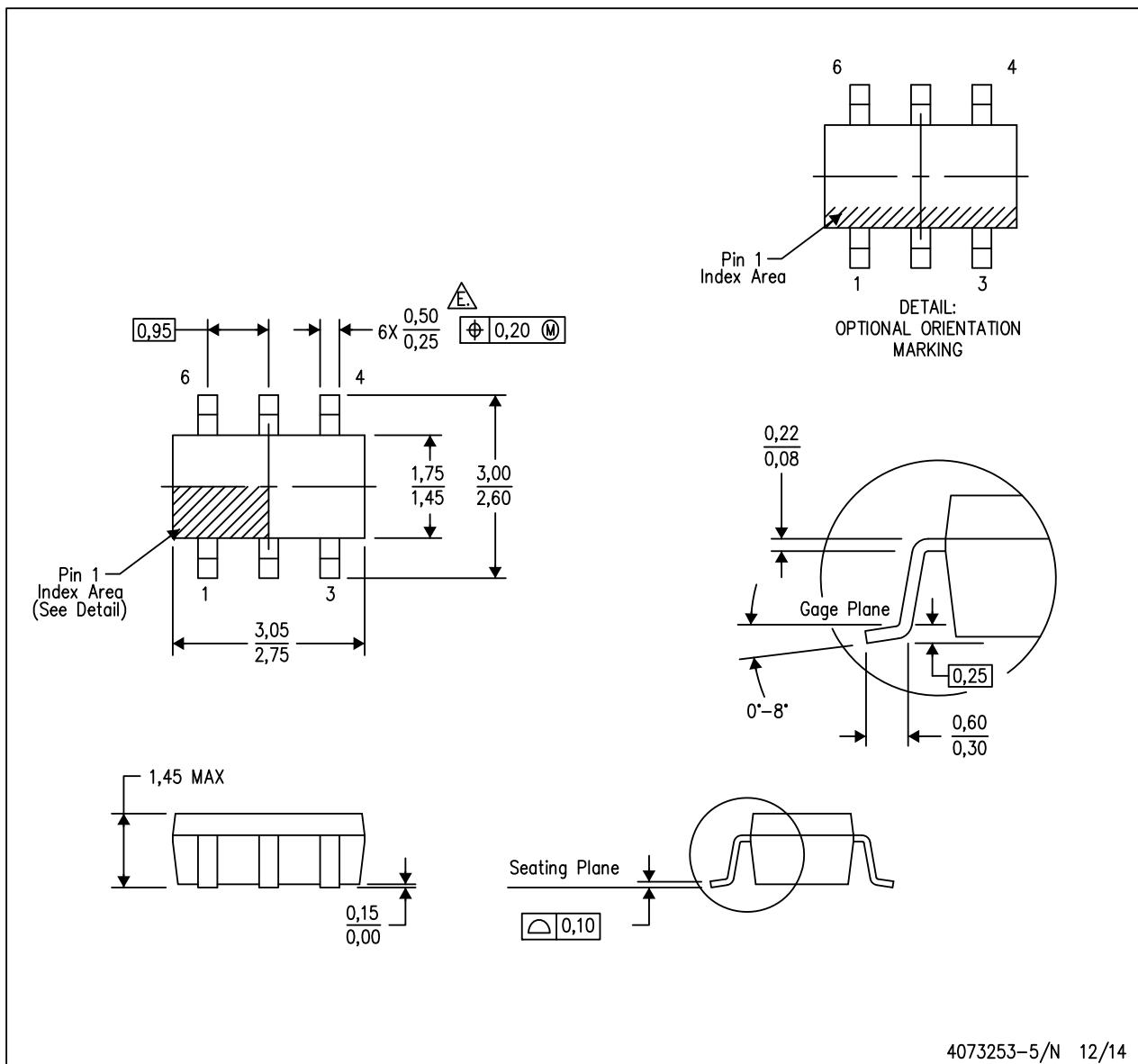
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0101DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
TXB0101DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
TXB0101DCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TXB0101DCKT	SC70	DCK	6	250	203.0	203.0	35.0
TXB0101DRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TXB0101DRLT	SOT	DRL	6	250	202.0	201.0	28.0
TXB0101YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

MECHANICAL DATA

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.

Falls within JEDEC MO-178 Variation AB, except minimum lead width.

4073253-5/N 12/14

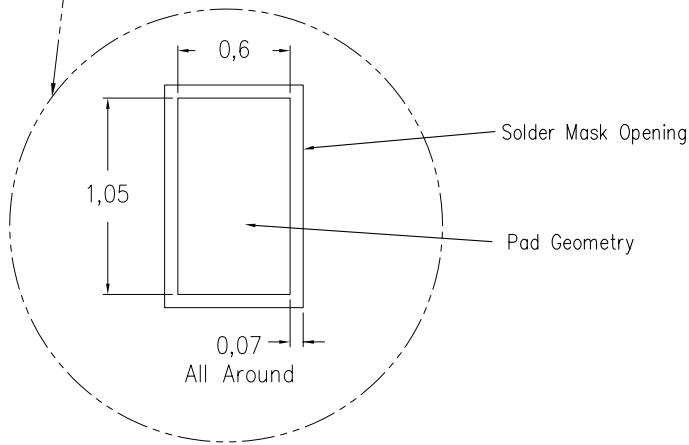
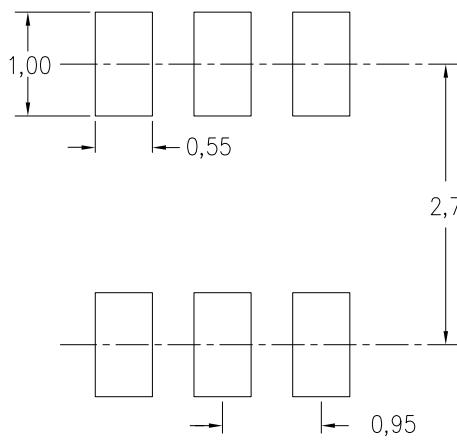
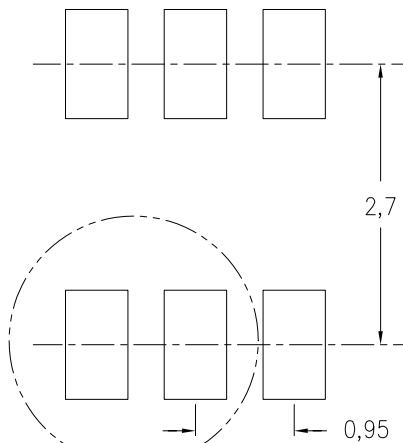
LAND PATTERN DATA

DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



4209593-4/C 08/11

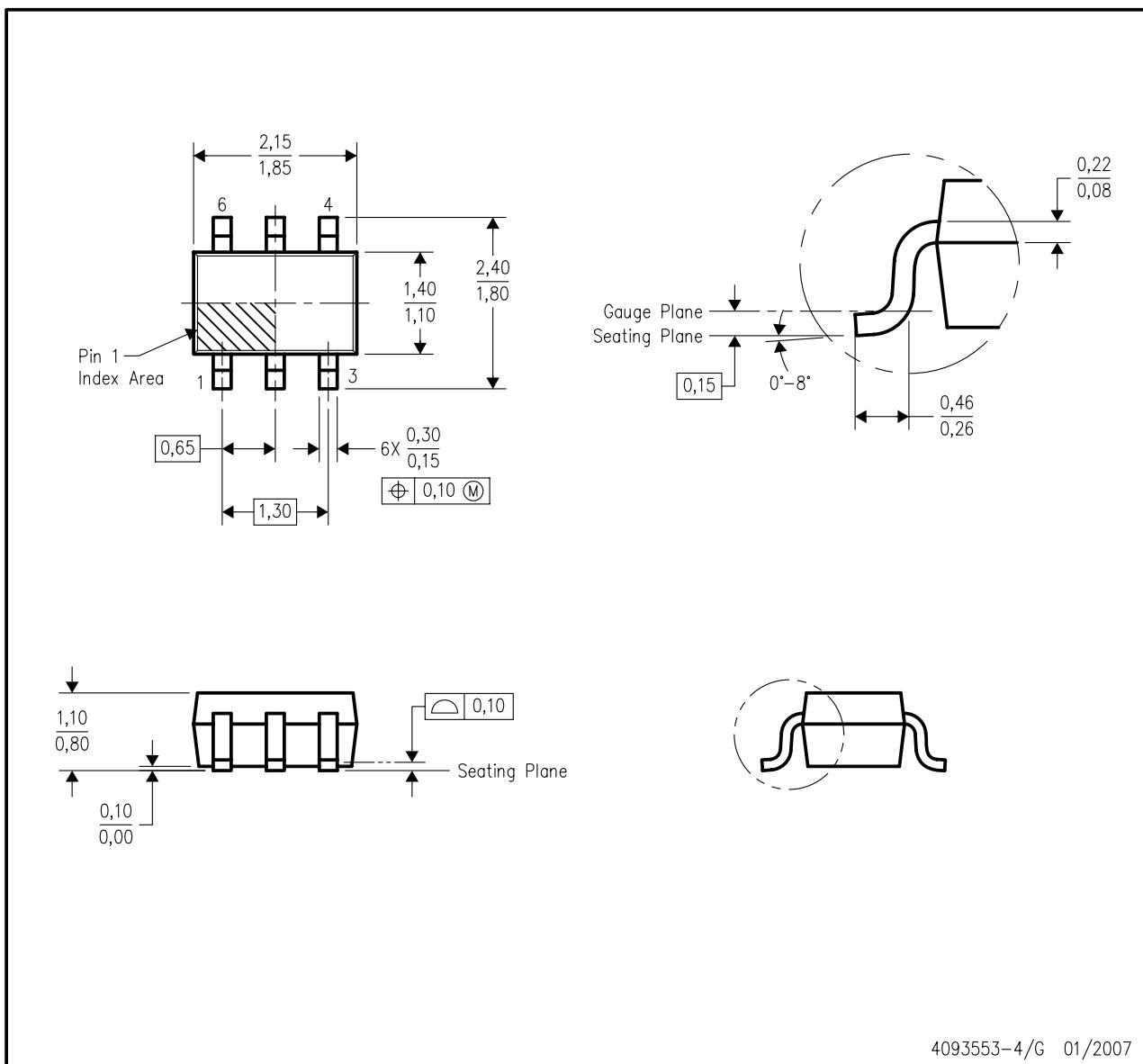
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

MECHANICAL DATA

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-4/G 01/2007

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-203 variation AB.

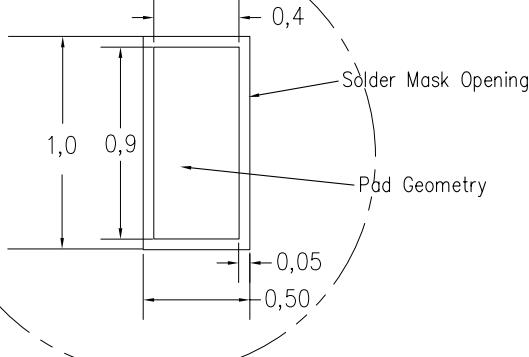
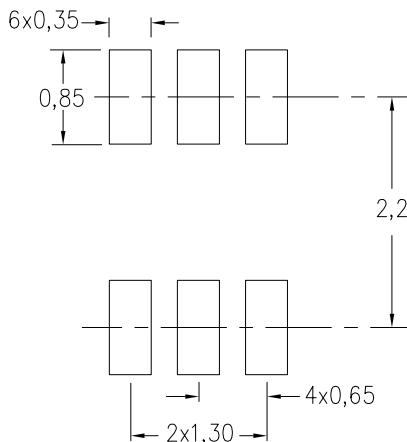
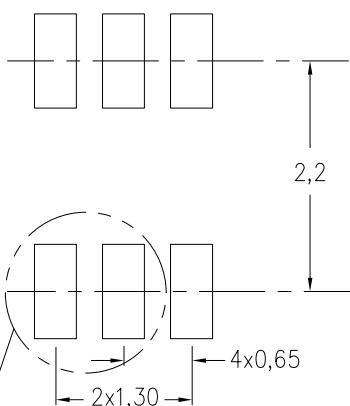
LAND PATTERN DATA

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



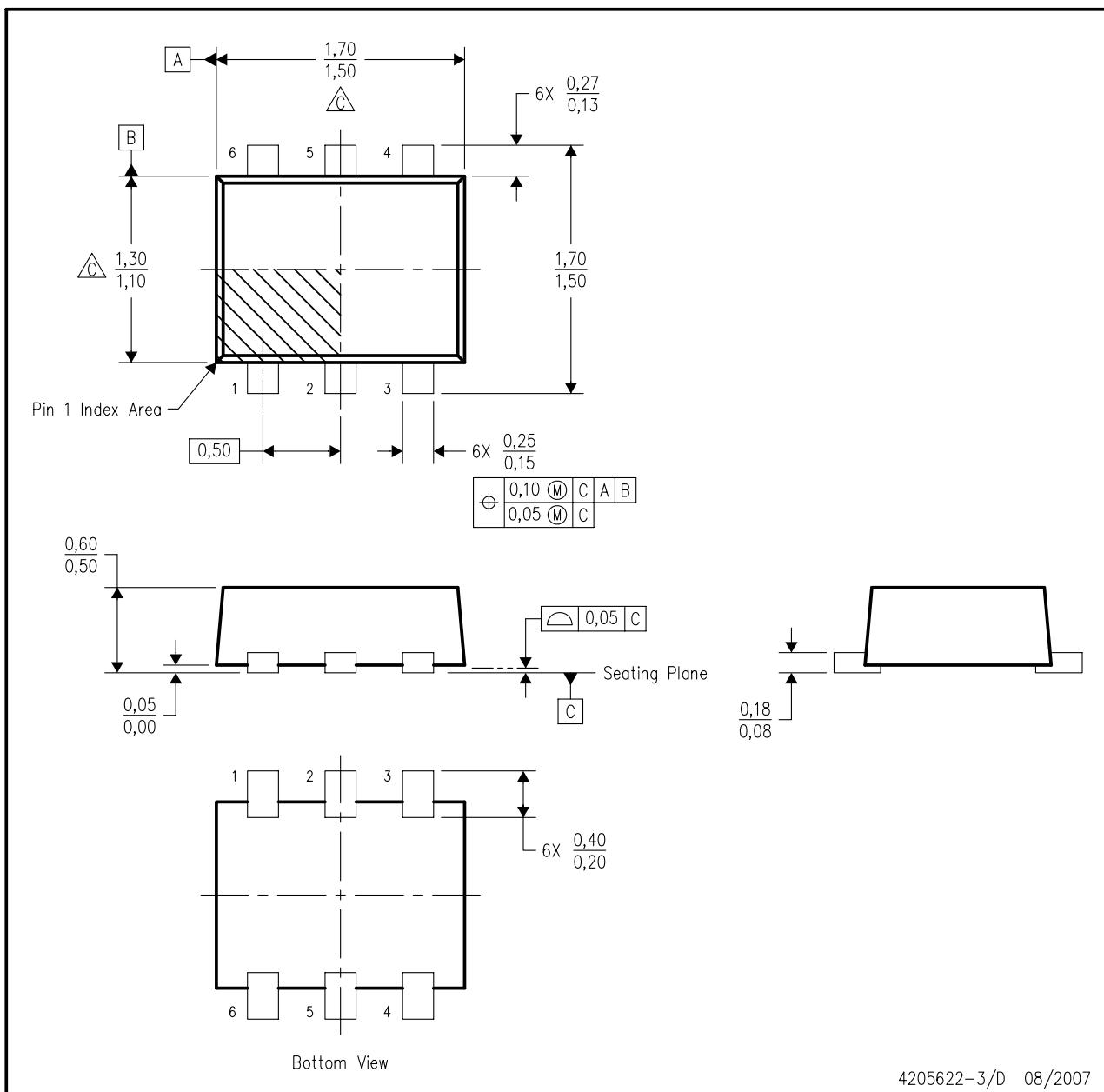
4210356-3/C 07/11

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

 Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs.

 Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 per end of the lead.

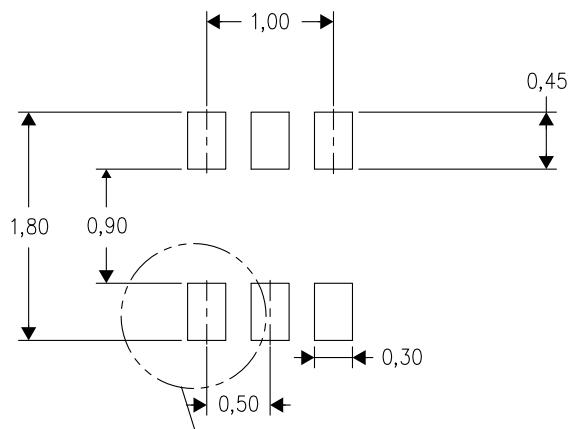
D. JEDEC package registration is pending.

D. QLBC package registration is pending.

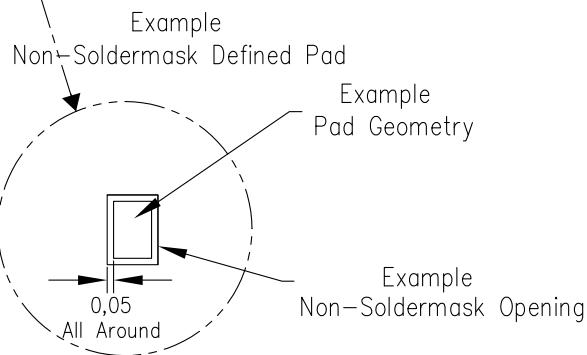
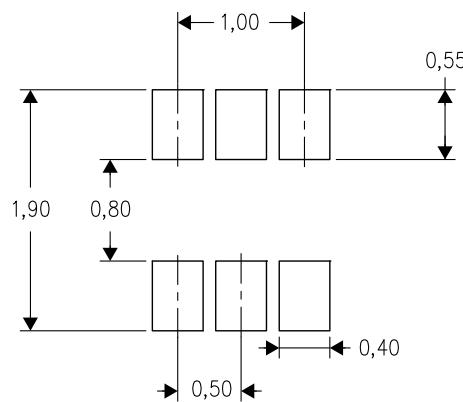
DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE

Example Board Layout



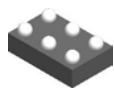
Example Stencil Design
(Note E)



4208207-3/E 06/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Side aperture dimensions over-print land for acceptable area ratio > 0.66 . Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

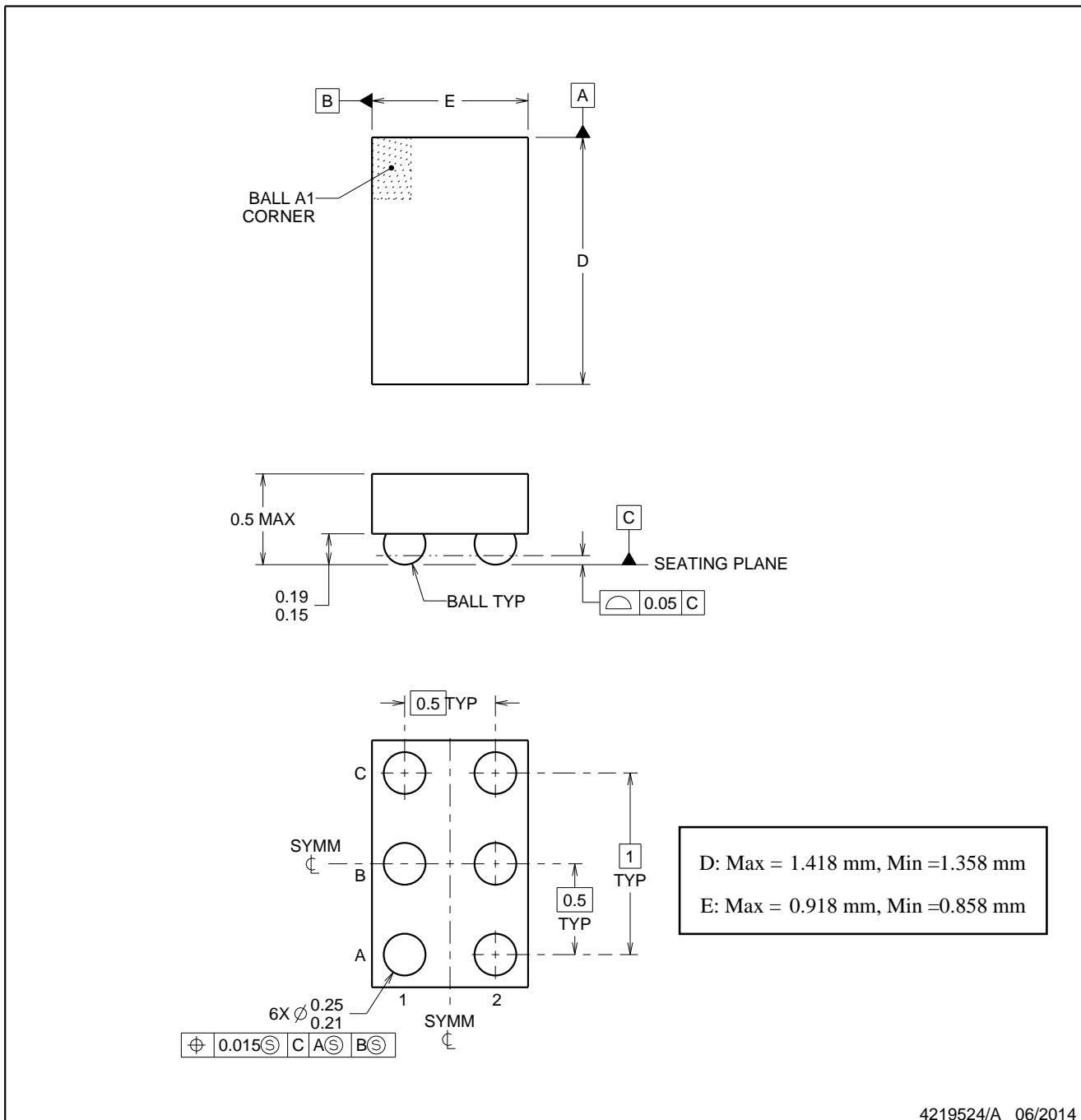


PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4219524/A 06/2014

NOTES:

NanoFree is a trademark of Texas Instruments.

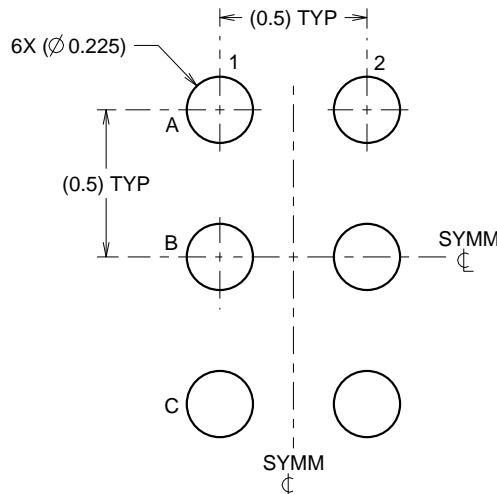
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

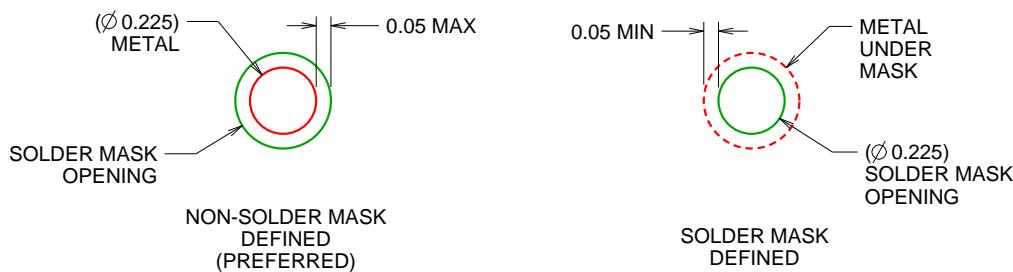
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

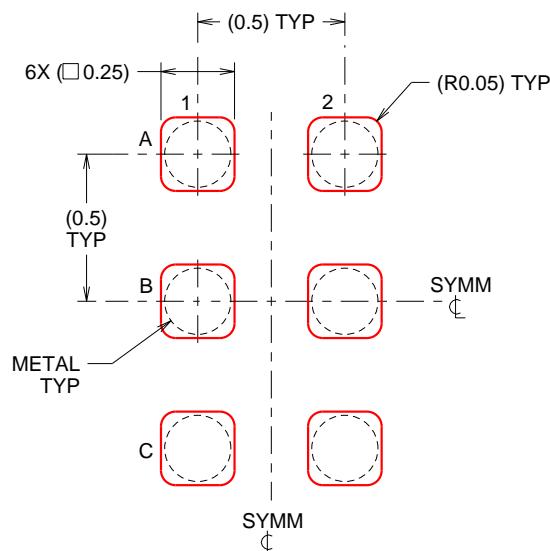
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NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN**YZP0006****DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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