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**Burr-Brown Products**  
from Texas Instruments

**PCM1727**



SBAS077A – JANUARY 1997 – REVISED MAY 2007

*SoundPLUS™* **Stereo Audio**  
**DIGITAL-TO-ANALOG CONVERTER**  
**With Programmable Dual PLL**

**FEATURES**

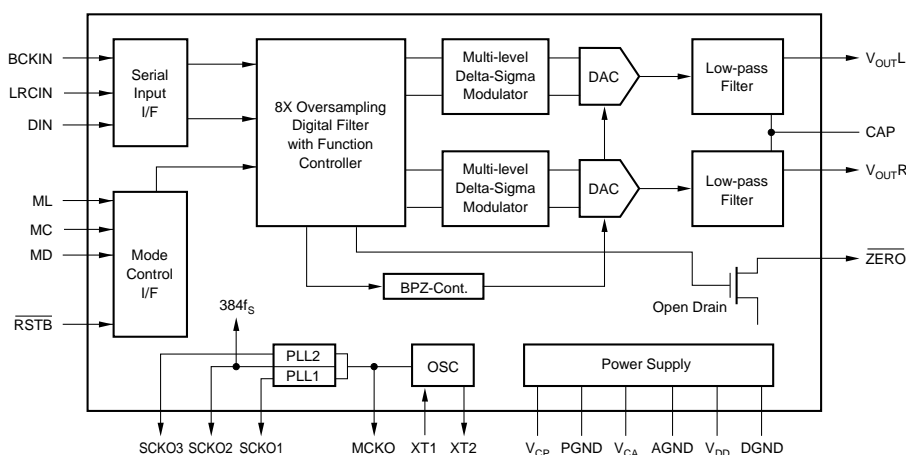
- ACCEPTS 16-, 20-, OR 24-BIT INPUT DATA
- COMPLETE STEREO DAC: Includes Digital Filter and Output Amp
- DYNAMIC RANGE: 92dB
- MULTIPLE SAMPLING FREQUENCIES:  
 $f_s = 44.1\text{kHz}, 48\text{kHz}, 96\text{kHz}$
- PROGRAMMABLE DUAL PLL CIRCUIT:  
 27MHz Master Clock Input
- GENERATED SYSTEM CLOCK  
 SCKO1: 33.8688MHz  
 SCKO2:  $384f_s$   
 SCKO3:  $768f_s$  (44.1k/48kHz)  
 $384f_s$  (96kHz)
- NORMAL OR I<sup>2</sup>S™ DATA INPUT FORMATS
- SELECTABLE FUNCTIONS:  
 Soft Mute, Analog Output Mode  
 Digital Attenuator (256 Steps)  
 Digital De-Emphasis
- +5V SINGLE POWER SUPPLY

**DESCRIPTION**

The PCM1727 is a complete, low-cost, stereo audio digital-to-analog converter (DAC) with a dual phase-locked loop (PLL) circuit included. PLL-1 derives a fixed 33.8688MHz ( $768f_s$ ,  $f_s = 44.1\text{kHz}$ ) system clock (SCKO-1), and PLL-2 derives both the  $384f_s$  ( $f_s = 44.1\text{k}/48\text{k}/96\text{kHz}$ ) system clock (SCKO-2) and the  $768f_s$  ( $f_s = 44.1\text{k}/48\text{kHz}$ )/ $384f_s$  ( $f_s = 96\text{kHz}$ ) system clock (SCKO-3) from an external 27MHz reference frequency. The DAC contains a 3rd-order Delta-Sigma ( $\Delta\Sigma$ ) modulator, a digital interpolation filter, and an analog output amplifier. The PCM1727 can accept 16-, 20-, or 24-bit input data in either normal or I<sup>2</sup>S formats.

The digital filter performs an 8X interpolation function and includes selectable features such as soft mute, digital attenuation and digital de-emphasis.

The PCM1727 is ideal for applications that combine compressed audio and video data such as DVD, DVD Audio with CD-DA compatibility, and karaoke DSP.



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## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

|   |                                   |
|---|-----------------------------------|
| Power Supply Voltage .....                            | +6.5V                             |
| +V <sub>CC</sub> to +V <sub>DD</sub> Difference ..... | ±0.1V                             |
| Input Logic Voltage .....                             | -0.3V to (V <sub>DD</sub> + 0.3V) |
| Input Current (except power supply) .....             | ±10mA                             |
| Power Dissipation .....                               | 300mW                             |
| Operating Temperature Range .....                     | -25°C to +85°C                    |
| Storage Temperature .....                             | -55°C to +125°C                   |
| Lead Temperature (soldering, 5s) .....                | +260°C                            |
| Thermal Resistance, $\theta_{JA}$ .....               | +70°C/W                           |

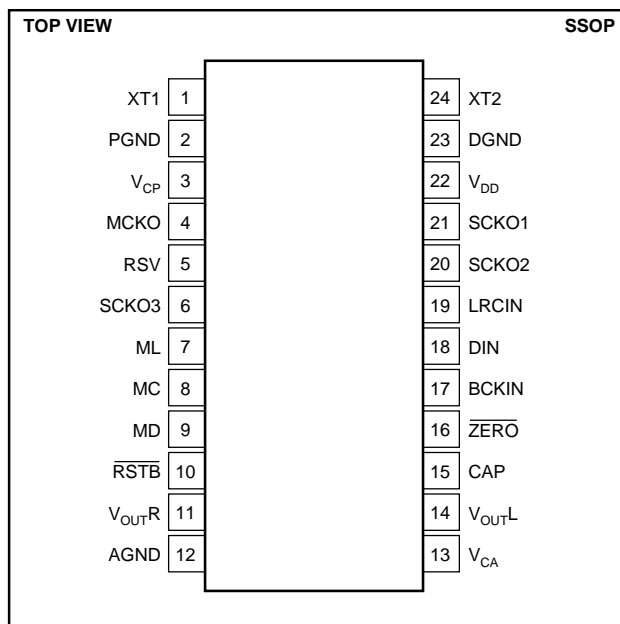
NOTE: (1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

### PACKAGE INFORMATION<sup>(1)</sup>

| PRODUCT  | PACKAGE     | PACKAGE DESIGNATOR |
|----------|-------------|--------------------|
| PCM1727E | 24-Pin SSOP | DB                 |

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

### PIN CONFIGURATION



### PIN ASSIGNMENTS

| PIN | NAME              | I/O | DESCRIPTION  |
|-----|-------------------|-----|--|
| 1   | XT1               | IN  | 27MHz Crystal or External Clock Input  |
| 2   | PGND              | —   | PLL Ground   |
| 3   | V <sub>CP</sub>   | —   | PLL Power Supply (+5V)   |
| 4   | MCKO              | OUT | Buffered Clock Output of Crystal Oscillator  |
| 5   | RSV               | —   | Reserve; This pin should be open.  |
| 6   | SCKO3             | OUT | System Clock Out 3; This output is 768f <sub>S</sub> or 384f <sub>S</sub> .  |
| 7   | ML                | IN  | Latch Enable Input for Serial Interface Mode <sup>(2)</sup>  |
| 8   | MC                | IN  | Bit Clock Input for Serial Interface Mode <sup>(2)</sup>   |
| 9   | MD                | IN  | Serial Data Input for Serial Interface Mode <sup>(2)</sup>   |
| 10  | RSTB              | IN  | Reset; When this pin is low, the DF and modulator are held in reset.   |
| 11  | V <sub>OUTR</sub> | OUT | Right Channel, Analog Voltage Output of Audio Signal   |
| 12  | AGND              | —   | Analog Ground  |
| 13  | V <sub>CA</sub>   | —   | Analog Power Supply (+5V)  |
| 14  | V <sub>OUTL</sub> | OUT | Left Channel, Analog Voltage Output of Audio Signal  |
| 15  | CAP               | —   | Common Pin of Analog Output Amp  |
| 16  | ZERO              | OUT | Zero Data Flag; This pin is low when the input data is continuously zero for more than 65,535 cycles of BCKIN <sup>(1)</sup> . |
| 17  | BCKIN             | IN  | Bit Clock Input for Serial Audio Data <sup>(3)</sup>   |
| 18  | DIN               | IN  | Serial Audio Data Input <sup>(3)</sup>   |
| 19  | LRCIN             | IN  | Left and Right Clock (sampling rate=f <sub>S</sub> ) <sup>(3)</sup>  |
| 20  | SCKO2             | OUT | System Clock Out 2; This output is 256f <sub>S</sub> or 384f <sub>S</sub> system clock.  |
| 21  | SCKO1             | OUT | System Clock Out 1; This output is 33.8688MHz system clock.  |
| 22  | V <sub>DD</sub>   | —   | Digital Power (+5V)  |
| 23  | DGND              | —   | Digital Ground   |
| 24  | XT2               | —   | 27MHz Crystal. Connected to GND at external clock.   |

NOTES: (1) Open Drain Output.  
 (2) Schmitt trigger input with internal pull-up resistors.  
 (3) Schmitt trigger input.

## ELECTRICAL CHARACTERISTICS

 All specifications at +25°C, +V<sub>CA</sub> = +V<sub>DD</sub> = +V<sub>CP</sub> = +5V, f<sub>S</sub> = 44.1kHz, and 16-bit input data, SYSCLK = 384f<sub>S</sub>, unless otherwise noted.

| PARAMETER   | CONDITIONS  | PCM1727  |  |  | UNITS   |
|---|---|--|--|--|---|
|   |   | MIN  | TYP  | MAX  |   |
| <b>RESOLUTION</b>   |   | 16   |  |  | Bits  |
| <b>DATA FORMAT</b><br>Audio Data Interface Format<br>Data Bit Length<br>Audio Data Format<br>Sampling Frequency (f <sub>S</sub> )   |   | Standard/I <sup>2</sup> S Selectable<br>16/20/24 Selectable<br>MSB First, 2's Comp |  |  |   |
|   |   | 44.1   |  | 96   | kHz   |
| <b>PLL PERFORMANCE</b><br>Master Clock Input Frequency <sup>(4)</sup><br>Generated System Clock<br>SCKO-1<br>SCKO-2<br>SCKO-3<br>Output Logic Level V <sub>OH</sub><br>(MCKO, SCKO 1 ~ 3) V <sub>OL</sub><br>Generated SYSCLK Jitter<br>Generated SYSCLK Transient <sup>(1)</sup><br>Power-Up Time<br>Generated SYSCLK Duty Cycle | 768f <sub>S</sub> (f <sub>S</sub> = 44.1k)<br>384f <sub>S</sub><br>768f <sub>S</sub> (f <sub>S</sub> = 44.1k/48k), 384f <sub>S</sub> (f <sub>S</sub> = 96k)<br>I <sub>OH</sub> = 2mA<br>I <sub>OL</sub> = 4mA<br>Standard Dev<br>f <sub>M</sub> = 27MHz<br>To Programmed Frequency<br>f <sub>M</sub> = 27MHz, C <sub>L</sub> = 15pF | 26.73<br><br>16.9344<br>33.8688<br>V <sub>DD</sub> - 0.4<br><br><br>40             | 27<br>33.8688<br><br>±150<br>15<br>50                  | 27.27<br><br>36.8640<br>36.8640<br>0.5<br>20<br>30<br>60 | MHz<br>MHz<br>MHz<br>VDC<br>VDC<br>ps<br>ms<br>ms<br>%    |
| <b>DIGITAL INPUT LOGIC LEVEL</b>  |   |  | TTL  |  |   |
| <b>DYNAMIC PERFORMANCE<sup>(2)</sup></b><br>THD+N at f <sub>S</sub> (0dB)<br>THD+N at -60dB<br>Dynamic Range (EIAJ Method)<br>Signal-to-Noise Ratio <sup>(3)</sup> (EIAJ Method)<br>Channel Separation  | f <sub>S</sub> = 44.1kHz<br>f <sub>S</sub> = 96kHz<br>f <sub>S</sub> = 44.1kHz<br>f <sub>S</sub> = 96kHz<br>f <sub>S</sub> = 44.1kHz<br>f <sub>S</sub> = 96kHz<br>f <sub>S</sub> = 44.1kHz<br>f <sub>S</sub> = 96kHz<br>f <sub>S</sub> = 44.1kHz  | 90<br><br>90<br><br>88   | -89<br>-87<br>-31<br>-29<br>92<br>90<br>94<br>90<br>93 | -80<br><br><br><br><br><br><br><br><br><br>              | dB<br>dB<br>dB<br>dB<br>dB<br>dB<br>dB<br>dB<br>dB        |
| <b>DC ACCURACY</b><br>Gain Error<br>Gain Mismatch, Channel-to-Channel<br>Bipolar Zero Error   | V <sub>OUT</sub> = V <sub>CC</sub> /2 at BPZ  |  | ±1.0<br>±1.0<br>±30                                    | ±3.0<br>±2.0   | % of FSR<br>% of FSR<br>mV                                |
| <b>ANALOG OUTPUT</b><br>Output Voltage<br>Center Voltage<br>Load Impedance  | Full Scale (-0dB)<br>AC Load  | 5  | 0.62 x V <sub>CA</sub><br>V <sub>CA</sub> /2           |  | V <sub>PP</sub><br>V <sub>DC</sub><br>kΩ                  |
| <b>DIGITAL FILTER PERFORMANCE</b><br>Passband<br>Stop Band<br>Passband Ripple<br>Stop Band Attenuation<br>Delay Time<br>De-emphasis Error   |   | 0.555<br><br>-35<br><br>-0.2   | <br><br><br>11.125/f <sub>S</sub>                      | 0.445<br><br>±0.17<br><br>+0.55                          | f <sub>S</sub><br>f <sub>S</sub><br>dB<br>dB<br>sec<br>dB |
| <b>INTERNAL ANALOG FILTER</b><br>-3dB Bandwidth<br>Passband Response  | f = 20kHz   |  | 100<br>-0.16   |  | kHz<br>dB   |
| <b>POWER SUPPLY REQUIREMENTS</b><br>Voltage Range<br>Supply Current: I <sub>CC</sub> + I <sub>DD</sub> + I <sub>CP</sub>  | V <sub>CC</sub> = V <sub>DD</sub> = V <sub>CP</sub><br>f <sub>S</sub> = 44.1kHz   | 4.5  | 5<br>25  | 5.5<br>27  | VDC<br>mA   |
| <b>TEMPERATURE RANGE</b><br>Operating<br>Storage  |   | -25<br>-55   |  | +85<br>+125  | °C<br>°C  |

NOTES: (1) Sysclk transient is the maximum frequency lock time when the PLL frequency is changed.

(2) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode.

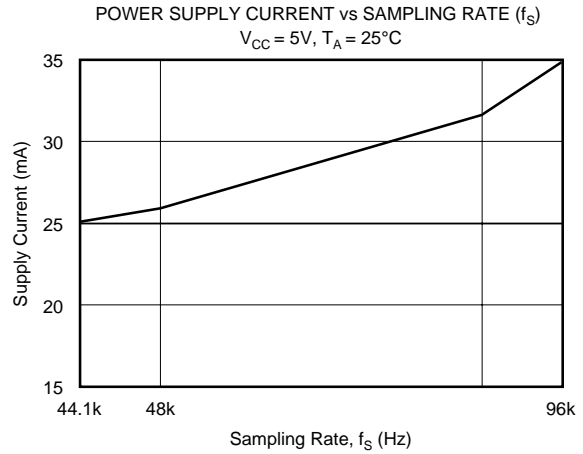
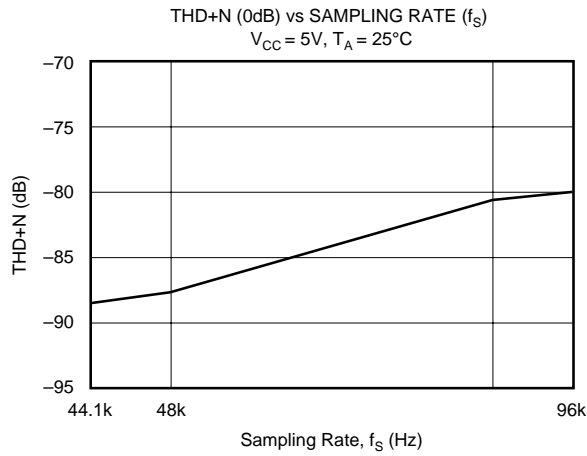
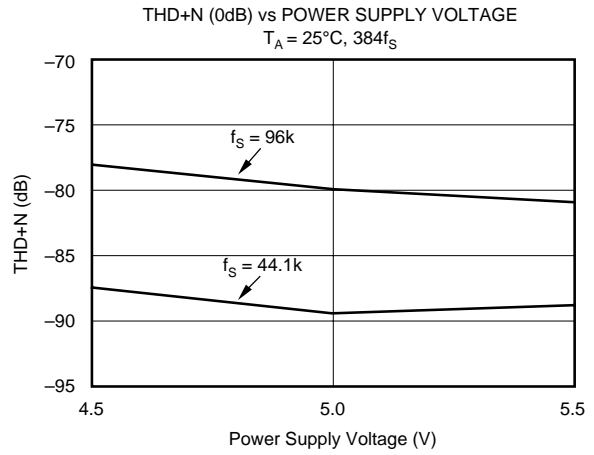
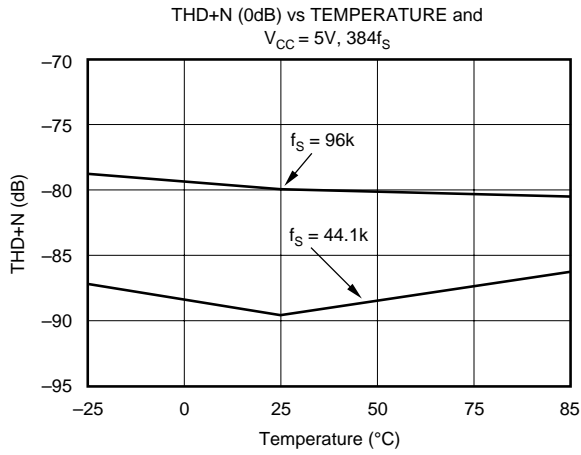
(3) SNR is tested at Infinite Zero Detection off.

(4) PLL evaluations tested with 1ns maximum jitter on the 27MHz input clock.

## TYPICAL CHARACTERISTICS

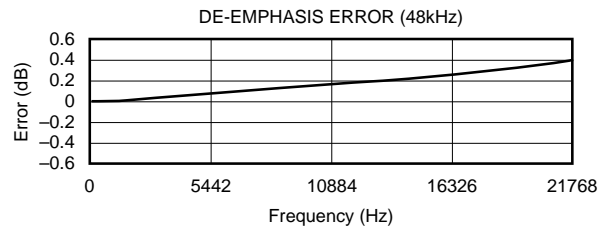
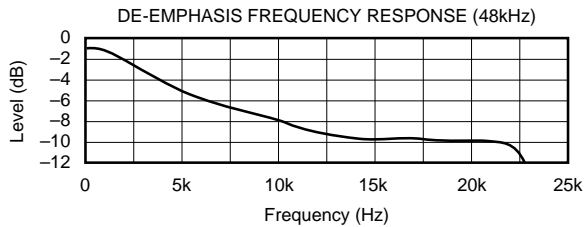
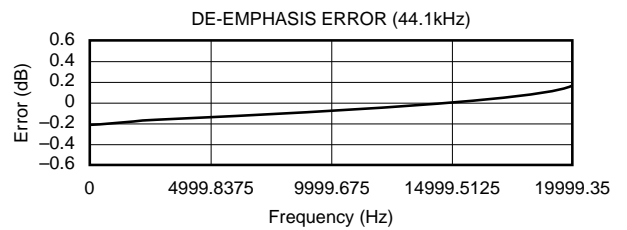
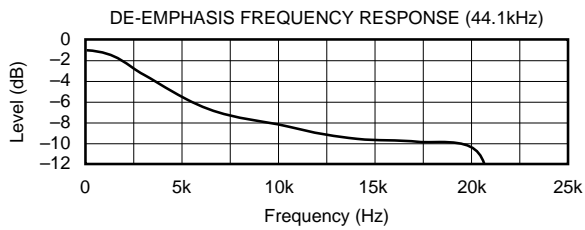
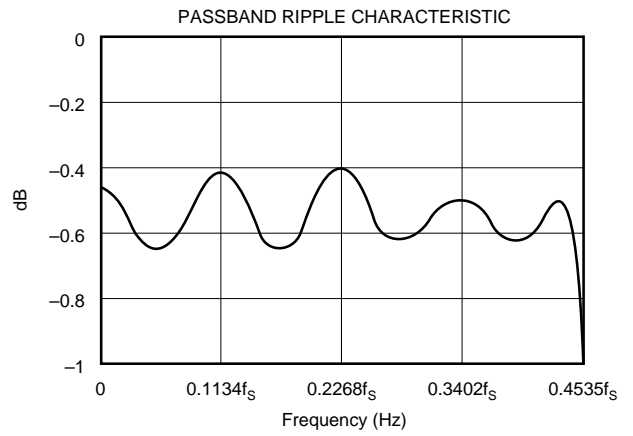
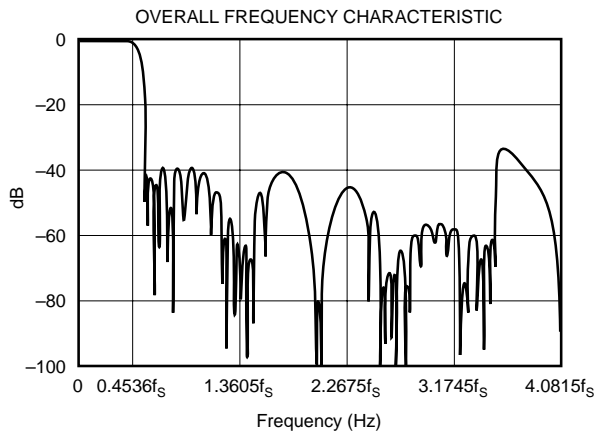
At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = V_{DD} = V_{CP} = +5\text{V}$ ,  $f_S = 44.1\text{kHz}$ , 16-bit input data,  $384f_S$ , unless otherwise noted. Measurement bandwidth is 20kHz.

### DYNAMIC PERFORMANCE



## TYPICAL CHARACTERISTICS (Cont.)

### DIGITAL FILTER



**TYPICAL CONNECTION DIAGRAM**

Figure 1 illustrates the typical connection diagram for the PCM1727 in a DVD Audio application. The 27MHz master video clock ( $f_M$ ) drives XT1 (pin 1) of the PCM1727. A programmable system clock is generated by the PCM1727 PLL, with SCKO2 used to drive the MPEG2 decoder system clock input, SCKO1 used to drive the CD-DA DSP system clock input, and SCKO3 used to drive Karaoke DSP system clock input. The standard audio signals (data, bit clock, and word clock) are generated in the decoder from the PCM1727 system clock, providing synchronization of audio and video signals.

**DUAL PLL CIRCUIT**

The PCM1727 has a programmable internal DUAL PLL circuit, as shown in Figure 2. The PLL is designed to accept a 27MHz master clock or crystal oscillator and generate all internal system clocks required to operate the digital filter and  $\Delta\Sigma$  modulator, at  $384f_s$ . If an external master clock is used, XT2 must be connected to ground. In both cases, the signal amplitude on XT1 must satisfy the specification described in Figure 3. Therefore, careful C1 and C2 determination is required to keep this specification satisfied when using a crystal oscillator. The PLL will directly track any variations in the master clock frequency, and jitter on the

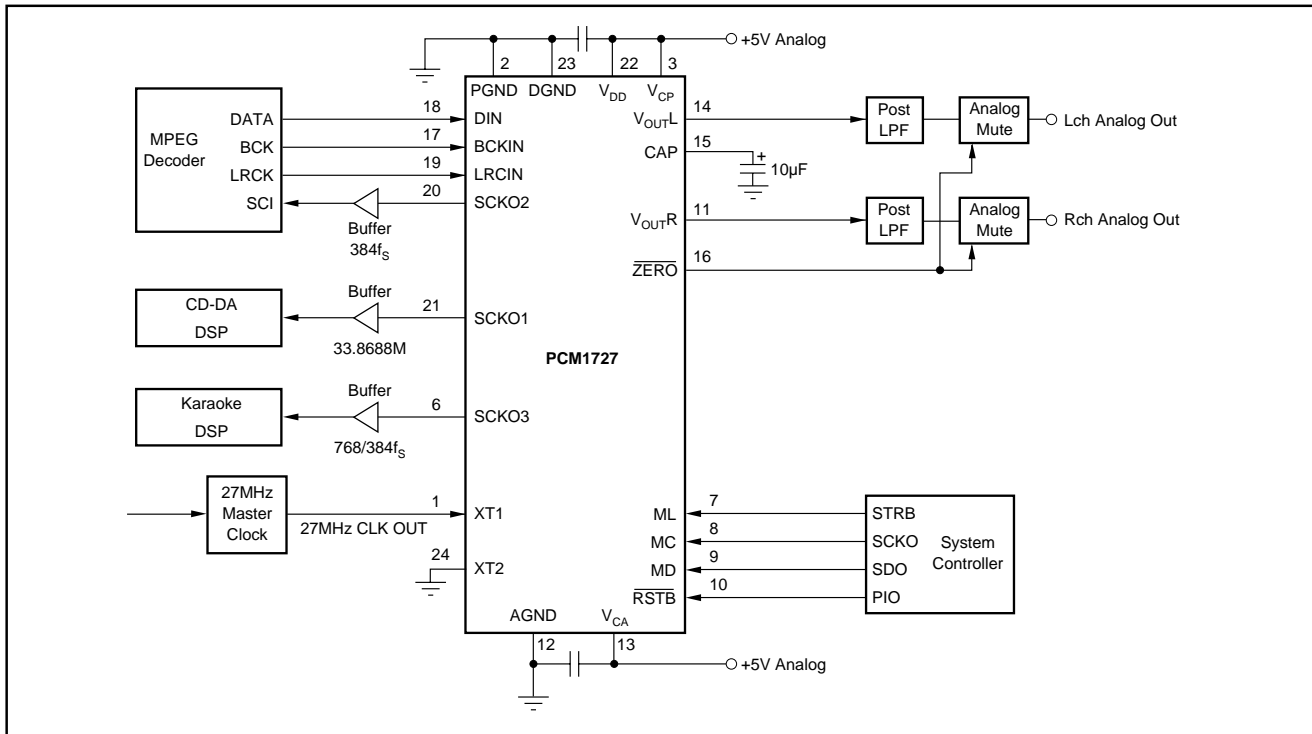


FIGURE 1. Connection Diagram for External Master Clock in a Typical MPEG2 Application.

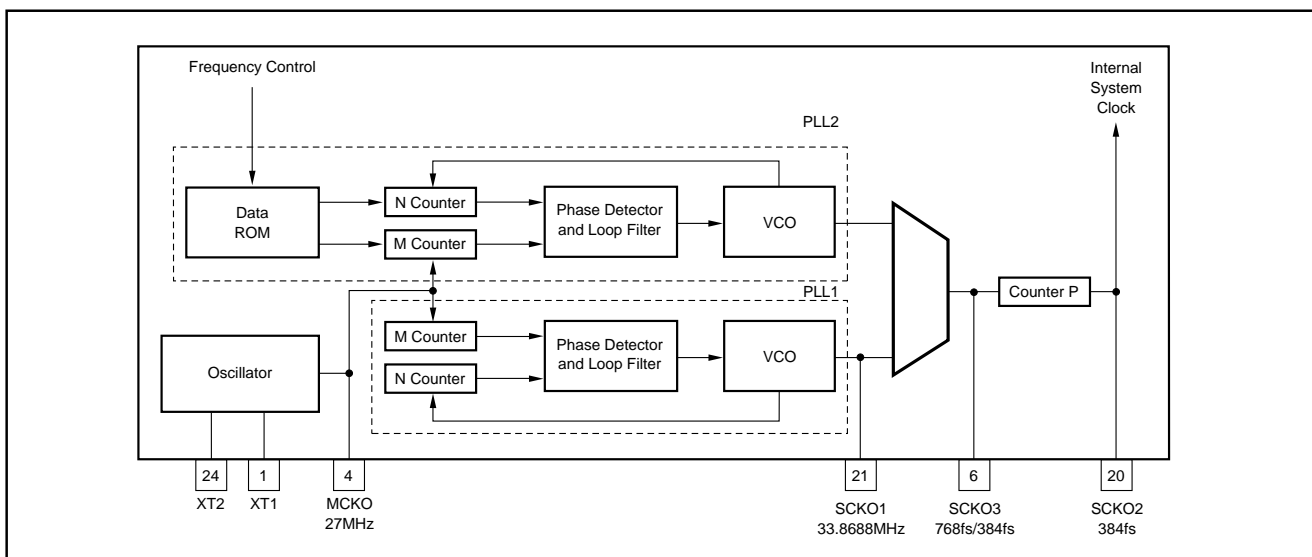


FIGURE 2. PLL Block Diagram.

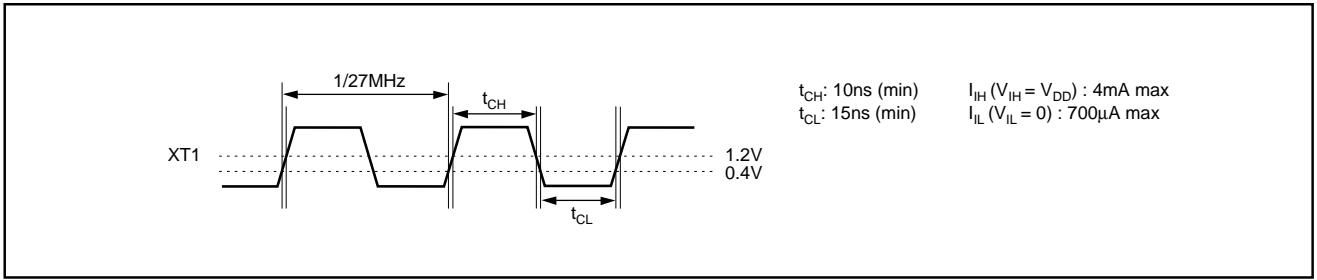


FIGURE 3. XT1 Input Timing.

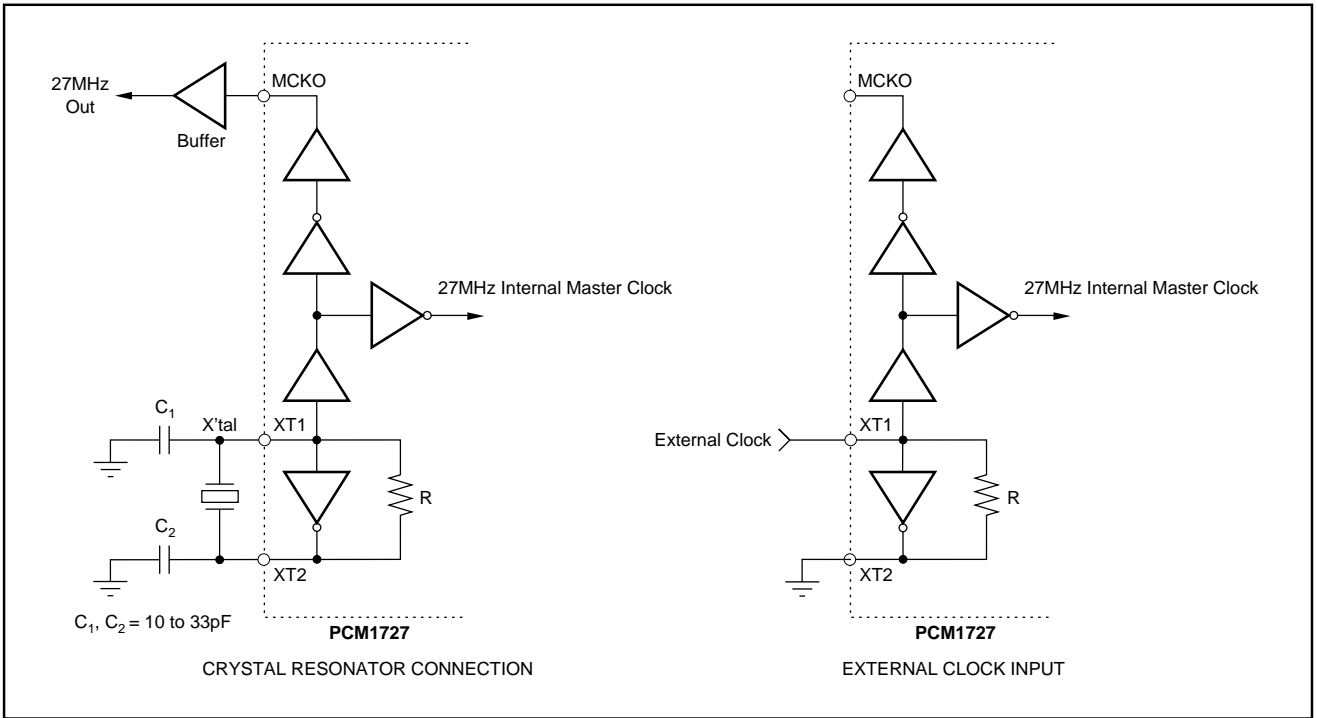


FIGURE 4. System Clock Connection.

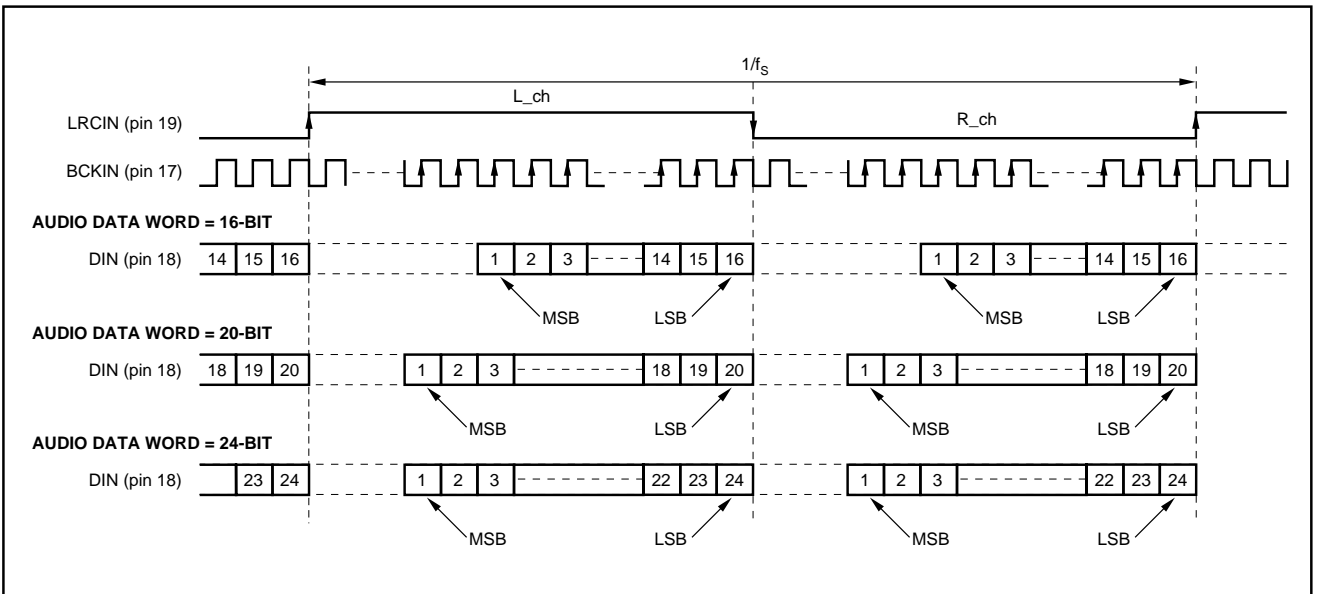


FIGURE 5. Normal Data Input Timing.



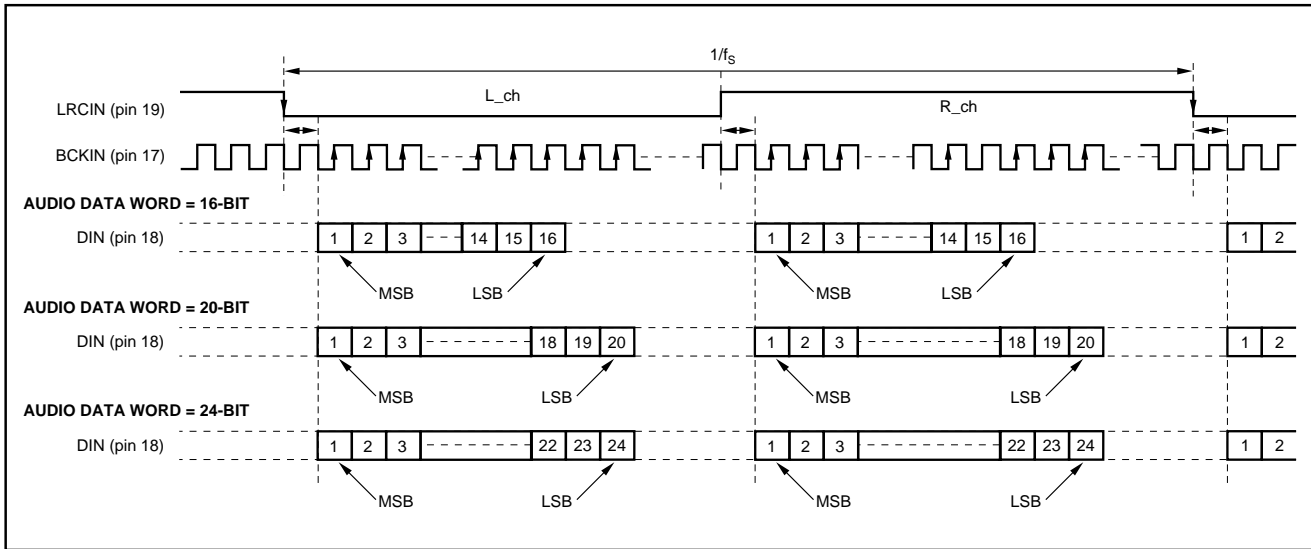


FIGURE 6. I<sup>2</sup>S Data Input Timing.

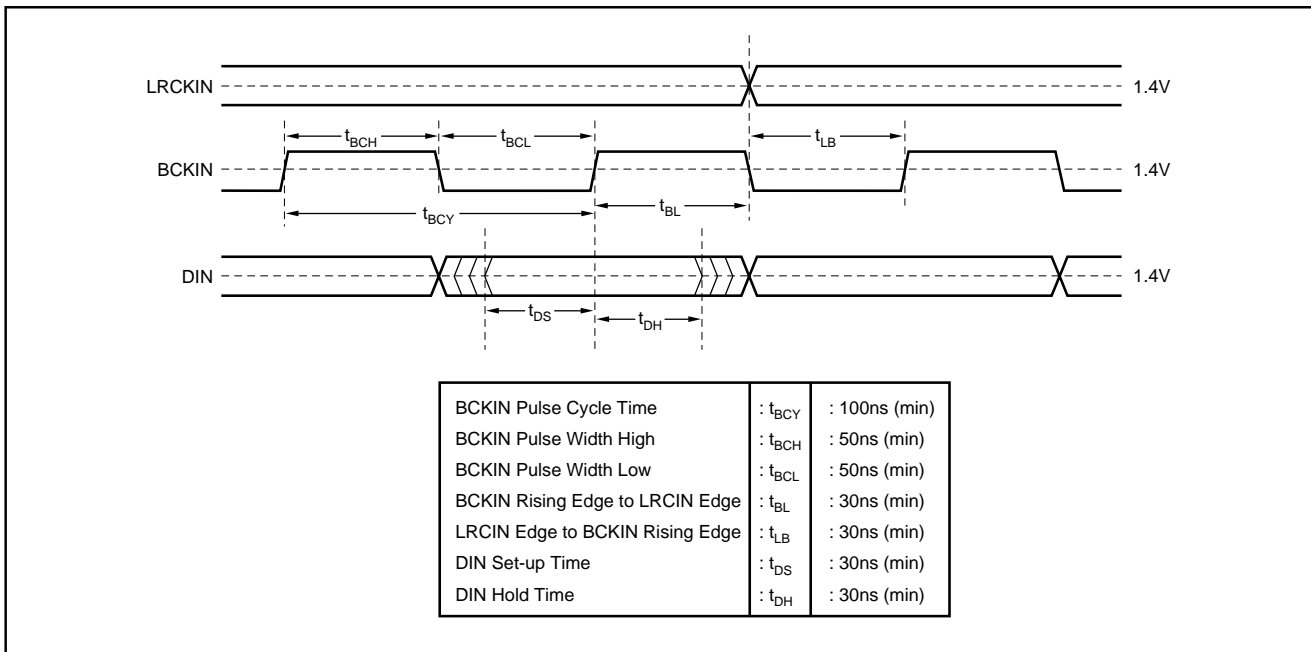


FIGURE 7. Audio Data Input Timing.

system clock is specified at 150ps typical. Figure 3 illustrates the timing requirements for the 27MHz master clock. Figure 4 illustrates the system clock connections for an external clock or crystal oscillator.

The PCM1727 internal PLL can be programmed for three different sampling frequencies (LRCIN), as shown in Table I. The internal sampling clocks generated by the various programmed frequencies are shown in Table II. The system clock output frequency for PCM1727 is 100% accurate.

To provide MCKO clock and SCKO1, SCKO2, SCKO3 clocks for external circuits, an external buffer may be used to avoid degrading audio performance (as shown in the connection diagram, in Figure 1).

|                                  | Sampling Frequencies-LRCIN (kHz) |    |
|----------------------------------|----------------------------------|----|
| Standard Sampling Freq           | 44.1                             | 48 |
| Double of Standard Sampling Freq |                                  | 96 |

TABLE I. Sampling Frequencies.

| Sampling Frequency (LRCIN) |          | SCKO2 System Clock | SCKO3 System Clock |
|----------------------------|----------|--------------------|--------------------|
| 44.1kHz                    | Standard | 16.9344MHz         | 33.8688MHz         |
| 48kHz                      | Standard | 18.4320MHz         | 36.8640MHz         |
| 96kHz                      | Double   | 36.8640MHz         | 36.8640MHz         |

TABLE II. Sampling Frequencies vs Internal System Clock (= Output Frequencies of Dual PLL).

## MAPPING OF PROGRAM REGISTERS

|       | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8  | B7  | B6  | B5   | B4   | B3  | B2  | B1  | B0               |
|-------|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|------|------|-----|-----|-----|------------------|
| MODE0 | res | res | res | res | res | A1  | A0 | LDL | AL7 | AL6 | AL5  | AL4  | AL3 | AL2 | AL1 | AL0              |
| MODE1 | res | res | res | res | res | A1  | A0 | LDR | AR7 | AR6 | AR5  | AR4  | AR3 | AR2 | AR1 | AR0              |
| MODE2 | res | res | res | res | res | A1  | A0 | PL3 | PL2 | PL1 | PL0  | IW1  | IW0 | OPE | DEM | MUT              |
| MODE3 | res | res | res | res | res | A1  | A0 | IZD | SF1 | SF0 | DSR1 | DSR0 | res | ATC | LRP | I <sup>2</sup> S |

## SPECIAL FUNCTIONS

The PCM1727 includes several special functions, including digital attenuation, digital de-emphasis, soft mute, data format selection and input word resolution. These functions are controlled using a three-wire interface. MD (pin 9) is used for the program data, MC (pin 8) is used to clock in the program data, and ML (pin 7) is used to latch in the program data. Table III lists the selectable special functions.

| FUNCTION   | DEFAULT MODE                          |
|--|---------------------------------------|
| Input Audio Data Format Selection<br>Normal Format<br>I <sup>2</sup> S Format  | Normal Format                         |
| Input Audio Data Bit Selection<br>16/20/24 Bits  | 16 Bits                               |
| Input LRCIN Polarity Selection<br>Lch/Rch = High/Low<br>Lch/Rch = Low/High   | Lch/Rch = High/Low                    |
| De-emphasis Control  | OFF                                   |
| Soft Mute Control  | OFF                                   |
| Attenuation Control<br>Lch, Rch Individually<br>Lch, Rch Common  | 0dB<br>Lch, Rch Individually Fixed    |
| Infinite Zero Detection Circuit Control  | OFF                                   |
| Operation Enable (OPE)   | Enabled                               |
| Sampling Rate Selection<br>Standard Sampling Rate—44.1/48kHz<br>Double Sampling Rate—96kHz<br>Sampling Frequency<br>44.1kHz Group<br>48kHz Group | Standard Sampling Rate<br><br>44.1kHz |
| Analog Output Mode<br>L, R, Mono, Mute   | Stereo                                |

TABLE III. Selectable Functions.

## PROGRAM REGISTER BIT MAPPING

The PCM1727 special functions are controlled using four program registers which are 16 bits long. These registers are all loaded using MD. After the 16 data bits are clocked in, ML is used to latch in the data to the appropriate register. Table IV shows the complete mapping of the four registers and Figure 8 illustrates the serial interface timing.

| REGISTER NAME | BIT NAME   | DESCRIPTION  |
|---------------|--|--|
| Register 0    | AL (7:0)<br>LDL<br>A (1:0)<br>res  | DAC Attenuation Data for Lch<br>Attenuation Data Load Control for Lch<br>Register Address<br>Reserved, should be "L"   |
| Register 1    | AR (7:0)<br>LDL<br>A (1:0)<br>res  | DAC Attenuation Data for Rch<br>Attenuation Data Load Control for Rch<br>Register Address<br>Reserved, should be "L"   |
| Register 2    | MUT<br>DEM<br>OPE<br>IW (1:0)<br>PL (3:0)<br>A (1:0)<br>res                      | Left and Right DACs Soft Mute Control<br>De-emphasis Control<br>Left and Right DACs Operation Control<br>Input Audio Data Bit Select<br>Output Mode Select<br>Register Address<br>Reserved, should be "L"                            |
| Register 3    | I <sup>2</sup> S<br>LRP<br>ATC<br>DSR (1:0)<br>SF (1:0)<br>IZD<br>A (1:0)<br>res | Audio Data Format Select<br>Polarity of LRCIN (pin 19) Select<br>Attenuator Control<br>Double Sampling Rate Select<br>Sampling Rate Select<br>Infinite Zero Detection Circuit Control<br>Register Address<br>Reserved, should be "L" |

TABLE IV. Internal Register Mapping.

## REGISTER 0 (A1 = 0, A0 = 0)

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8  | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0  |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| res | res | res | res | res | A1  | A0 | LDL | AL7 | AL6 | AL5 | AL4 | AL3 | AL2 | AL1 | AL0 |

Register 0 is used to control left channel attenuation. Bits 0 - 7 (AL0 - AL7) are used to determine the attenuation level. The level of attenuation is given by:

$$ATT = [20 \log_{10} (ATT\_DATA/255)] \text{ dB}$$

## ATTENUATION DATA LOAD CONTROL

Bit 8 (LDL) is used to control the loading of attenuation data in B0:B7. When LDL is set to 0, attenuation data will be loaded into AL0:AL7, but it will not affect the attenuation level until LDL is set to 1. LDR in Register 1 has the same function for right channel attenuation.

Attenuation Level (ATT) can be controlled as following Resistor set AL (R) (7:0).

| AL (R) (7:0) | ATT LEVEL   |
|--------------|-------------|
| 00h          | -∞dB (Mute) |
| 01h          | -48.16dB    |
| .            | .           |
| .            | .           |
| .            | .           |
| FEh          | -0.07dB     |
| FFh          | 0dB         |

### REGISTER 1 (A1 = 0, A0 = 1)

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8  | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0  |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| res | res | res | res | res | A1  | A0 | LDR | AR7 | AR6 | AR5 | AR4 | AR3 | AR2 | AR1 | AR0 |

Register 1 is used to control right channel attenuation. As in Register 1, bits 0 - 7 (AR0 - AR7) control the level of attenuation.

### REGISTER 2 (A1 = 1, A0 = 0)

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8  | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0   |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| res | res | res | res | res | A1  | A0 | PL3 | PL2 | PL1 | PL0 | IW1 | IW0 | OPE | DEM | MUTE |

Register 2 is used to control soft mute, de-emphasis, operation enable, input resolution, and output format. Bit 0 is used for soft mute: a HIGH level on bit 0 will cause the output to be muted (this is ramped down in the digital domain, so no *click* is audible). Bit 1 is used to control de-emphasis. A LOW level on bit 1 disables de-emphasis, while a HIGH level enables de-emphasis.

Bit 2, (OPE) is used for operational control. Table V illustrates the features controlled by OPE.

|         | DATA INPUT | DAC OUTPUT                   | SOFTWARE MODE INPUT |
|---------|------------|------------------------------|---------------------|
| OPE = 1 | Zero       | Forced to BPZ <sup>(1)</sup> | Enabled             |
|         | Other      | Forced to BPZ <sup>(1)</sup> | Enabled             |
| OPE = 0 | Zero       | Controlled by IZD            | Enabled             |
|         | Other      | Normal                       | Enabled             |

TABLE V. Operation Enable (OPE) Function.

OPE controls the operation of the DAC: when OPE is LOW, the DAC will convert all non-zero input data. If the input data is continuously zero for 65, 536 cycles of BCKIN, the output will be forced to zero only if IZD is HIGH. When OPE is HIGH, the output of the DAC will be forced to bipolar zero, irrespective of any input data.

|         | DATA INPUT | DAC OUTPUT                   |
|---------|------------|------------------------------|
| IZD = 1 | Zero       | Forced to BPZ <sup>(1)</sup> |
|         | Other      | Normal                       |
| IZD = 0 | Zero       | Zero <sup>(2)</sup>          |
|         | Other      | Normal                       |

TABLE VI. Infinite Zero Detection (IZD) Function.

|             | DATA INPUT | DAC OUTPUT                   | SOFTWARE MODE INPUT |
|-------------|------------|------------------------------|---------------------|
| RSTB = HIGH | Zero       | Controlled by OPE and IZD    | Enabled             |
|             | Other      | Controlled by OPE and IZD    | Enabled             |
| RSTB = LOW  | Zero       | Forced to BPZ <sup>(1)</sup> | Disabled            |
|             | Other      | Forced to BPZ <sup>(1)</sup> | Disabled            |

TABLE VII. Reset (RSTB) Function.

NOTE: (1)  $\Delta\Sigma$  is disconnected from output amplifier. (2)  $\Delta\Sigma$  is connected to output amplifier.

Bits 3 (IW0) and 4 (IW1) are used to determine input word resolution. PCM1727 can be set up for input word resolutions of 16, 20, or 24 bits:

| Bit 4 (IW1) | Bit 3 (IW0) | Input Resolution |
|-------------|-------------|------------------|
| 0           | 0           | 16-bit Data Word |
| 0           | 1           | 20-bit Data Word |
| 1           | 0           | 24-bit Data Word |
| 1           | 1           | Reserved         |

Bits 5, 6, 7, and 8 (PL0:3) are used to control output format. The output of PCM1727 can be programmed for 16 different states, as shown in Table VIII.

| PL0 | PL1 | PL2 | PL3 | Lch OUTPUT | Rch OUTPUT | NOTE    |
|-----|-----|-----|-----|------------|------------|---------|
| 0   | 0   | 0   | 0   | MUTE       | MUTE       | MUTE    |
| 0   | 0   | 0   | 1   | MUTE       | R          |         |
| 0   | 0   | 1   | 0   | MUTE       | L          |         |
| 0   | 0   | 1   | 1   | MUTE       | (L + R)/2  |         |
| 0   | 1   | 0   | 0   | R          | MUTE       |         |
| 0   | 1   | 0   | 1   | R          | R          |         |
| 0   | 1   | 1   | 0   | R          | L          | REVERSE |
| 0   | 1   | 1   | 1   | R          | (L + R)/2  |         |
| 1   | 0   | 0   | 0   | L          | MUTE       |         |
| 1   | 0   | 0   | 1   | L          | R          | STEREO  |
| 1   | 0   | 1   | 0   | L          | L          |         |
| 1   | 0   | 1   | 1   | L          | (L + R)/2  |         |
| 1   | 1   | 0   | 0   | (L + R)/2  | MUTE       |         |
| 1   | 1   | 0   | 1   | (L + R)/2  | R          |         |
| 1   | 1   | 1   | 0   | (L + R)/2  | L          |         |
| 1   | 1   | 1   | 1   | (L + R)/2  | (L + R)/2  | MONO    |

TABLE VIII. Programmable Output Format.

### REGISTER 3 (A1 = 1, A0 = 1)

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8  | B7  | B6  | B5   | B4   | B3  | B2  | B1  | B0               |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|------|------|-----|-----|-----|------------------|
| res | res | res | res | res | A1  | A0 | IZD | SF1 | SF0 | DSR1 | DSR0 | res | ATC | LRP | I <sup>2</sup> S |

Register 3 is used to control input data format and polarity, attenuation channel control, system clock frequency, sampling frequency and infinite zero detection.

Bits 0 (I<sup>2</sup>S) and 1 (LRP) are used to control the input data format. A LOW on bit 0 sets the format to *Normal* (MSB-first, right-justified Japanese format) and a HIGH sets the format to I<sup>2</sup>S (Philips serial data protocol). Bit 1 (LRP) is used to select the polarity of LRCIN (sample rate clock). When bit 1 is LOW, left channel data are assumed when

LRCIN is in a HIGH phase and right channel data are assumed when LRCIN is in a LOW phase. When bit 1 is HIGH, the polarity assumption is reversed.

Bit 2 (ATC) is used for controlling the attenuator. When bit 2 is HIGH, the attenuation data loaded in program Register 0 are used for both left and right channels. When bit 2 is LOW, the attenuation data for each register are applied separately to left and right channels.

Bits 4 (DSR0) and 5 (DSR1) are used to control multiples of the sampling rate:

| DSR1 | DSR0 | Multiple |            |
|------|------|----------|------------|
| 0    | 0    | Normal   | 44.1/48kHz |
| 0    | 1    | Double   | 96kHz      |
| 1    | 0    | Reserved | Reserved   |
| 1    | 1    | Reserved | Reserved   |

Bits 6 (SF0) and 7 (SF1) are used to select the sampling frequency. Frequency selection must be made with an interval time greater than 20µs.

| SF1 | SF0 | Sampling Frequency |          |
|-----|-----|--------------------|----------|
| 0   | 0   | 44.1kHz group      | 44.1kHz  |
| 0   | 1   | 48kHz group        | 48/96kHz |
| 1   | 0   | Reserved           | Reserved |
| 1   | 1   | Reserved           | Reserved |

Bit 8 is used to control the infinite zero detection function (IZD).

When IZD is LOW, the zero detect circuit is off. Under this condition, no automatic muting will occur if the input is continuously zero. When IZD is HIGH, the zero detect feature is enabled. If the input data is continuously zero for 65, 536 cycles of BCKIN, the output will be immediately forced to a bipolar zero state ( $V_{CC}/2$ ). The zero detection feature is used to avoid noise which may occur when the input is DC. When the output is forced to bipolar zero, there may be an audible click. PCM1727 allows the zero detect feature to be disabled so the user can implement an external muting circuit.

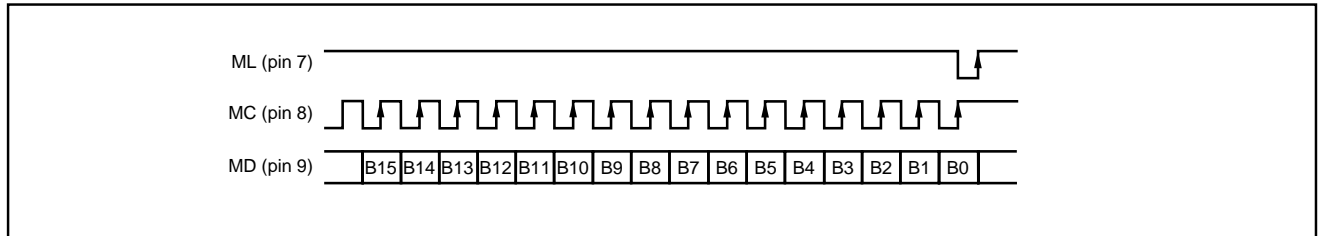


FIGURE 8. Three-Wire Serial Interface.

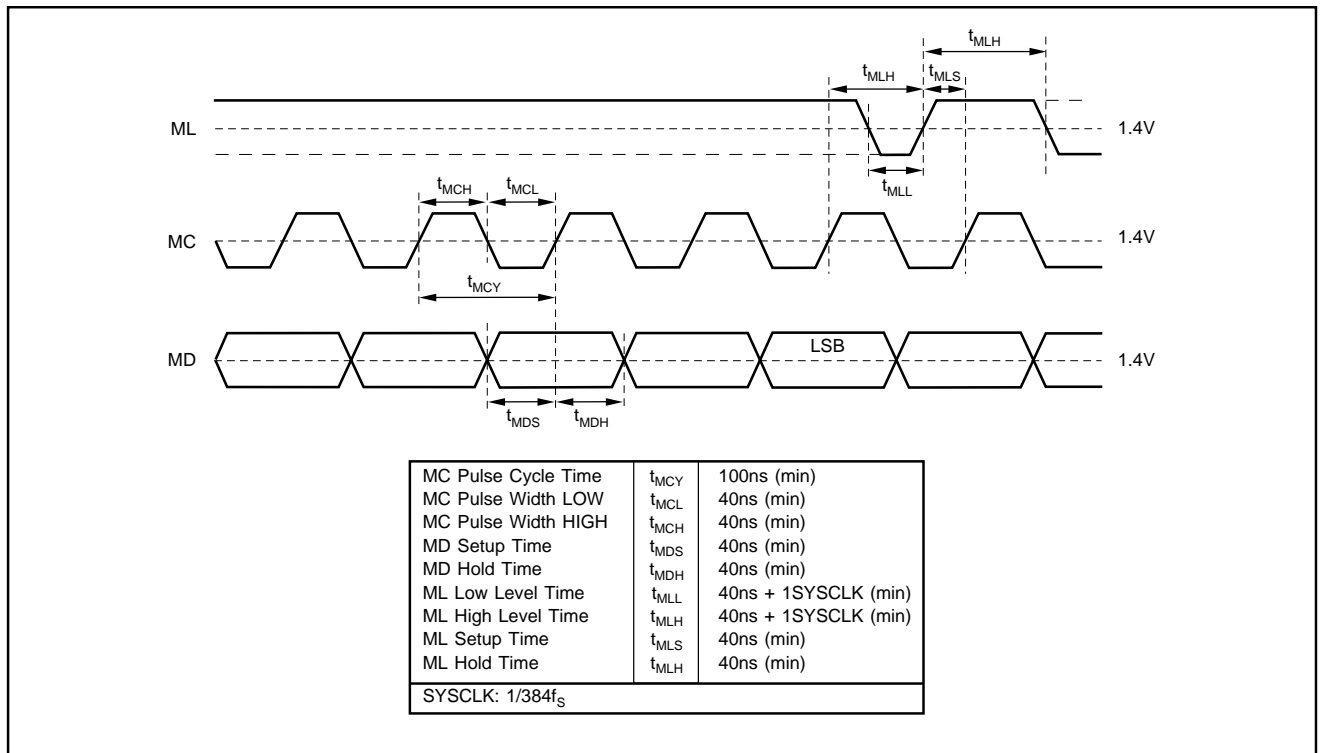


FIGURE 9. Program Register Input Timing.

## APPLICATION CONSIDERATIONS

### DELAY TIME

There is a finite delay time in delta-sigma converters. In analog-to-digital converters, this is commonly referred to as latency. For a delta-sigma DAC, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of the PCM1727:

$$t_D = 11.125 \times 1/f_s$$

For  $f_s = 44.1\text{kHz}$ ,  $t_D = 11.125/44.1\text{kHz} = 251.4\mu\text{s}$

Applications using data from a disc or tape source, such as CD audio, DVD audio, Video CD, DAT, Minidisc, etc., generally are not affected by delay time.

### OUTPUT FILTERING

For testing purposes, all dynamic tests are done on the PCM1727 using a 20kHz low-pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low-pass filter removes out-of-band noise. Although not audible, it may affect dynamic specification numbers.

The performance of the internal low-pass filter from DC to 24kHz is shown in Figure 10. The higher frequency rolloff of the filter is shown in Figure 11. If an application has the PCM1727 driving a wideband amplifier, it is recommended to use an external low-pass filter. A simple 3rd-order filter is shown in Figure 12. For some applications, a passive RC filter or 2nd-order filter may be adequate.

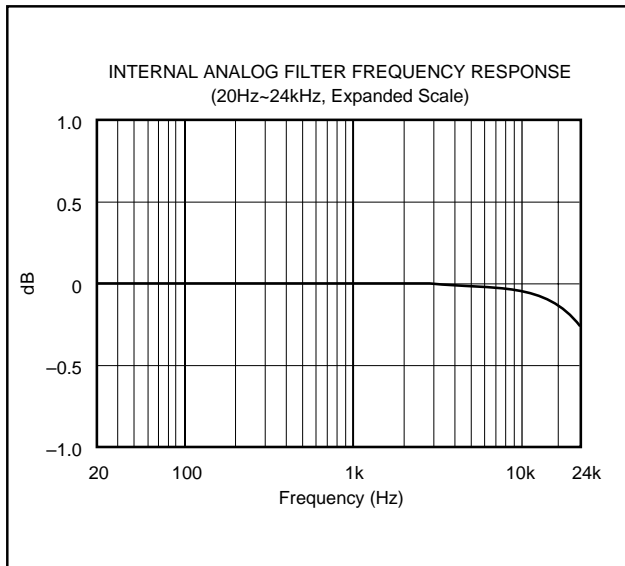


FIGURE 10. Low-Pass Filter Frequency Response.

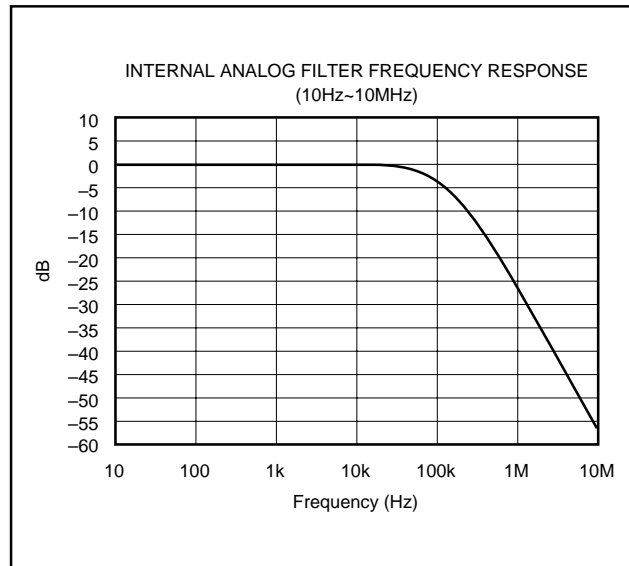


FIGURE 11. Low-Pass Filter Wideband Frequency Response.

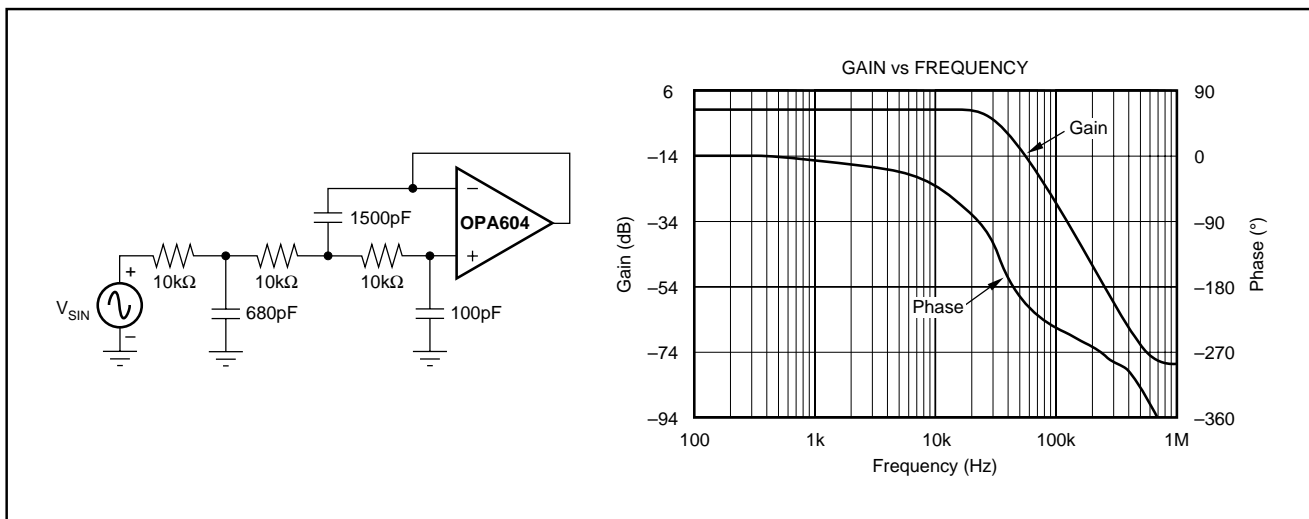


FIGURE 12. 3rd-Order Low-Pass Filter.

**Reset**

The PCM1727 has both an internal power-on reset circuit and the  $\overline{\text{RSTB}}$  pin (pin 10) which accepts an external forced reset by  $\overline{\text{RSTB}} = \text{LOW}$ . For internal power-on reset, initialize (reset) is done automatically at power on  $V_{\text{DD}} > 2.2\text{V}$  (typ). During internal reset = LOW, the output of the DAC is invalid and the analog outputs are forced to  $V_{\text{CC}}/2$ . Figure 13 illustrates the timing of the internal power-on reset.

The PCM1727 accepts an external forced reset when  $\overline{\text{RSTB}} = \text{L}$ . When  $\overline{\text{RSTB}} = \text{L}$ , the output of the DAC is invalid and the analog outputs are forced to  $V_{\text{CC}}/2$  after internal initialization (1024 system clocks count after  $\overline{\text{RSTB}} = \text{H}$ .) Figure 14 illustrates the timing of the  $\overline{\text{RSTB}}$  reset pin.

For system applications, the power-up time of the internal PLL circuit to provide a stable system clock output, is approximately 1024 system clocks plus a 15ms transient time.

**POWER SUPPLY CONNECTIONS**

The PCM1727 has three power supply connections: digital ( $V_{\text{DD}}$ ), analog ( $V_{\text{CA}}$ ), and PLL ( $V_{\text{CP}}$ ). Each connection also has a separate ground return pin. It is acceptable to use a

common +5V power supply for all three power pins. If separate supplies are used without a common connection, the delta between the supplies during ramp-up time must be less than 0.3V. An application circuit to avoid a power-on latch-up condition is shown in Figure 15.

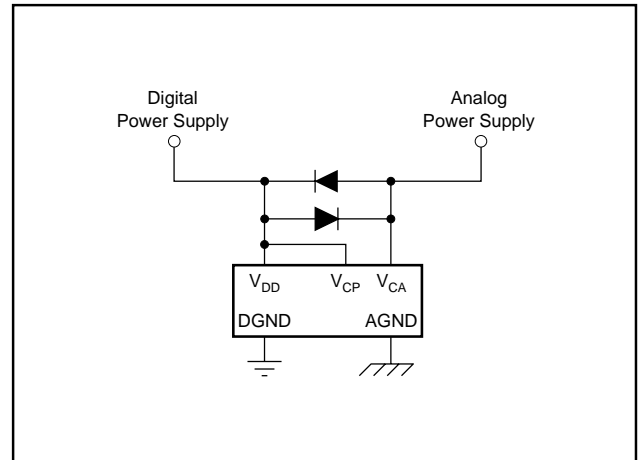


FIGURE 15. Latch-up Prevention Circuit.

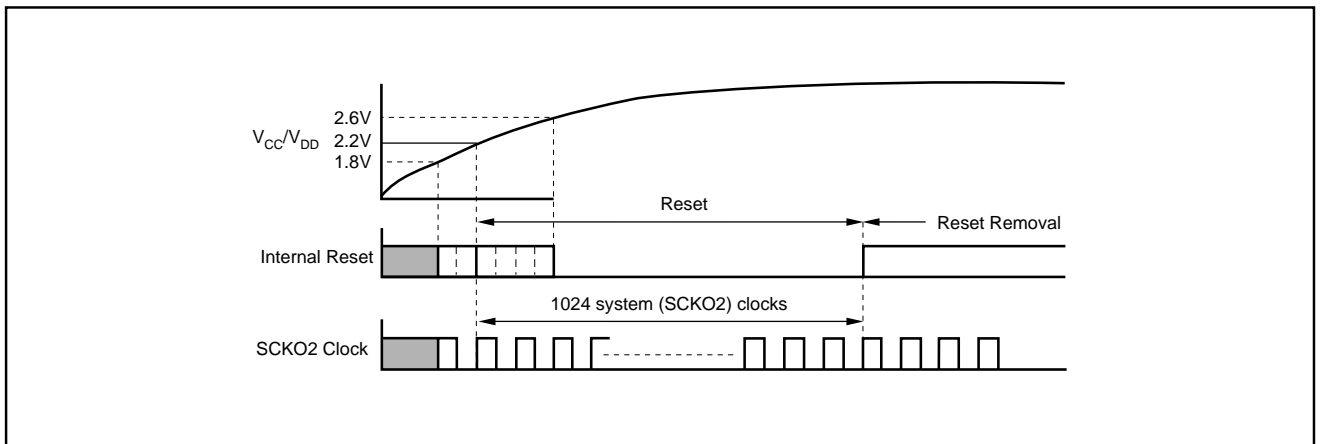


FIGURE 13. Internal Power-On Reset Timing.

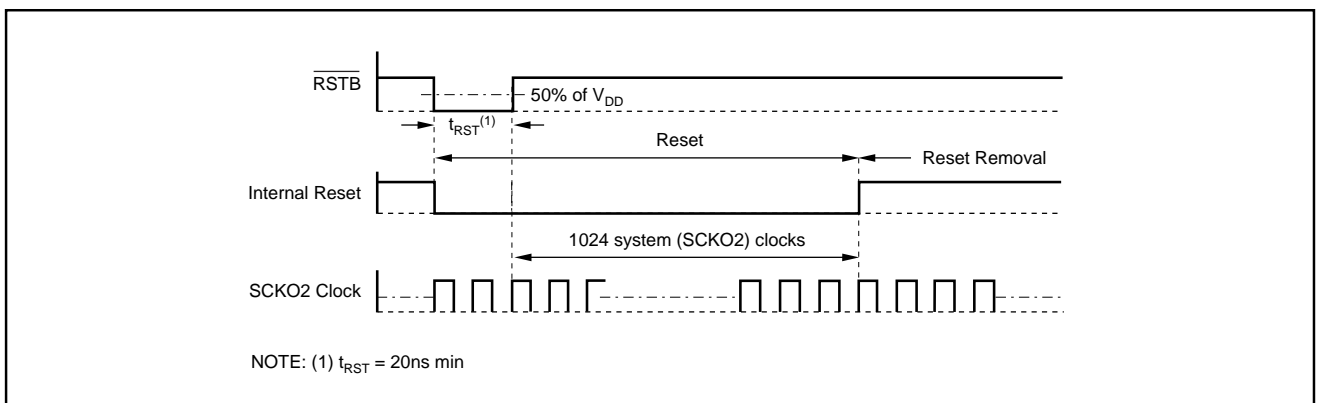


FIGURE 14.  $\overline{\text{RSTB}}$ -Pin Reset Timing.

**BYPASSING POWER SUPPLIES**

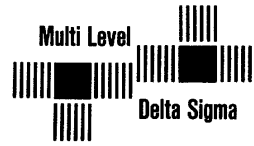
The power supplies should be bypassed as close as possible to the unit. Refer to Figure 18 for optimal values of bypass capacitors. It is also recommended to include a 0.1µF ceramic capacitor in parallel with the 10µF tantalum capacitor.

**THEORY OF OPERATION**

The delta-sigma section of the PCM1727 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format.

A block diagram of the 5-level delta-sigma modulator is shown in Figure 16. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8X interpolation filter is  $48f_s$  for a  $384f_s$  system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 17.



**AC-3 APPLICATION CIRCUIT**

A typical application for the PCM1727 is AC-3 5.1 channel audio decoding and playback. This circuit uses the PCM1727 to develop the audio system clock from the 27MHz video clock, with the SCKO2 pin used to drive the AC-3 decoder and two PCM1720 units, the non-PLL version of the PCM1723 and PCM1727.

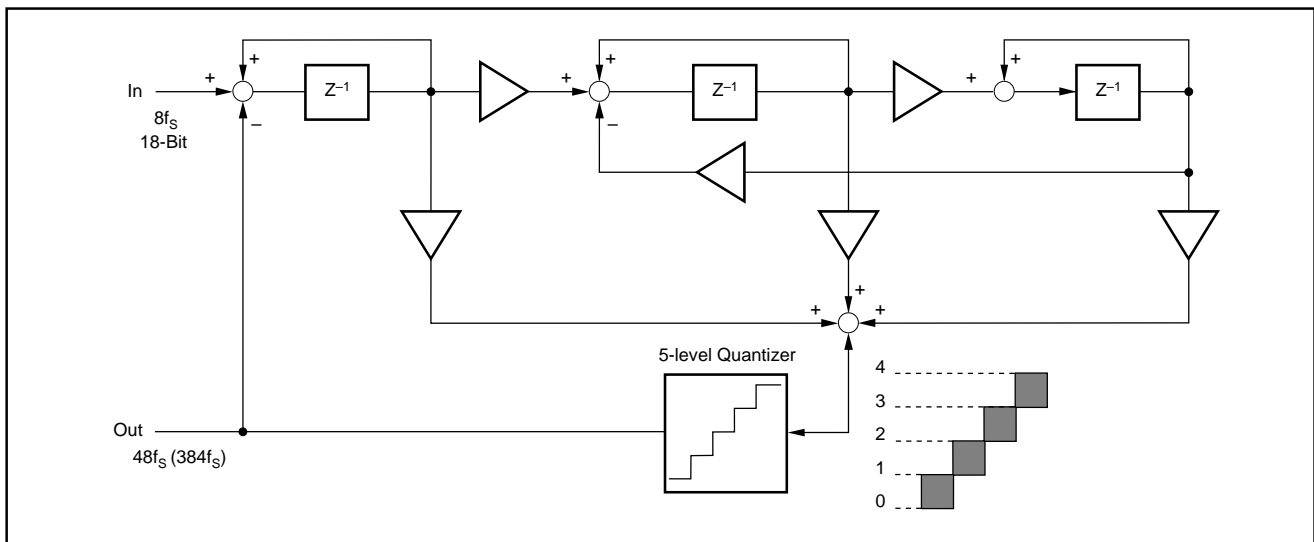


FIGURE 16. 5-Level ΔΣ Modulator Block Diagram.

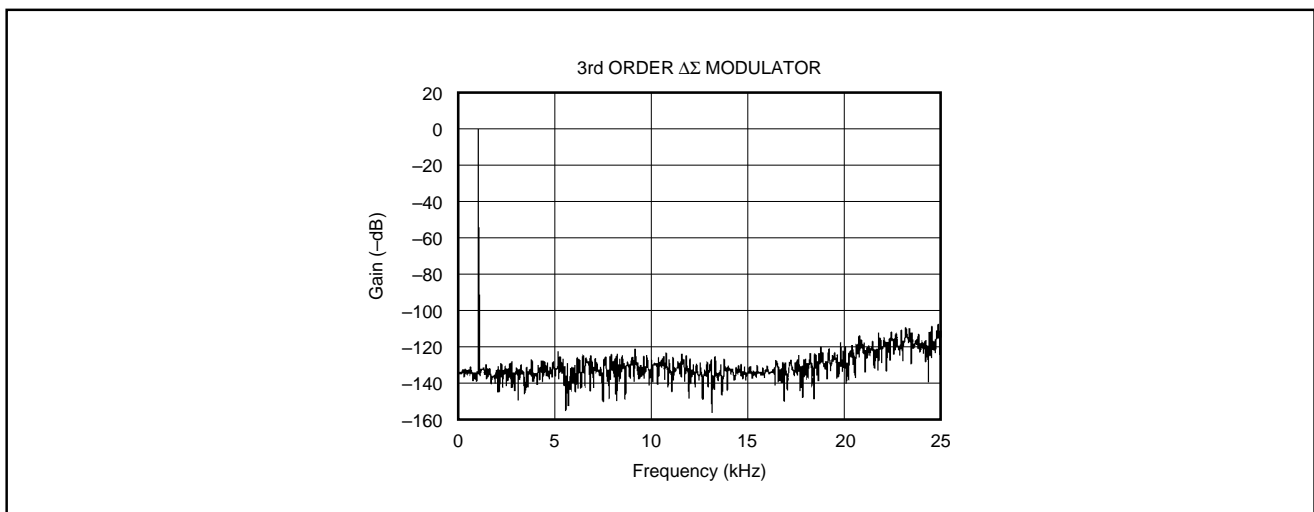


FIGURE 17. Quantization Noise Spectrum.

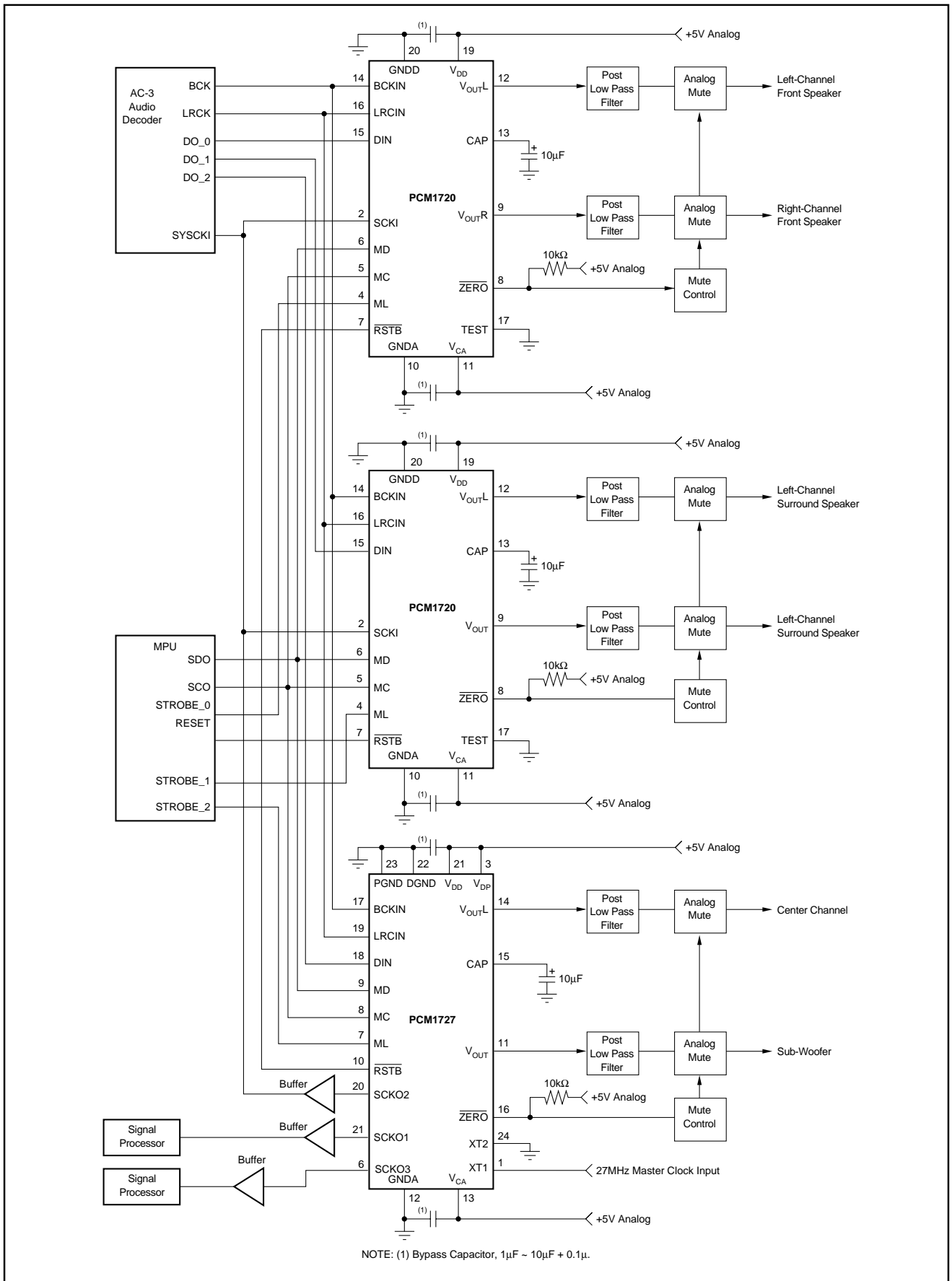


FIGURE 18. Connection Diagram for a 6-Channel AC-3 Application.



### Revision History

| DATE | REVISION   | PAGE   | SECTION                    | DESCRIPTION  |
|------|------------|--|----------------------------|--|
| 5/07 | A          | —  | Entire Document            | Updated format and added overbars to RSTB and ZERO.                            |
|      |            | 2  | Electrical Characteristics | Added "Selectable" to <i>Audio Data Interface Format</i> typical value column. |
|      |            |  |                            | Deleted "Selectable" from <i>Audio Data Format</i> unit column.                |
|      |            | 6  | Dual PLL Circuit           | Changed "XT2 should be connected" to "XT2 must be connected."                  |
|      |            |  |                            | Added sentence regarding XT1 signal amplitude and C1, C2 determination.        |
|      |            | 7  | Figure 3                   | Changed 2.0V/0.8V to 1.2V/0.4V.  |
|      |            | 8  | Dual PLL Circuit           | Deleted paragraph regarding frequency error.                                   |
|      |            | 10   | Register 3                 | Changed B3 from "YES" to "res" (typo).   |
| 11   | Register 3 | Added sentence to Bit 6 regarding interval time must be greater than 20μs. |                            |  |
| 15   | Figure 18  | Changed Figure 18.   |                            |  |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| PCM1727E         | ACTIVE                | SSOP         | DB              | 24   | 58          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCM1727E/2KG4    | ACTIVE                | SSOP         | DB              | 24   |             | TBD                     | Call TI          | Call TI                      |
| PCM1727EG4       | ACTIVE                | SSOP         | DB              | 24   | 58          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

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<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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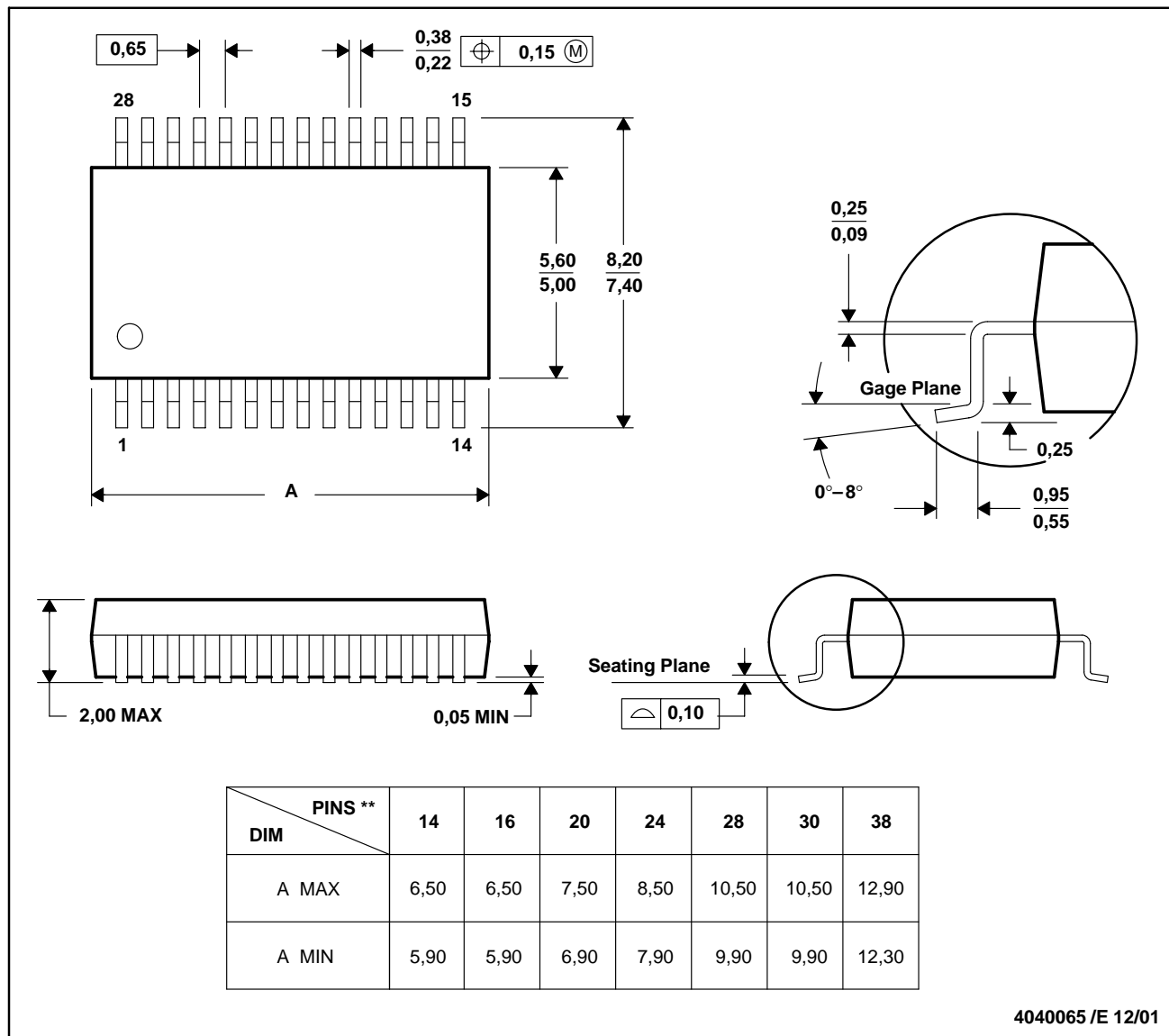
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MSS0002E - JANUARY 1995 - REVISED DECEMBER 2001

**DB (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



4040065 / E 12/01

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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| DSP                   | <a href="http://dsp.ti.com">dsp.ti.com</a>                         |
| Interface             | <a href="http://interface.ti.com">interface.ti.com</a>             |
| Logic                 | <a href="http://logic.ti.com">logic.ti.com</a>                     |
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