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[IXGQ85N33PCD1](#)

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Advance Technical Information

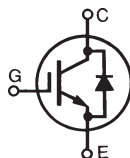
Polar™ High Speed IGBT
with Anti-Parallel Diode
for PDP Sustain Circuit

IXGQ85N33PCD1

$$V_{CES} = 330 \text{ V}$$

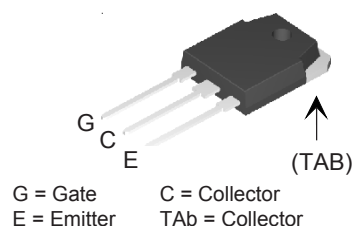
$$I_{CP} = 340 \text{ A}$$

$$V_{CE(sat)} \leq 2.1 \text{ V}$$



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}$	330	V
V_{GEM}		± 30	V
I_{C25}	$T_C = 25^\circ\text{C}$, IGBT chip capability	85	A
I_{CP}	$T_J \leq 150^\circ\text{C}$, $t_p \leq 1 \mu\text{s}$, $D \leq 1\%$	340	A
I_{DP}	$T_J \leq 150^\circ\text{C}$, $t_p < 10 \mu\text{s}$	40	A
$I_{C(RMS)}$	Lead current limit	75	A
SSOA (RBSOA)	$V_{GE} = 15 \text{ V}$, $T_{VJ} = 150^\circ\text{C}$, $R_G = 20 \Omega$ Clamped inductive load, $V_{CE} < 300 \text{ V}$	$I_{CM} = 96$	A
P_c	$T_C = 25^\circ\text{C}$	150	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
	Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s	300	$^\circ\text{C}$
	Plastic body	260	
M_d	Mounting torque	1.3/10	Nm/lb.in.
Weight		5.5	g

TO-3P


Features

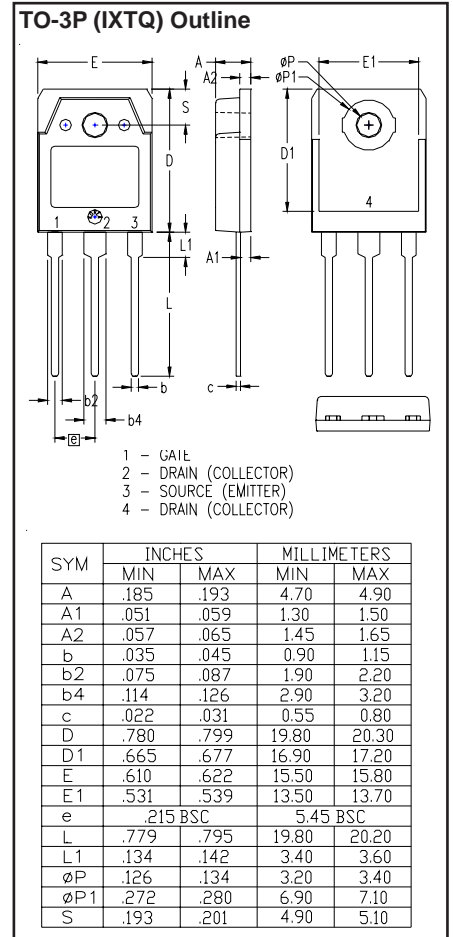
- International standard package
- Fast t_{fi} for minimum turn off switching losses
- MOS Gate turn-on - drive simplicity
- Positive dV_{sat}/dt for paralleling

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Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
$V_{GE(th)}$	$I_C = 1 \text{ mA}$, $V_{CE} = V_{GE}$	3.0		6.0 V
I_{CES}	$V_{CE} = 330 \text{ V}$			1 μA
	$V_{GE} = 0 \text{ V}$		$T_J = 125^\circ\text{C}$	200 μA
I_{GES}	$V_{CE} = 0 \text{ V}$, $V_{GE} = \pm 20 \text{ V}$			$\pm 100 \text{ nA}$
$V_{CE(sat)}$	$V_{GE} = 15 \text{ V}$, Note 1	$I_C = 50 \text{ A}$		1.43 2.1 V
			$T_J = 125^\circ\text{C}$	1.47 V
		$I_C = 100 \text{ A}$		1.85 3.0 V
			$T_J = 125^\circ\text{C}$	2.0 V

Symbol		Test Conditions	Characteristic Values		
		($T_J = 25^\circ\text{C}$ unless otherwise specified)	Min.	Typ.	Max.
g_{fs}		$I_C = 43\text{ A}, V_{CE} = 10\text{ V}$	30	49	S
C_{ies}	}	$V_{CE} = 25\text{ V}, V_{GE} = 0\text{ V}, f = 1\text{ MHz}$		2200	pF
C_{oes}				155	pF
C_{res}				25	pF
Q_g	}	$I_C = 43\text{ A}, V_{GE} = 15\text{ V}, V_{CE} = 0.5 V_{CES}$		80	nC
Q_{ge}				15	nC
Q_{gc}				23	nC
$t_{d(on)}$	}	Resistive load, $T_J = 25^\circ\text{C}$ $I_C = 50\text{ A}, V_{GE} = 15\text{ V}$ $V_{CE} = 240\text{ V}, R_G = 5\ \Omega$		20	ns
t_{ri}				43	ns
$t_{d(off)}$				87	ns
t_{fi}				72	350
$t_{d(on)}$	}	Resistive load, $T_J = 125^\circ\text{C}$ $I_C = 50\text{ A}, V_{GE} = 15\text{ V}$ $V_{CE} = 240\text{ V}, R_G = 5\ \Omega$		20	ns
t_{ri}				95	ns
$t_{d(off)}$				88	ns
t_{fi}				130	ns
R_{thJC}					0.833 K/W
R_{thCK}			0.25		K/W

Reverse Diode		Characteristic Values		
		$(T_J = 25^\circ\text{C}$ unless otherwise specified)		
Symbol	Test Conditions	Min.	Typ.	Max.
V_F	$I_F = 20\text{ A}, V_{GE} = 0\text{ V}$, Note 1			2.0 V
	$I_F = 40\text{ A}, V_{GE} = 0\text{ V}$, Note 1			2.8 V
R_{thJC}				2.5 K/W
t_{rr}				250 ns

 Note 1: Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$


IXYS reserves the right to change limits, test conditions and dimensions.

 IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338 B2
4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ 25 °C

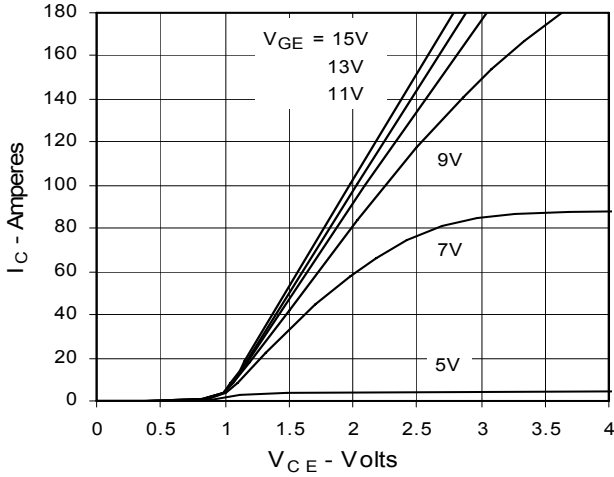


Fig. 2. Extended Output Characteristics @ 25 °C

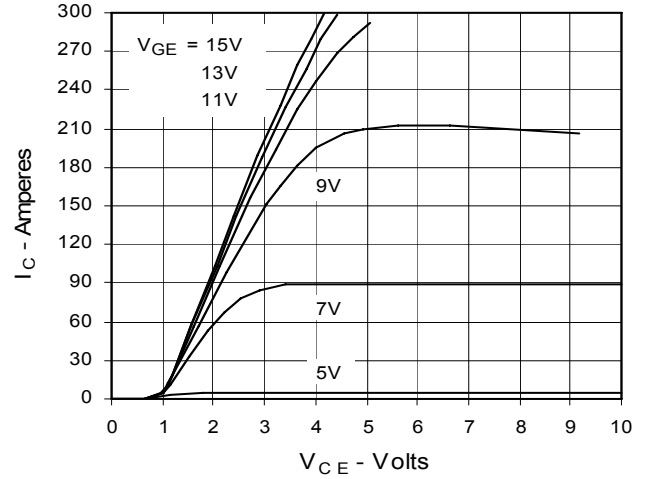


Fig. 3. Output Characteristics @ 125 °C

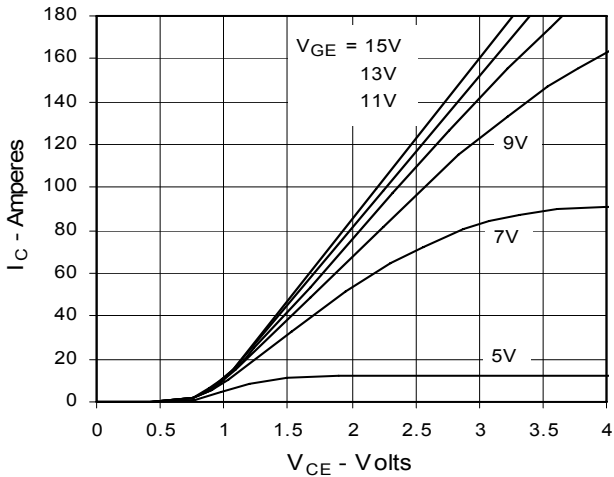


Fig. 4. Dependence of $V_{CE(sat)}$ on Temperature

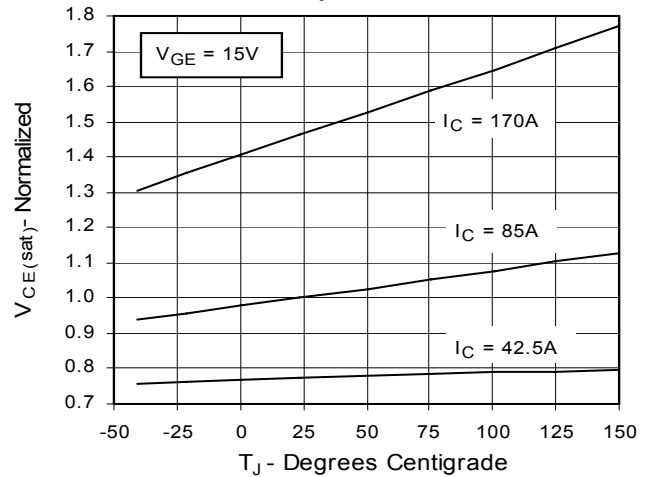


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter voltage

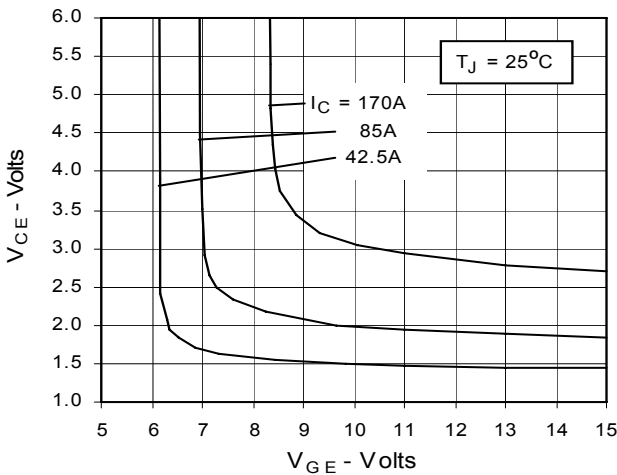


Fig. 6. Input Admittance

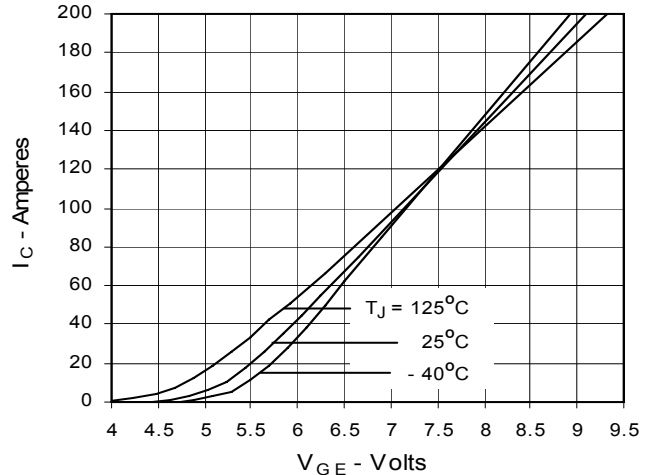


Fig. 7. Transconductance

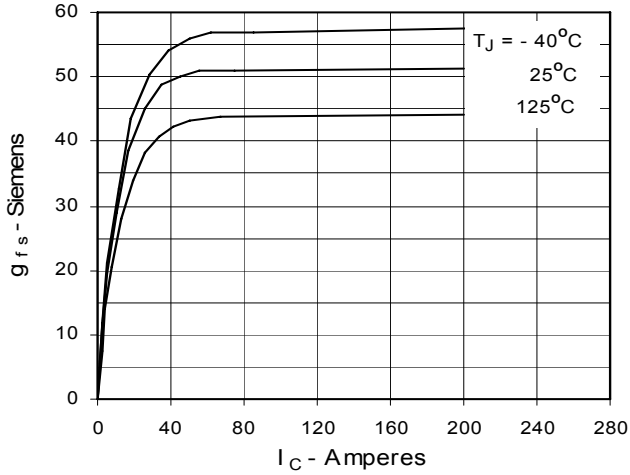


Fig. 8. Resistive Turn-On Rise Time vs. Junction Temperature

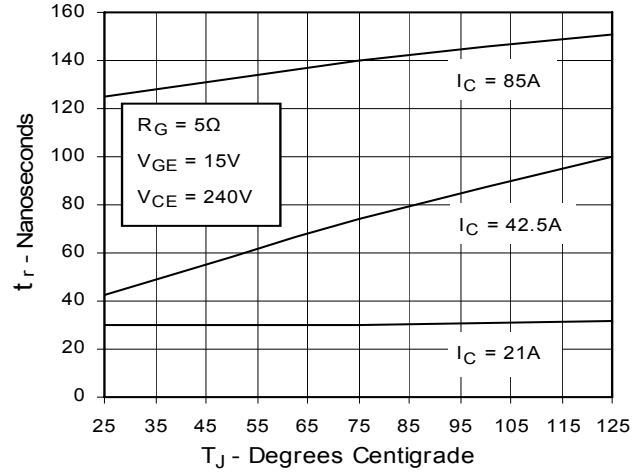


Fig. 9. Resistive Turn-On Rise Time vs. Collector Current

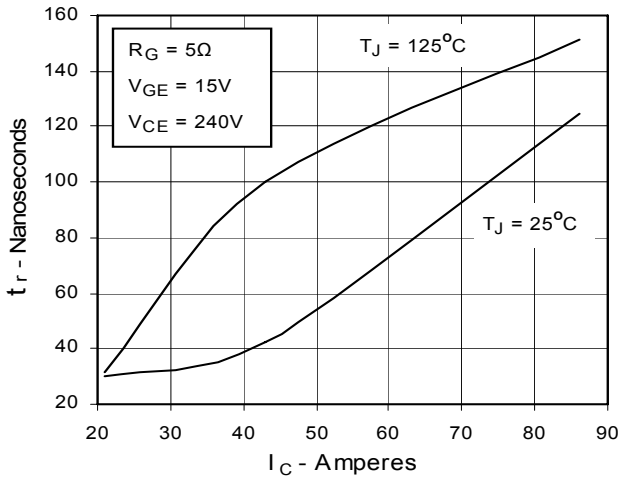


Fig. 10. Resistive Turn-On Rise Time vs. Gate Resistance

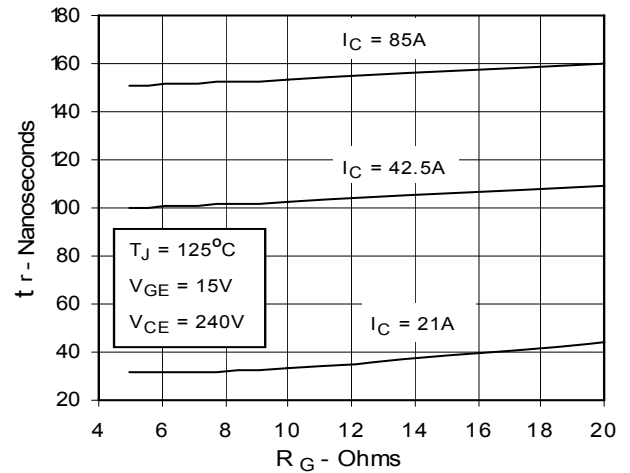


Fig. 11. Resistive Turn-On Delay Time vs. Gate Resistance

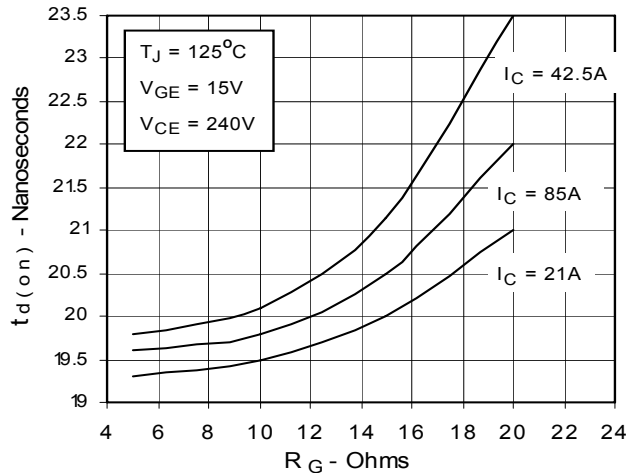


Fig. 12. Resistive Turn-Off Switching Time vs. Junction Temperature

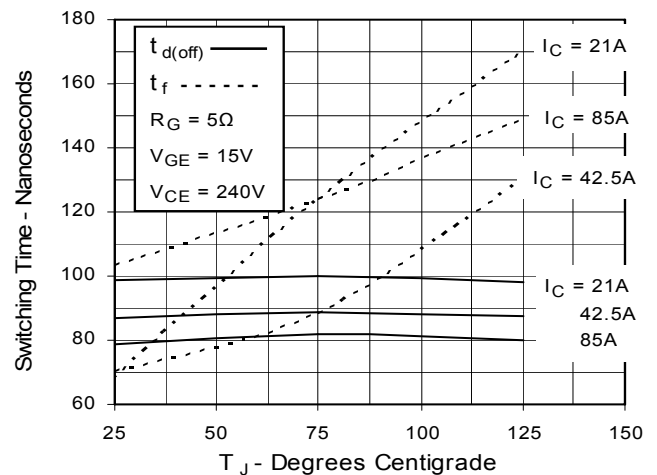


Fig. 13. Resistive Turn-Off Switching Time vs. Collector Current

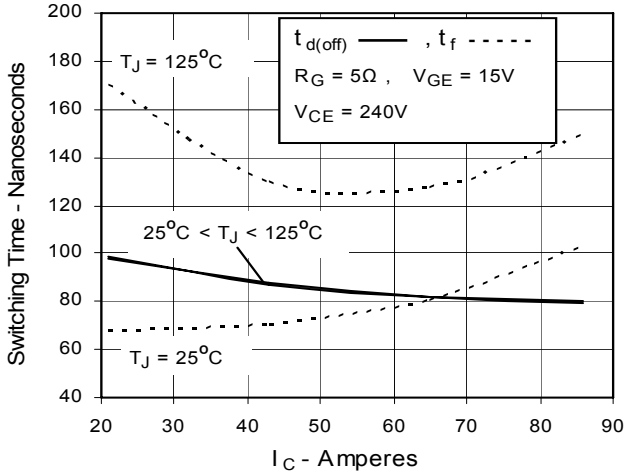


Fig. 14. Resistive Turn-off Switching Time vs. Gate Resistance

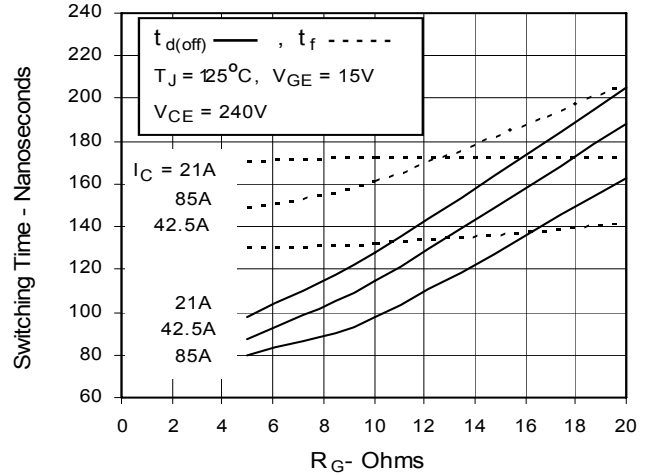


Fig. 15. Reverse-Bias Safe Operating Area

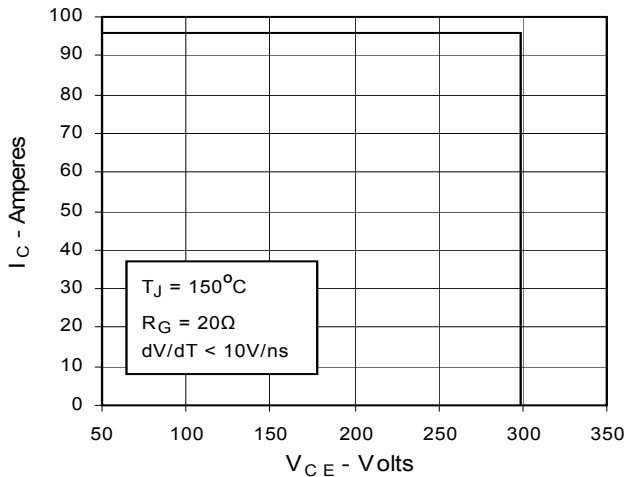


Fig. 16. Gate Charge

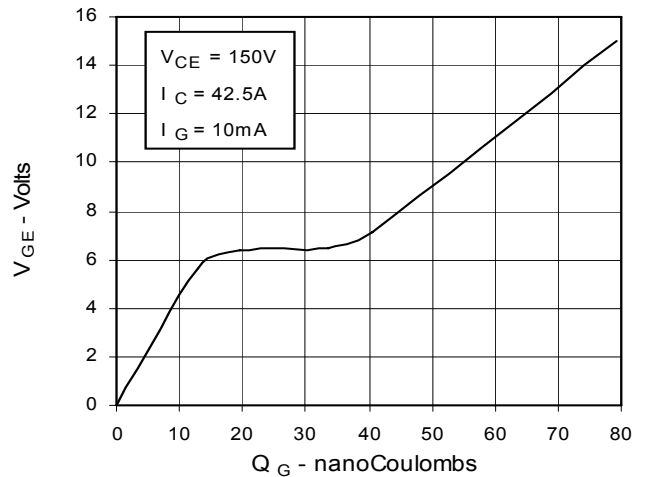


Fig. 17. Capacitance

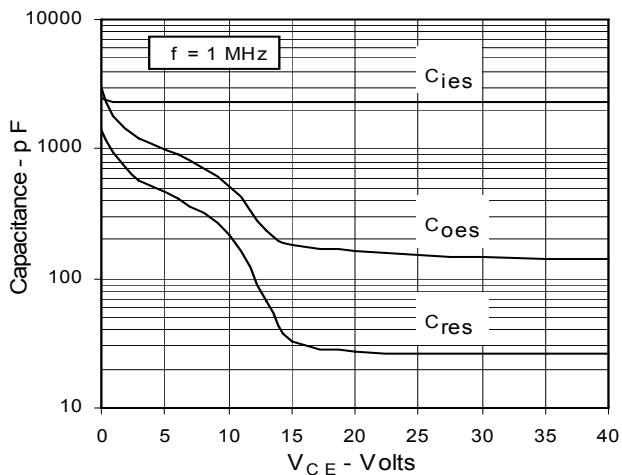


Fig. 18. Maximum Transient Thermal Resistance

