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[Vishay/Siliconix](#)
[SI4368DY-T1-E3](#)

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sales@integrated-circuit.com



Si4368DY
 Vishay Siliconix

N-Channel Reduced Q_{gd} , Fast Switching MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
30	0.0032 at $V_{GS} = 10$ V	25
	0.0036 at $V_{GS} = 4.5$ V	22

FEATURES

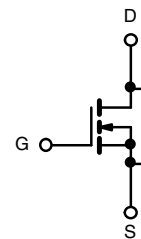
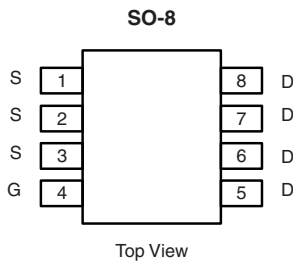
- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low Q_{gd} for Switching Losses Improvement
- TrenchFET[®] Gen II Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
 COMPLIANT
 HALOGEN
FREE
 Available

APPLICATIONS

- Low-Side DC/DC Conversion
 - Notebook, Server, VRM Module
- Fixed Telecom



Ordering Information: Si4368DY-T1-E3 (Lead (Pb)-free)
 Si4368DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
Parameter	Symbol	10 s	Steady State	Unit
Drain-Source Voltage	V_{DS}	30		V
Gate-Source Voltage	V_{GS}	± 12		
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	$T_A = 25$ °C	25	17
		$T_A = 70$ °C	20	13
Pulsed Drain Current (10 μ s Pulse Width)	I_{DM}	70		A
Continuous Source Current (Diode Conduction) ^a	I_S	2.9	1.3	
Avalanch Current	I_{AS}	50		W
Maximum Power Dissipation ^a	P_D	$T_A = 25$ °C	3.5	
		$T_A = 70$ °C	2.2	1
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ s	29	35	°C/W
		Steady State	67	80	
Maximum Junction-to-Foot (Drain)	R_{thJF}	13	16		

Notes:
 a. Surface mounted on 1" x 1" FR4 board.

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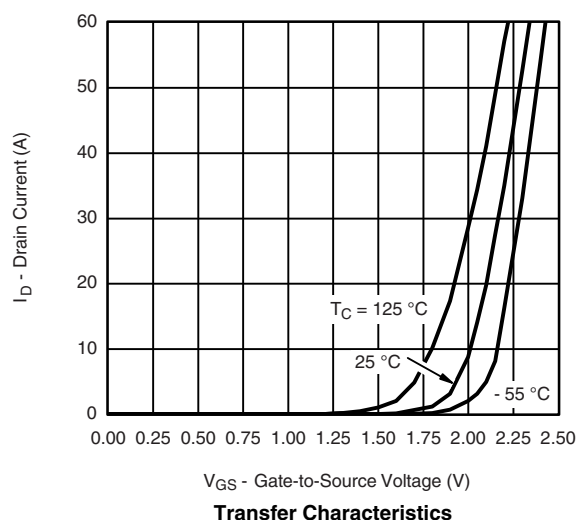
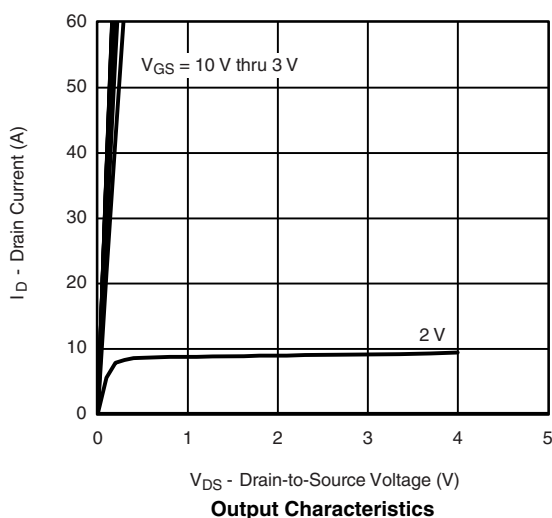
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.6		1.8	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 25 A		0.0026	0.0032	Ω
		V _{GS} = 4.5 V, I _D = 22 A		0.0029	0.0036	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 25 A		150		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.9 A, V _{GS} = 0 V		0.66	1.1	V
Dynamic^b						
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		8340		pF
Output Capacitance	C _{oss}			850		
Reverse Transfer Capacitance	C _{rss}			355		
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 20 A		53	80	nC
Gate-Source Charge	Q _{gs}			17.5		
Gate-Drain Charge	Q _{gd}			6.5		
Gate Resistance	R _g		f = 1 MHz	0.8	1.2	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 6 Ω		25	38	ns
Rise Time	t _r			20	30	
Turn-Off Delay Time	t _{d(off)}			172	260	
Fall Time	t _f			41	62	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 2.9 A, di/dt = 100 A/μs		42	

Notes:

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

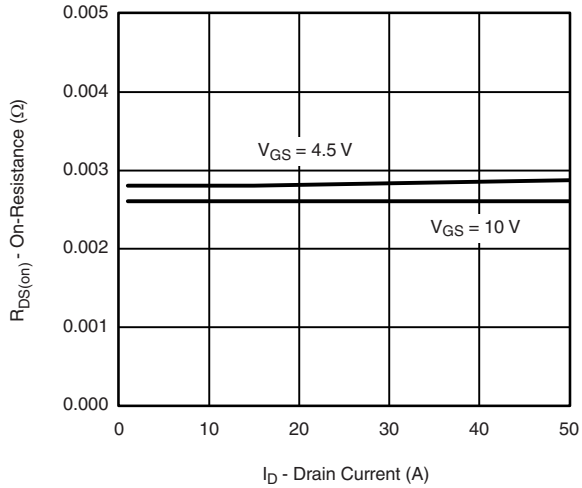
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



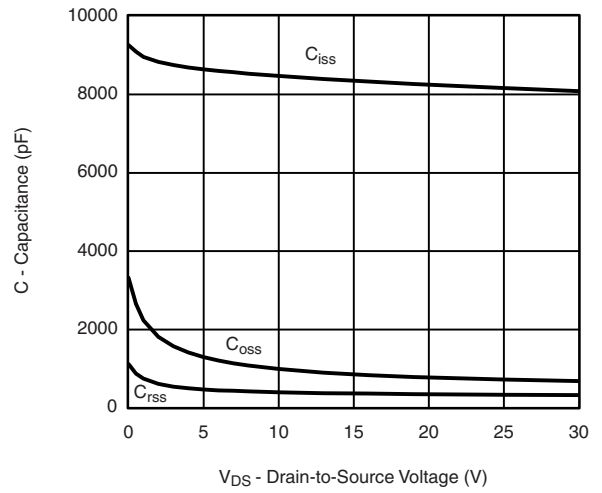


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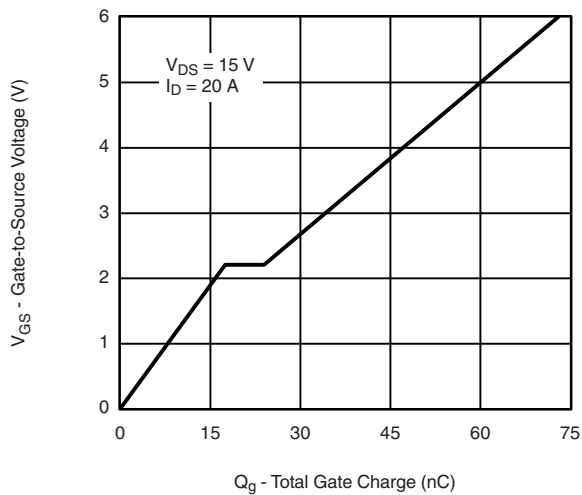
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



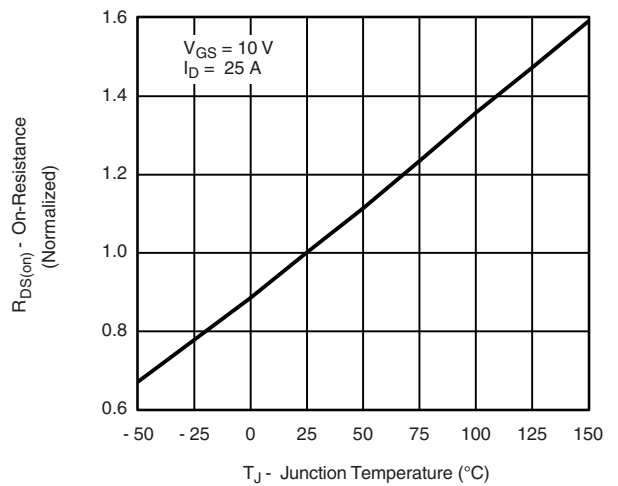
On-Resistance vs. Drain Current



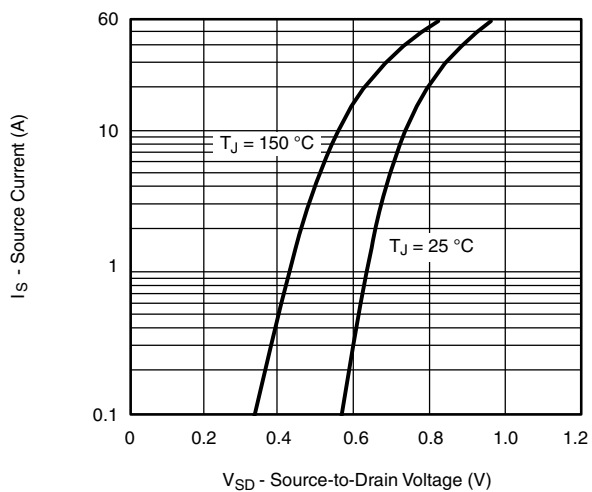
Capacitance



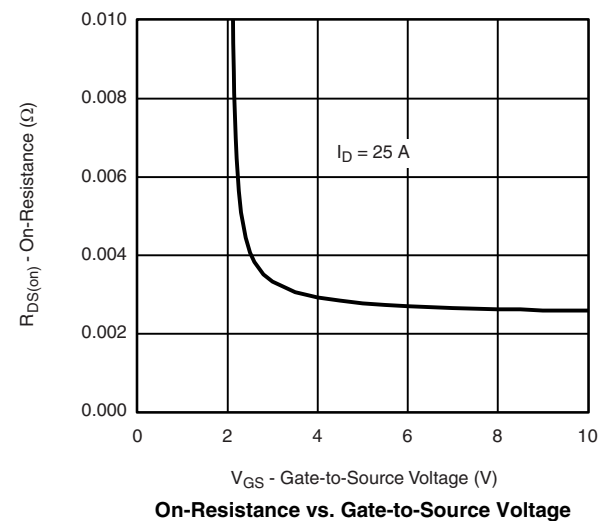
Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



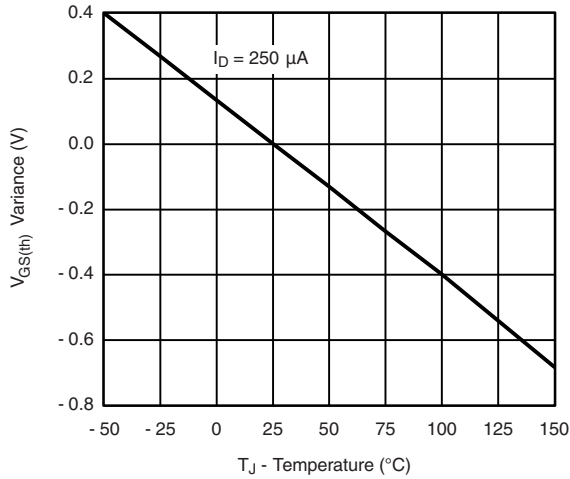
On-Resistance vs. Gate-to-Source Voltage

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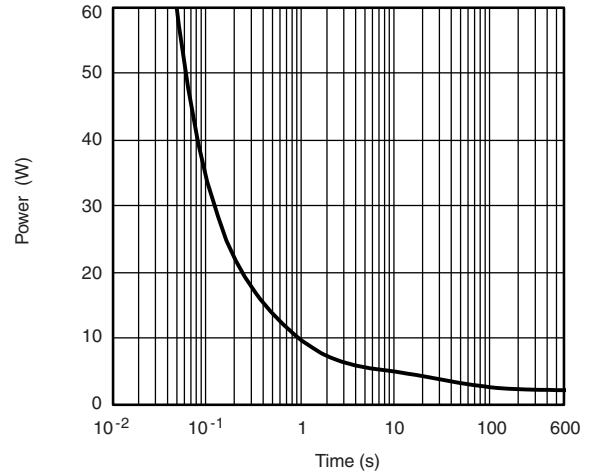
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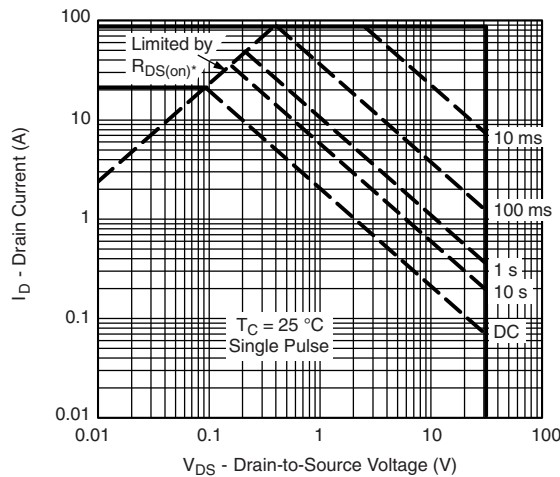
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Threshold Voltage

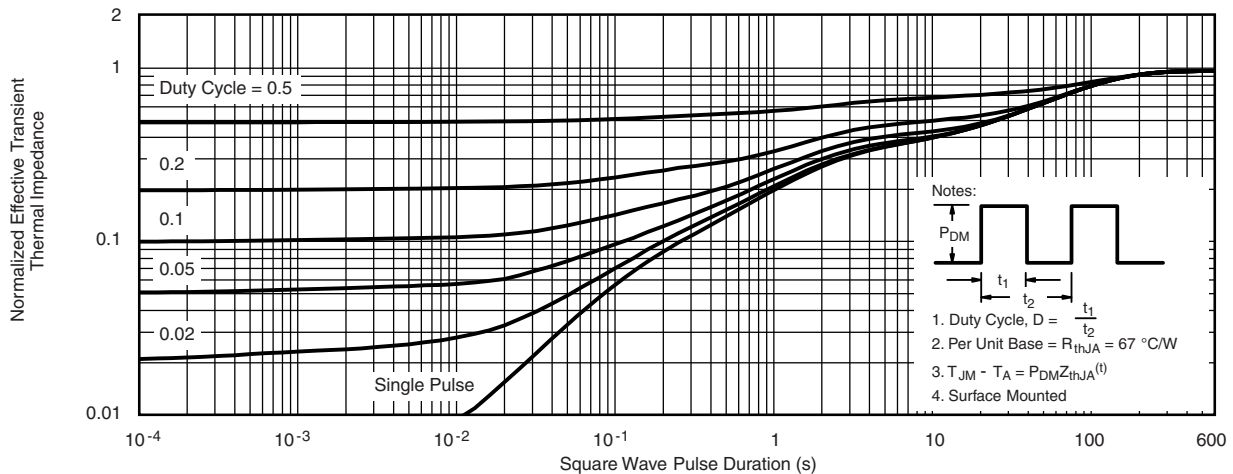


Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case



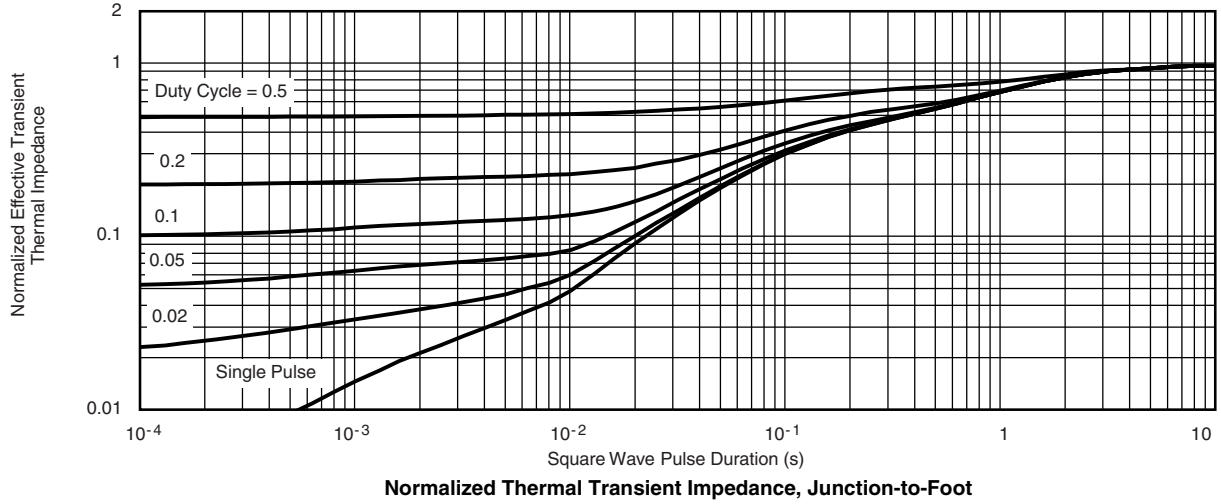
- Notes:
- Duty Cycle, $D = \frac{t_1}{t_2}$
 - Per Unit Base = $R_{thJA} = 67 \text{ }^\circ\text{C/W}$
 - $T_{JM} - T_A = P_{DM} Z_{thJA}^{(1)}$
 - Surface Mounted

Normalized Thermal Transient Impedance, Junction-to-Ambient



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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72704.

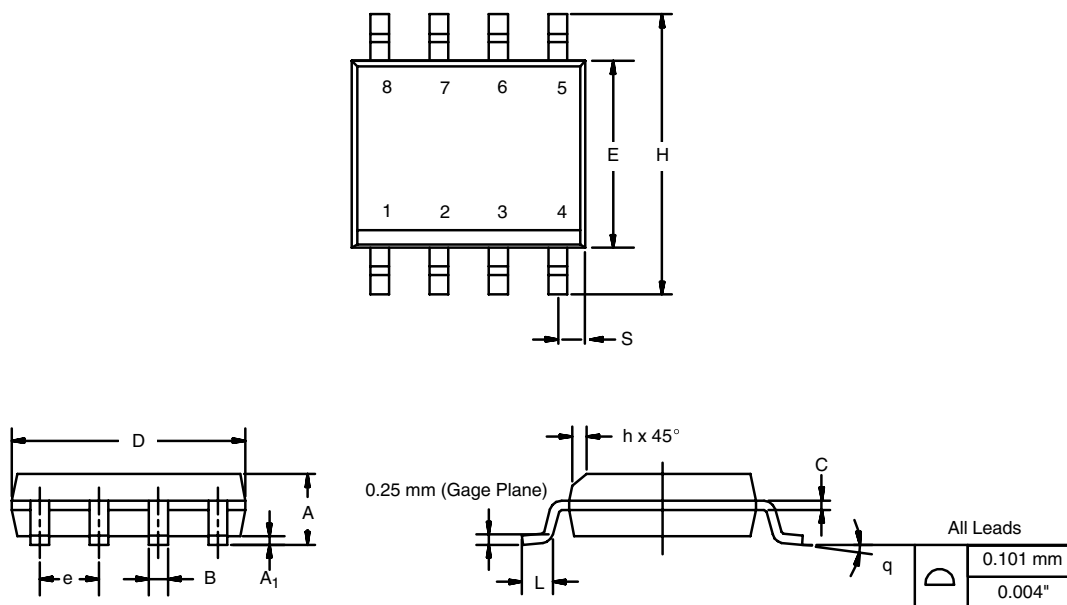


Package Information

Vishay Siliconix

SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

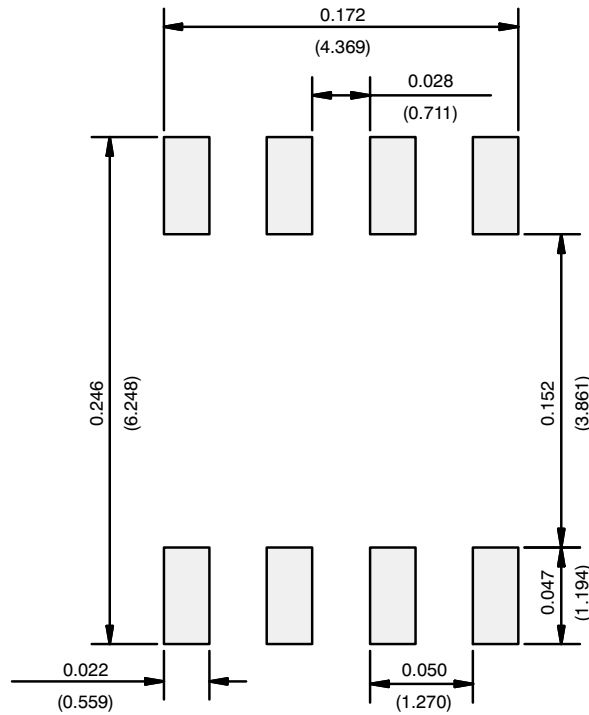
ECN: C-06527-Rev. I, 11-Sep-06
DWG: 5498

Application Note 826

Vishay Siliconix



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
 Dimensions in Inches/(mm)

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