

## **Excellent Integrated System Limited**

Stocking Distributor

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[Vishay/Siliconix](#)  
[SI5445BDC-T1-E3](#)

For any questions, you can email us directly:

[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)



## P-Channel 1.8-V (G-S) MOSFET

<b>PRODUCT SUMMARY</b>			
<b><math>V_{DS}</math> (V)</b>	<b><math>R_{DS(on)}</math> (<math>\Omega</math>)</b>	<b><math>I_D</math> (A)</b>	<b><math>Q_g</math> (Typ.)</b>
<b>- 8</b>	0.033 at $V_{GS} = - 4.5$ V	- 7.1	<b>14</b>
	0.043 at $V_{GS} = - 2.5$ V	- 6.2	
	0.060 at $V_{GS} = - 1.8$ V	- 5.3	

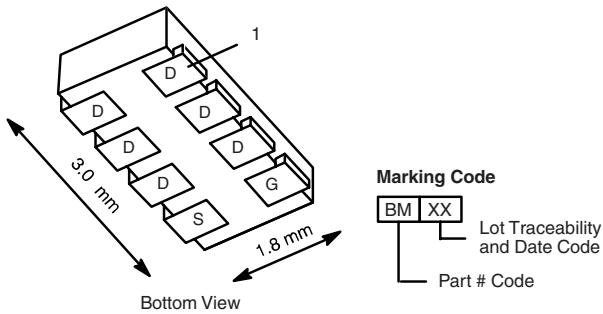
### FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET

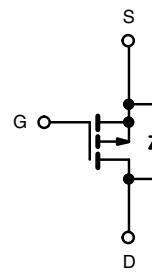


**RoHS**  
COMPLIANT  
**HALOGEN**  
**FREE**  
Available

1206-8 ChipFET®



Ordering Information: Si5445BDC-T1-E3 (Lead (Pb)-free)  
Si5445BDC-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> $T_A = 25$ °C, unless otherwise noted							
Parameter	Symbol	5 s	Steady State	Unit			
Drain-Source Voltage	$V_{DS}$	- 8		$V$			
Gate-Source Voltage	$V_{GS}$	$\pm 8$					
Continuous Drain Current ( $T_J = 150$ °C) <sup>a</sup>	$I_D$	- 7.1		$A$			
		- 5.2					
Pulsed Drain Current	$I_{DM}$	$\pm 20$					
Continuous Source Current <sup>a</sup>	$I_S$	- 2.1					
Maximum Power Dissipation <sup>a</sup>	$P_D$	2.5		$W$			
		1.3					
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150		$^{\circ}C$			
Soldering Recommendations (Peak Temperature) <sup>b, c</sup>		260					

<b>THERMAL RESISTANCE RATINGS</b>					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	45	50	$^{\circ}C/W$	
		85	95		
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	17	20	

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

## Si5445BDC

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### SPECIFICATIONS $T_J = 25^\circ\text{C}$ , unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$ , $I_D = -250 \mu\text{A}$	-0.45		-1.0	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}$ , $V_{GS} = \pm 8 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -8 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-1		$\mu\text{A}$
		$V_{DS} = -8 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 85^\circ\text{C}$			-5	
On-State Drain Current <sup>a</sup>	$I_{D(\text{on})}$	$V_{DS} \leq -5 \text{ V}$ , $V_{GS} = -4.5 \text{ V}$	-20			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(\text{on})}$	$V_{GS} = -4.5 \text{ V}$ , $I_D = -5.2 \text{ A}$		0.027	0.033	$\Omega$
		$V_{GS} = -2.5 \text{ V}$ , $I_D = -4.5 \text{ A}$		0.035	0.043	
		$V_{GS} = -1.8 \text{ V}$ , $I_D = -1.7 \text{ A}$		0.050	0.060	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -5 \text{ V}$ , $I_D = -5.2 \text{ A}$		18		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = -1.1 \text{ A}$ , $V_{GS} = 0 \text{ V}$		-0.8	-1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = -4 \text{ V}$ , $V_{GS} = -4.5 \text{ V}$ , $I_D = -5.2 \text{ A}$		14	21	nC
Gate-Source Charge	$Q_{gs}$			1.8		
Gate-Drain Charge	$Q_{gd}$			3.3		
Gate Resistance	$R_g$	$f = 1 \text{ MHz}$		8		$\Omega$
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = -4 \text{ V}$ , $R_L = 4 \Omega$ $I_D \equiv -1 \text{ A}$ , $V_{GEN} = -4.5 \text{ V}$ , $R_g = 6 \Omega$		12	20	ns
Rise Time	$t_r$			22	35	
Turn-Off Delay Time	$t_{d(\text{off})}$			75	115	
Fall Time	$t_f$			50	75	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = -1.1 \text{ A}$ , $dl/dt = 100 \text{ A}/\mu\text{s}$		75	115	ns
Reverse Recovery Charge	$Q_{rr}$			40	60	

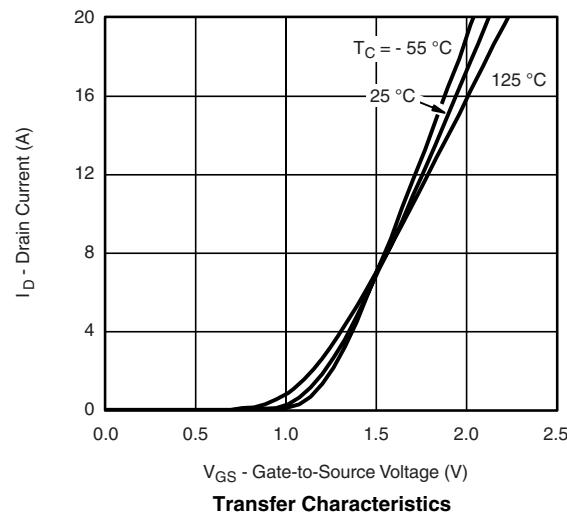
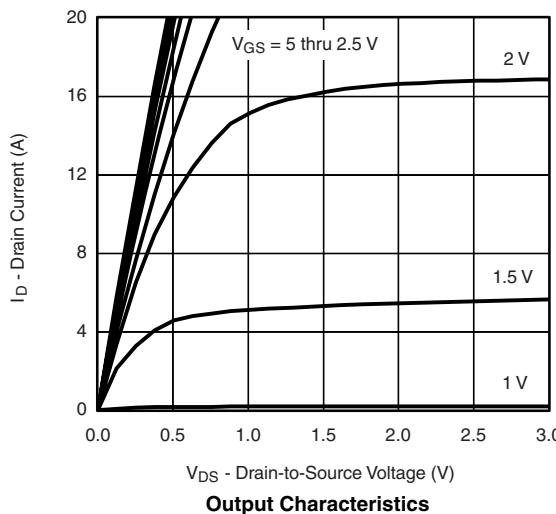
Notes:

a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

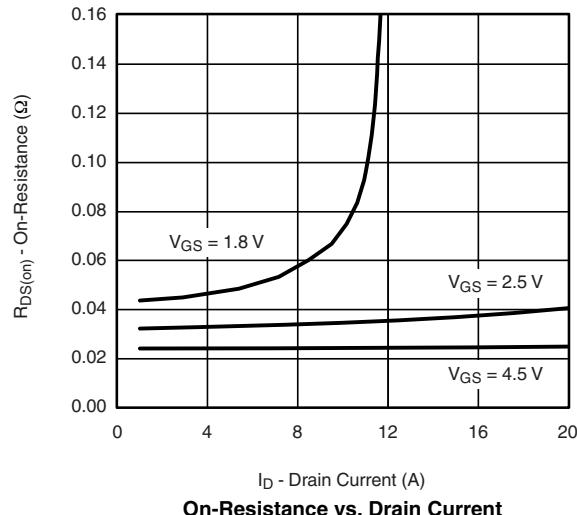
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### TYPICAL CHARACTERISTICS $25^\circ\text{C}$ , unless otherwise noted

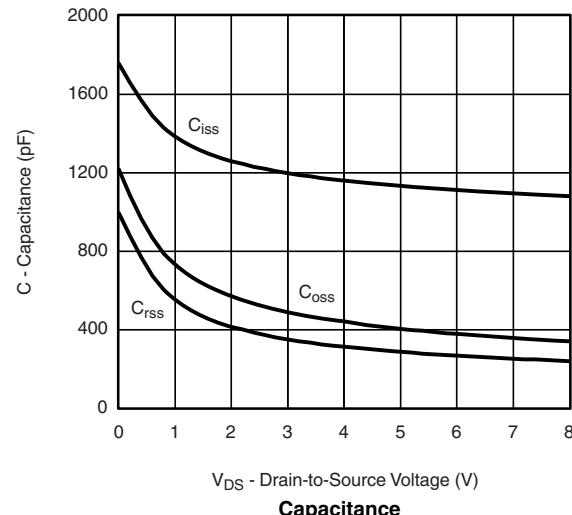




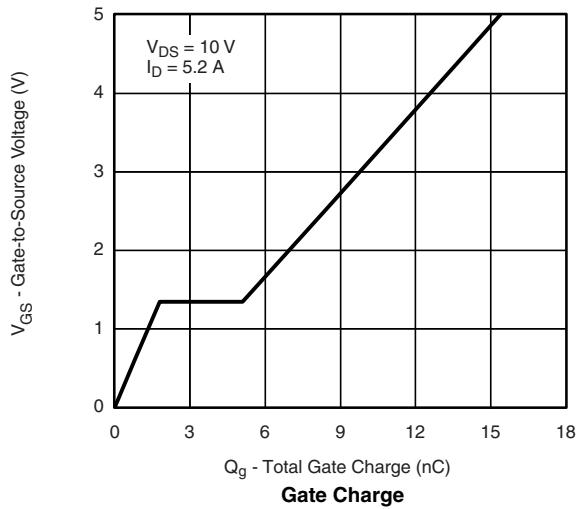
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



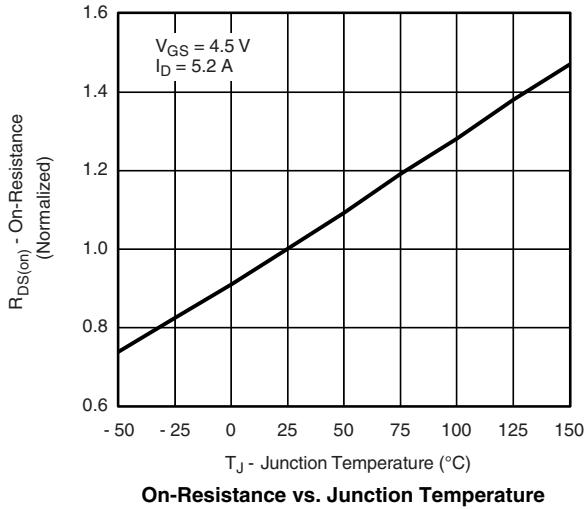
On-Resistance vs. Drain Current



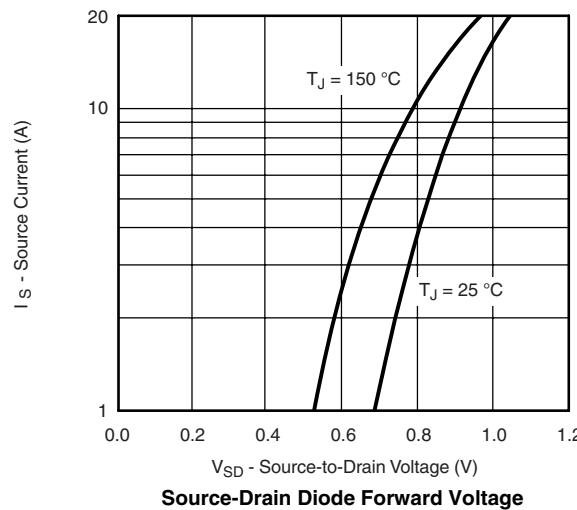
Capacitance



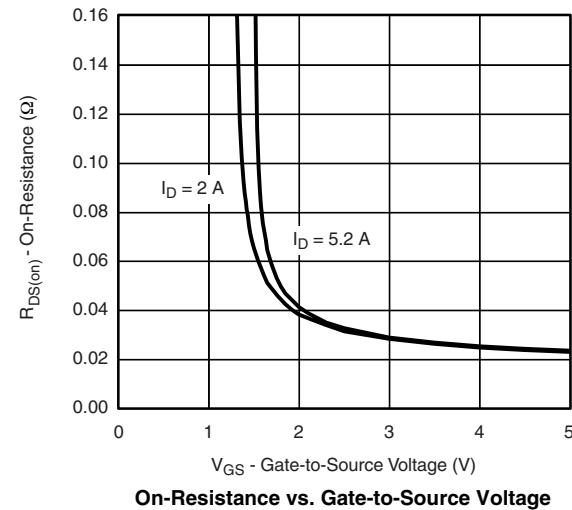
Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



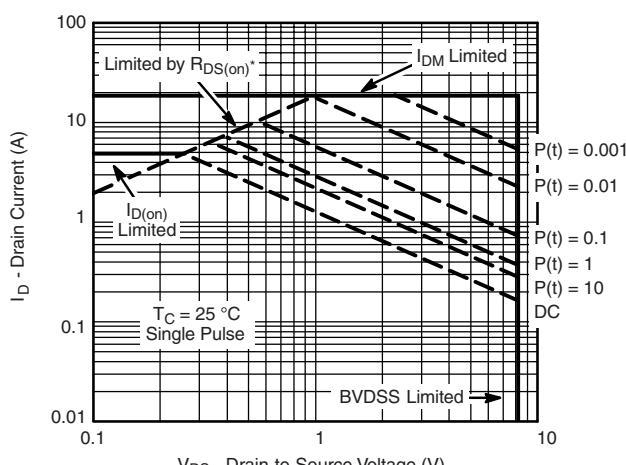
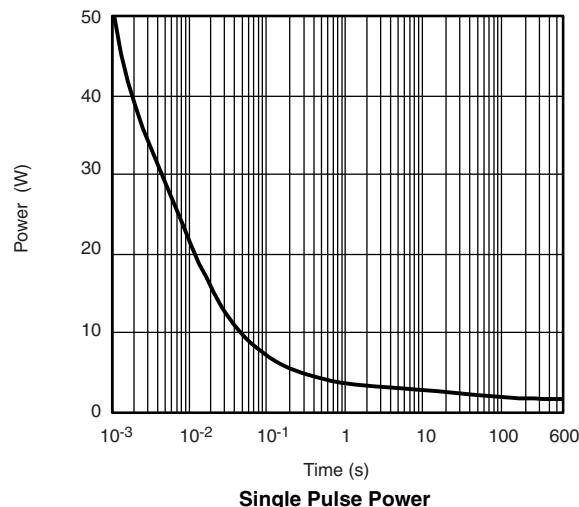
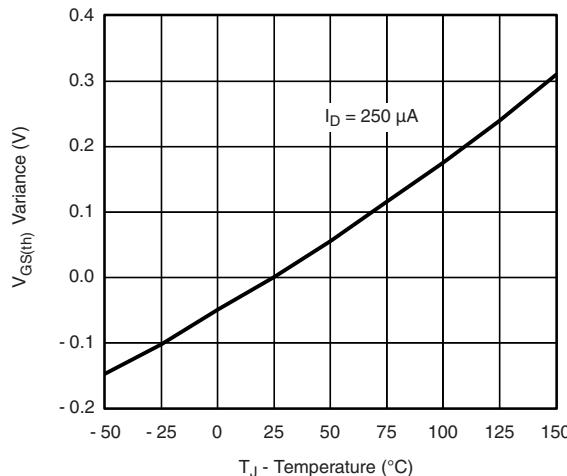
On-Resistance vs. Gate-to-Source Voltage

## Si5445BDC

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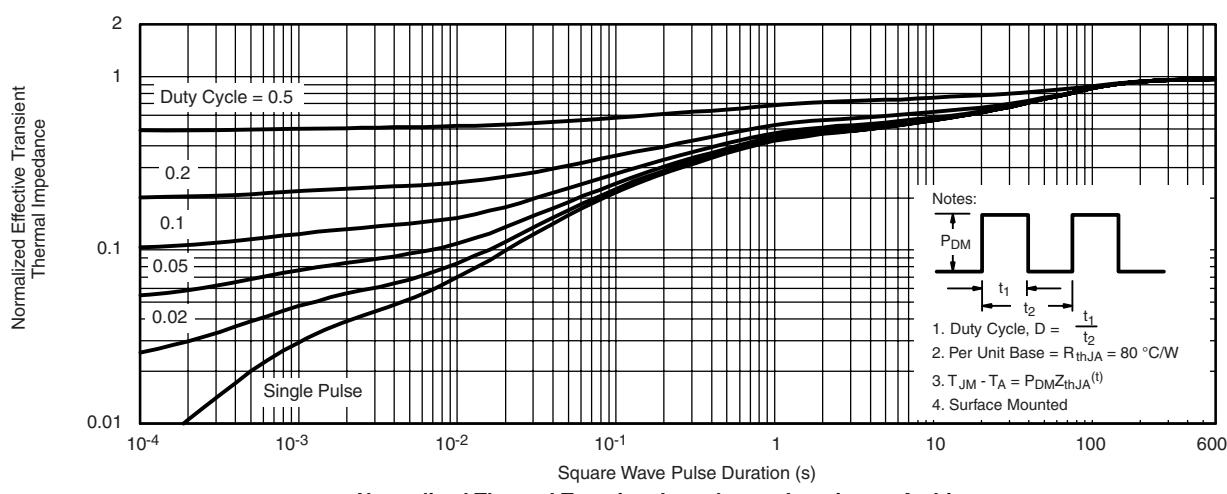


**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

### Safe Operating Area



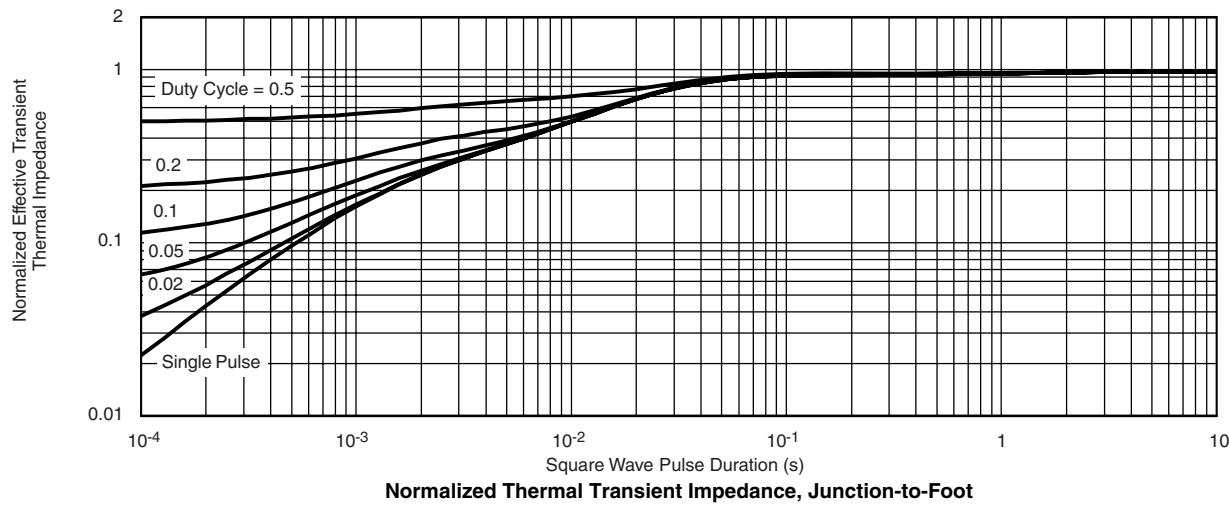
### Normalized Thermal Transient Impedance, Junction-to-Ambient



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**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



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