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Vishay/Siliconix SI2351DS-T1-E3

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### **Si2351DS**

Vishay Siliconix

# P-Channel 20-V (D-S) MOSFET

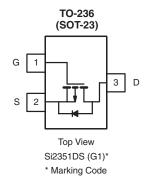
MOSFET PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)		
- 20	0.115 at V <sub>GS</sub> = - 4.5 V	- 3.0	3.2 nC		
	0.205 at V <sub>GS</sub> = - 2.5 V	- 2.2	3.2 110		

### **FEATURES**

- Halogen-free Option Available
- TrenchFET<sup>®</sup> Power MOSFET
- PWM Optimized
- 100 % R<sub>g</sub> Tested



COMPLIANT



Ordering Information: Si2351DS-T1-E3 (Lead (Pb)-free)

Si2351DS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS TA	= 25 °C, unless oth	erwise noted			
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V <sub>DS</sub>	- 20	V	
Gate-Source Voltage		$V_{GS}$	± 12	v	
	T <sub>C</sub> = 25 °C		- 2.8		
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C	l <sub>D</sub>	- 2.4		
Continuous Diani Guitent (1) = 100 C)	T <sub>A</sub> = 25 °C		- 2.2 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		- 1.8 <sup>b, c</sup>	Α	
Pulsed Drain Current		I <sub>DM</sub>	- 10		
	T <sub>C</sub> = 25 °C		- 2.0		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	- 0.91 <sup>b, c</sup>		
	T <sub>C</sub> = 25 °C		2.1		
Maximum Power Dissipation	T <sub>C</sub> = 70 °C	P <sub>D</sub>	1.5	W	
	T <sub>A</sub> = 25 °C	' D	1.0 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		0.7 <sup>b, c</sup>		
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, d</sup>	≤ 5 s	R <sub>thJA</sub>	90	115	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	60	75		

### Notes:

- a. Based on T<sub>C</sub> = 25 °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. Maximum under Steady State conditions is 130  $^{\circ}\text{C/W}.$

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Datasheet of SI2351DS-T1-E3 - MOSFET P-CH 20V 2.8A SOT23-3

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{DS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	- 20			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$			- 16.7		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = - 250 μA		2.1			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 0.6		- 1.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA	
Zara Cata Valtaga Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V			- 1	- 1 - 10 μA	
Zero Gate Voltage Drain Current		$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			- 10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	- 10			Α	
	<u> </u>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 2.4 A		0.092	0.115	Ω	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 1.8 A		0.164	0.205		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 2.4 A		5.5		S	
Dynamic <sup>b</sup>	•			•		<u>I</u>	
Input Capacitance	C <sub>iss</sub>			250		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz		80			
Reverse Transfer Capacitance	C <sub>rss</sub>			55			
Total Cata Chaves		V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 5.0 V, I <sub>D</sub> = - 2.4 A		3.4	5.1	nC	
Total Gate Charge	Qg			3.2	5		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -2.4 \text{ A}$		0.5			
Gate-Drain Charge	Q <sub>gd</sub>			1.4			
Gate Resistance	$R_{g}$	f = 1 MHz		8.5	13	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			9	14		
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 10 V, $R_{L}$ = 5.26 $\Omega$		30	45	- ns	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong -1.9 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_G = 1 \Omega$		32	48		
Fall Time	t <sub>f</sub>			16	24		
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 2.0		
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				- 10	- A	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = - 2.0 A		- 0.8	- 1.2	٧	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			17	26	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	1 - 20 A di/dt - 100 A/vo T - 05 °C		5	8	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = -2.0 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		14			
Reverse Recovery Rise Time	t <sub>b</sub>			3		ns	

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

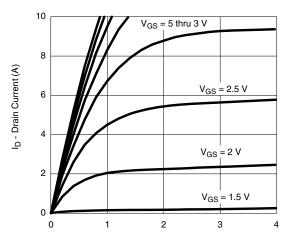




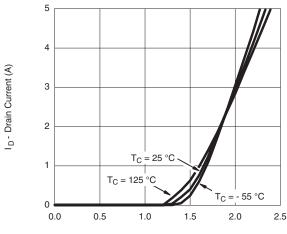
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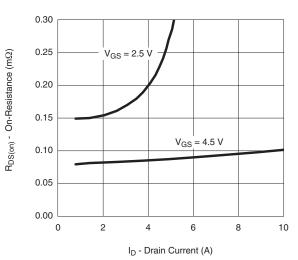
### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



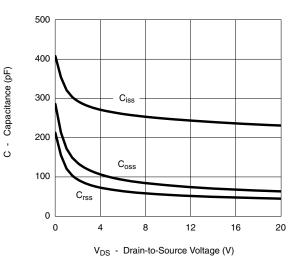
V<sub>DS</sub> - Drain-to-Source Voltage (V) **Output Characteristics** 



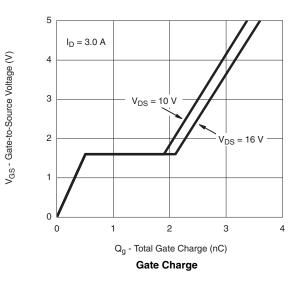
V<sub>GS</sub> - Gate-to-Source Voltage (V) **Transfer Characteristics** 

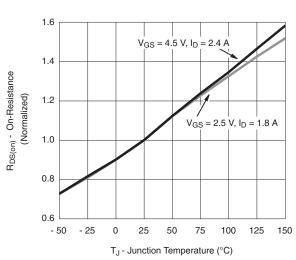


On-Resistance vs. Drain Current and Gate Voltage



Capacitance





On-Resistance vs. Junction Temperature

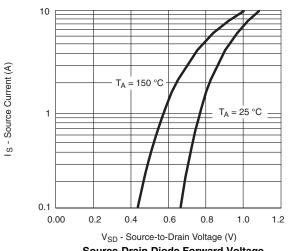
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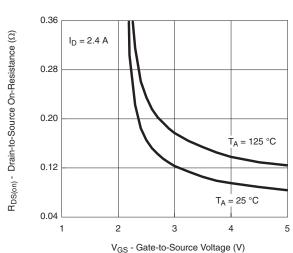


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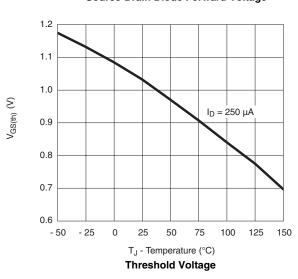
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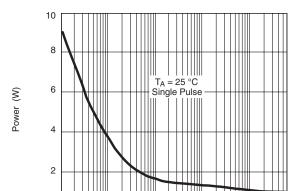
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Source-Drain Diode Forward Voltage





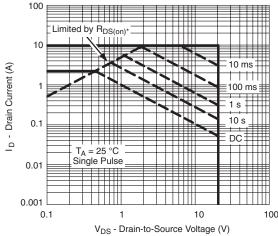
On-Resistance vs. Gate-to-Source Voltage

Time (s) Single Pulse Power

10

100

600



0

0.01

0.1

\*  $V_{GS} > \mbox{minimum } V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area

Datasheet of SI2351DS-T1-E3 - MOSFET P-CH 20V 2.8A SOT23-3

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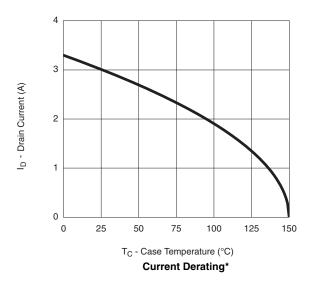


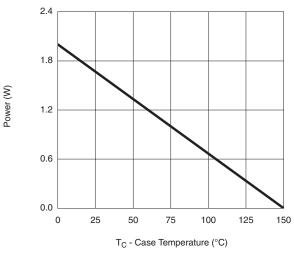
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### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





Power Derating, Junction-to-Foot

Document Number: 73702 S-80642-Rev. C, 24-Mar-08

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

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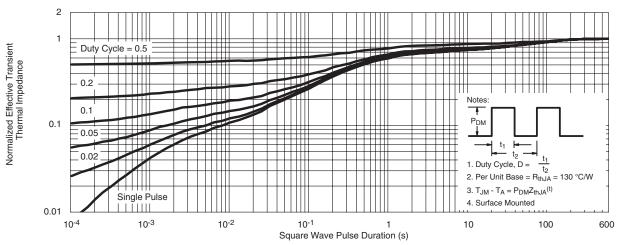
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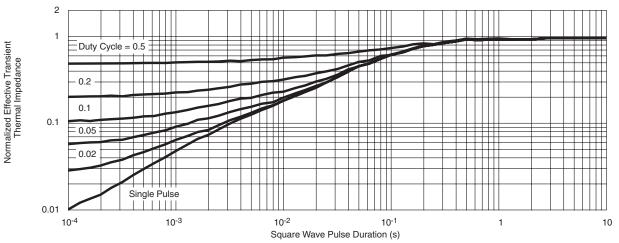
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### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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Datasheet of SI2351DS-T1-E3 - MOSFET P-CH 20V 2.8A SOT23-3

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