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Stocking Distributor

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Vishay/Siliconix
SI7120DN-T1-E3

For any questions, you can email us directly:
sales@integrated-circuit.com

# N-Channel 60-V (D-S) MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) | $I_D$ (A) |
| 60 | 0.019 at $V_{GS}$ = 10 V | 10 |
| | 0.028 at $V_{GS}$ = 4.5 V | 8.2 |

## FEATURES

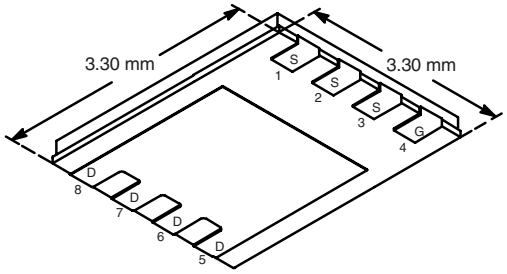
- **Halogen-free Option Available**
- TrenchFET® Power MOSFET
- New Low Thermal Resistance
- PowerPAK® 1212-8 Package with Low 1.07 mm Profile
- 100 % $R_g$ Tested

RoHS COMPLIANT

## APPLICATIONS

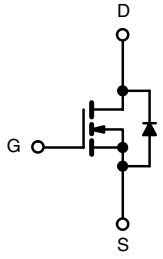
- Primary Side Switch
- Synchronous Rectification

**PowerPAK 1212-8**




Bottom View

**Ordering Information:** Si7120DN-T1-E3 (Lead (Pb)-free)
Si7120DN-T1-GE3 (Lead (Pb)-free and Halogen-free)




N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS $T_A$ = 25 °C, unless otherwise noted | | | | | |
|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **10 s** | **Steady State** | **Unit** |
| Drain-Source Voltage | | $V_{DS}$ | 60 | | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 20 | | |
| Continuous Drain Current ($T_J$ = 150 °C)[a] | $T_A$ = 25 °C | $I_D$ | 10 | 6.3 | A |
| | $T_A$ = 70 °C | | 8.0 | 5.1 | |
| Pulsed Drain Current | | $I_{DM}$ | 40 | | |
| Continuous Source Current (Diode Conduction)[a] | | $I_S$ | 3.2 | 1.3 | |
| Single Avalanche Current | L = 0 1 mH | $I_{AS}$ | 22 | | |
| Single Avalanche Energy | | $E_{AS}$ | 24 | | mJ |
| Maximum Power Dissipation[a] | $T_A$ = 25 °C | $P_D$ | 3.8 | 1.5 | W |
| | $T_A$ = 70 °C | | 2.4 | 1.0 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | - 55 to 150 | | °C |
| Soldering Recommendations (Peak Temperature)[b, c] | | | 260 | | |

| THERMAL RESISTANCE RATINGS | | | | | |
|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Typical** | **Maximum** | **Unit** |
| Maximum Junction-to-Ambient[a] | t ≤ 10 s | $R_{thJA}$ | 26 | 33 | °C/W |
| | Steady State | | 65 | 81 | |
| Maximum Junction-to-Case (Drain) | Steady State | $R_{thJC}$ | 1.9 | 2.4 | |

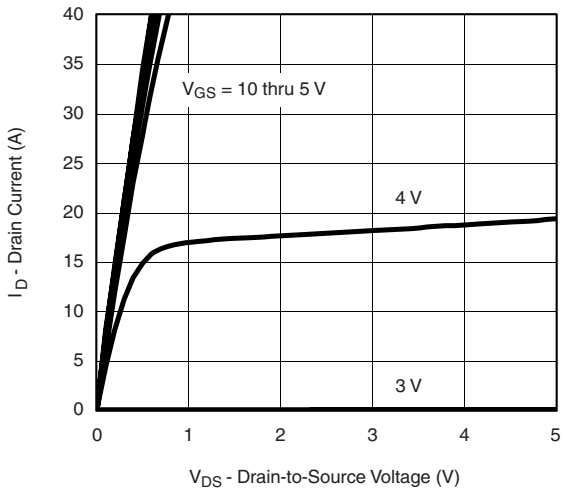
Notes:
a. Surface Mounted on 1" x 1" FR4 board.
b. See Solder Profile (*http://www.vishay.com/ppg?73257*). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

| **MOSFET SPECIFICATIONS** $T_J$ = 25 °C, unless otherwise noted | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1.5 | 2.5 | 3.5 | V |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 20 V | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V, $T_J$ = 55 °C | | | 5 | |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS}$ ≥ 5 V, $V_{GS}$ = 10 V | 30 | | | A |
| Drain-Source On-State Resistance[a] | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 10 A | | 0.015 | 0.019 | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 8.2 A | | 0.023 | 0.028 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 15 V, $I_D$ = 10 A | | 35 | | S |
| Diode Forward Voltage[a] | $V_{SD}$ | $I_S$ = 3.2 A, $V_{GS}$ = 0 V | | 0.78 | 1.2 | V |
| **Dynamic[b]** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 10 V, $V_{GS}$ = 10 V, $I_D$ = 10 A | | 30 | 45 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 6.9 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 5.8 | | |
| Gate Resistance | $R_g$ | | 0.65 | 1.3 | 1.95 | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 30 V, $R_L$ = 30 Ω<br>$I_D$ ≅ 1 A, $V_{GEN}$ = 10 V, $R_g$ = 6 Ω | | 14 | 25 | ns |
| Rise Time | $t_r$ | | | 12 | 20 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 50 | 80 | |
| Fall Time | $t_f$ | | | 12 | 20 | |
| Source-Drain Reverse Recovery Time | $t_{rr}$ | $I_F$ = 3.2 A, di/dt = 100 A/µs | | 60 | 100 | |

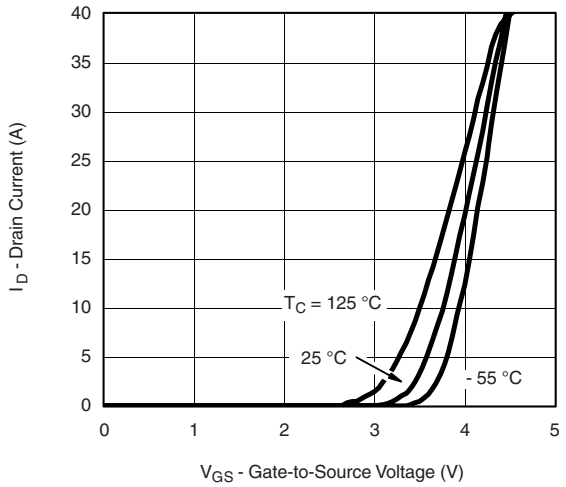
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

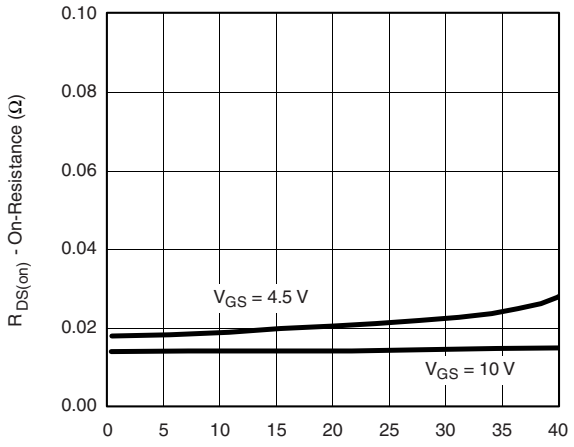



**Output Characteristics**

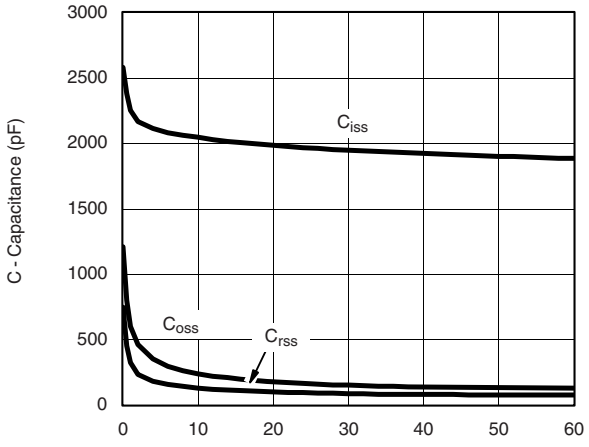



**Transfer Characteristics**

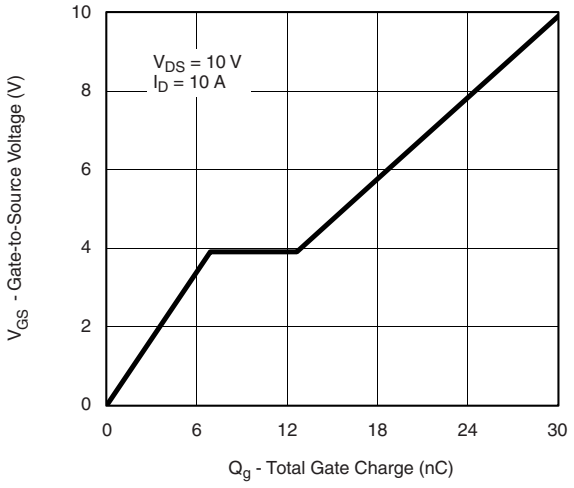
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



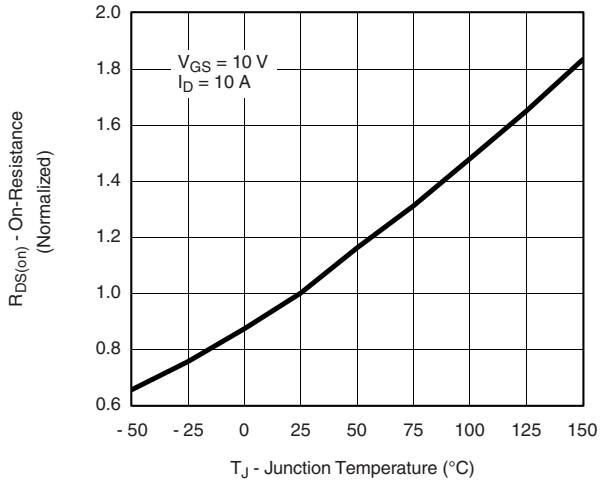

**On-Resistance vs. Drain Current**



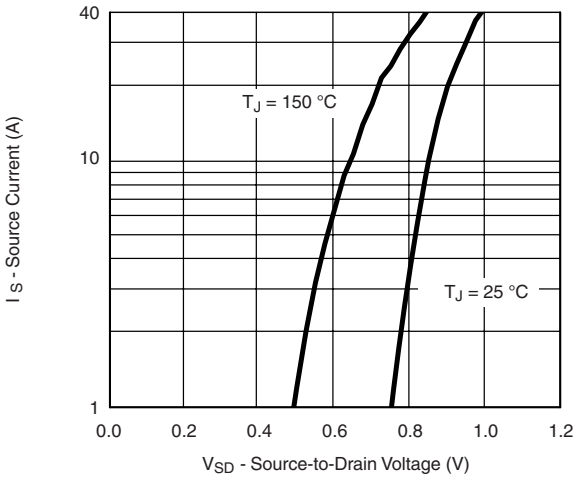

**Capacitance**



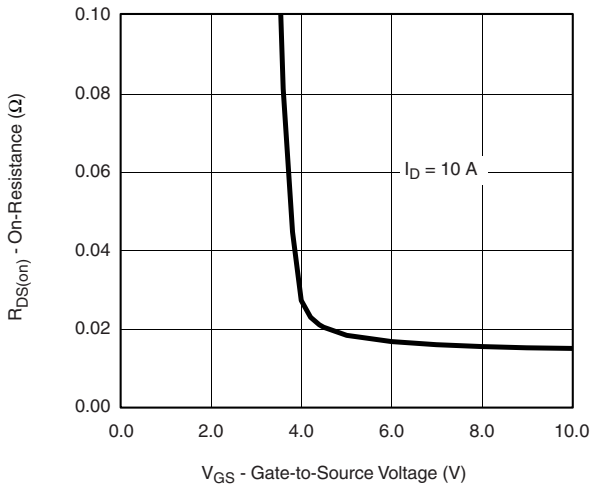

**Gate Charge**




**On-Resistance vs. Junction Temperature**

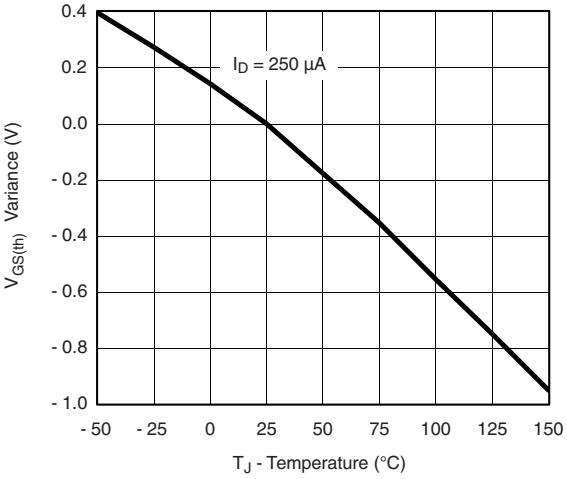



**Source-Drain Diode Forward Voltage**

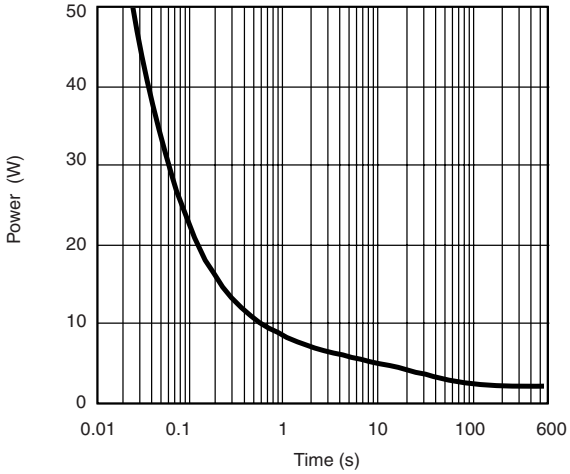



**On-Resistance vs. Gate-to-Source Voltage**

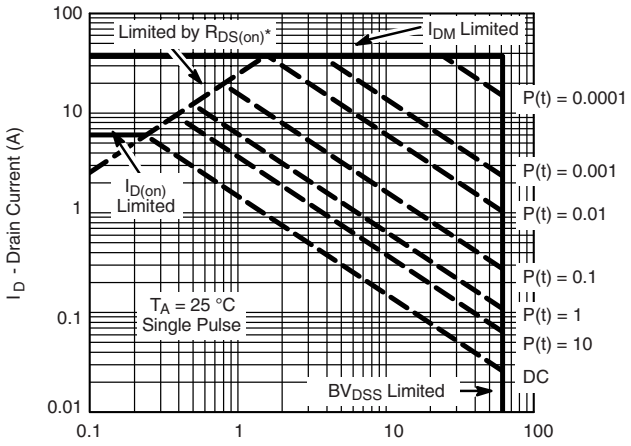
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted




**Threshold Voltage**

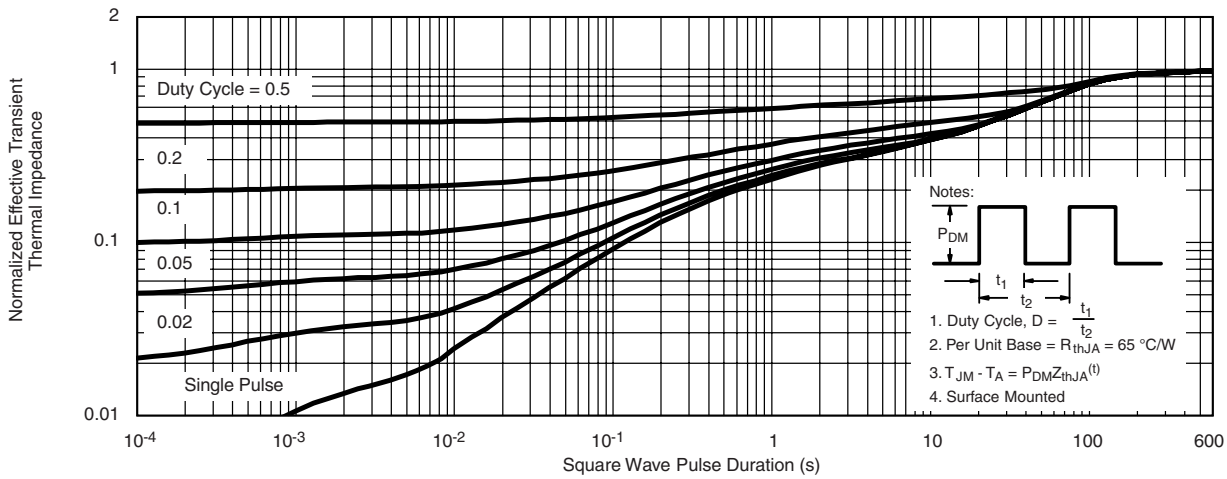



**Single Pulse Power, Junction-to-Ambient**



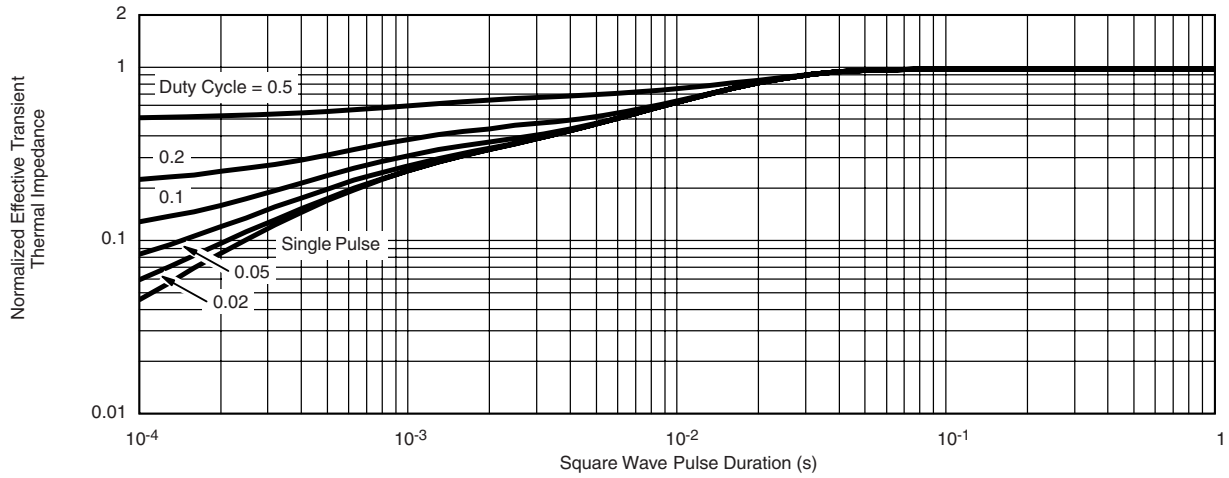

* $V_{GS}$ > minimum $V_{GS}$ at which $R_{DS(on)}$ is specified

**Safe Operating Area**




**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted




**Normalized Thermal Transient Impedance, Junction-to-Case**

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