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[SI7501DN-T1-E3](#)

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Si7501DN
Vishay Siliconix

Complementary 30-V (D-S) MOSFET

PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
P-Channel	- 30	0.051 at V _{GS} = - 10 V	- 6.4
		0.075 at V _{GS} = - 6 V	- 5.3
N-Channel	30	0.035 at V _{GS} = 10 V	7.7
		0.050 at V _{GS} = 4.5 V	6.5

FEATURES

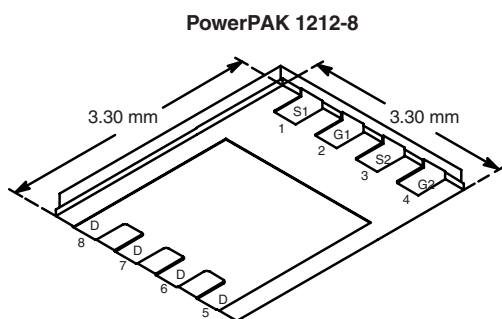
- Halogen-free Option Available
- TrenchFET® Power MOSFET
- New Low Thermal Resistance
- PowerPAK® Package with Low 1.07 mm Profile



RoHS
COMPLIANT

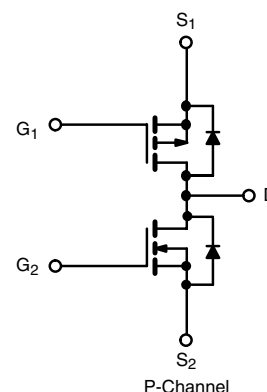
APPLICATIONS

- Backlight Inverter
- DC/DC Converter
- - 4 Cell Battery



Bottom View

Ordering Information: Si7501DN-T1-E3 (Lead (Pb)-free)
Si7501DN-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	P-Channel		N-Channel		Unit
			10 s	Steady State	10 s	Steady State	
Drain-Source Voltage		V _{DS}	- 30		30		V
Gate-Source Voltage		V _{GS}	± 25		± 20		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	- 6.4	- 4.5	7.7	5.4	A
	T _A = 70 °C		- 5.1	- 3.6	4.7	4.3	
Pulsed Drain Current		I _{DM}	- 25		25		
Continuous Source Current (Diode Conduction) ^a		I _S	- 2.6	- 1.3	2.6	1.3	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	3.1	1.6	3.1	1.6	W
	T _A = 70 °C		3	1.0	2	1.0	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150				°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260				

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	t ≤ 10 s	R _{thJA}	32	40	°C/W
	Steady State		65	81	
Maximum Junction-to-Foot (Case)	Steady State	R _{thJC}	5	6.3	

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- See Solder Profile (<http://www.vishay.com/ppg73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	- 1.0		- 3	V
		V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.0		3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 25 V	P-Ch			± 200	nA
		V _{DS} = 0 V, V _{GS} = ± 20 V	N-Ch			± 100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 30 V, V _{GS} = 0 V	P-Ch			- 1	μA
		V _{DS} = 30 V, V _{GS} = 0 V	N-Ch			1	
		V _{DS} = - 30 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch			- 5	
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ - 5 V, V _{GS} = - 10 V	P-Ch	- 25			A
		V _{DS} ≤ 5 V, V _{GS} = 10 V	N-Ch	25			
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 6.4 A	P-Ch		0.041	0.051	Ω
		V _{GS} = 10 V, I _D = 7.7 A	N-Ch		0.028	0.035	
		V _{GS} = - 6 V, I _D = - 5.3 A	P-Ch		0.055	0.075	
		V _{GS} = 4.5 V, I _D = 6.5 A	N-Ch		0.040	0.050	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 15 V, I _D = - 6.4 A	P-Ch		13		S
		V _{DS} = 15 V, I _D = 7.7 A	N-Ch		15		
Diode Forward Voltage ^a	V _{SD}	I _S = - 1.7 A, V _{GS} = 0 V	P-Ch		- 0.80	- 1.2	V
		I _S = 1.7 A, V _{GS} = 0 V	N-Ch		0.80	1.2	
Dynamic ^b							
Total Gate Charge	Q _g	P-Channel V _{DS} = - 15 V, V _{GS} = - 10 V, I _D = - 6.4 A	P-Ch		12.5	19	nC
Gate-Source Charge	Q _{gs}		N-Ch		9	14	
Gate-Drain Charge	Q _{gd}	N-Channel V _{DS} = 15 V, V _{GS} = 10 V, I _D = 7.7 A	P-Ch		2.5		
			N-Ch		2		
Gate Resistance	R _g		P-Ch		9		Ω
			N-Ch		3		
Turn-On Delay Time	t _{d(on)}	P-Channel V _{DD} = - 15 V, R _L = 5 Ω I _D ≅ - 3 A, V _{GEN} = - 10 V, R _G = 1 Ω	P-Ch		10	15	ns
Rise Time	t _r		N-Ch		10	15	
Turn-Off Delay Time	t _{d(off)}	N-Channel V _{DD} = 15 V, R _L = 5 Ω I _D ≅ 3 A, V _{GEN} = 10 V, R _G = 1 Ω	P-Ch		20	30	
			N-Ch		15	25	
Fall Time	t _f		P-Ch		25	40	
			N-Ch		20	30	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = - 1.7 A, dI/dt = 100 A/μs	P-Ch		30	45	
		I _F = 1.7 A, dI/dt = 100 A/μs	N-Ch		10	15	
					25	50	
					20	40	

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

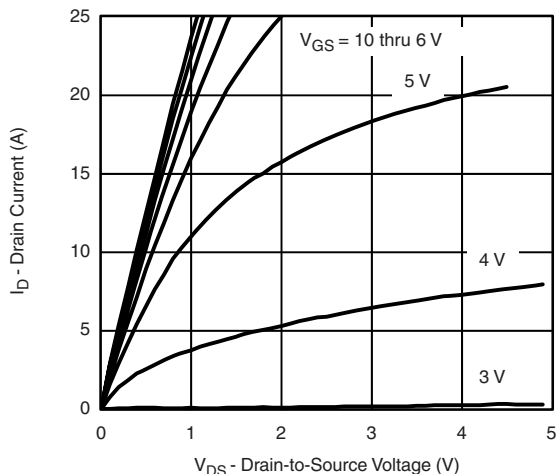
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



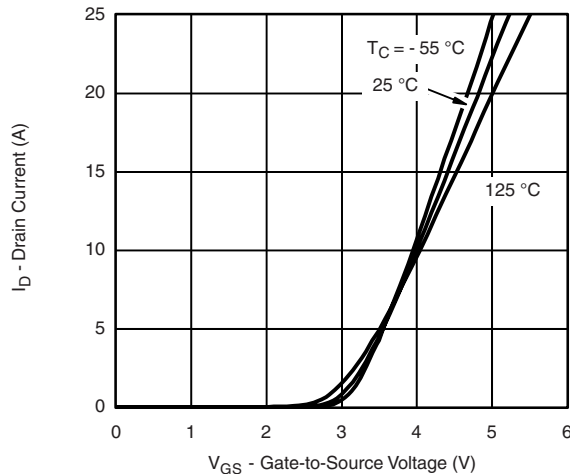
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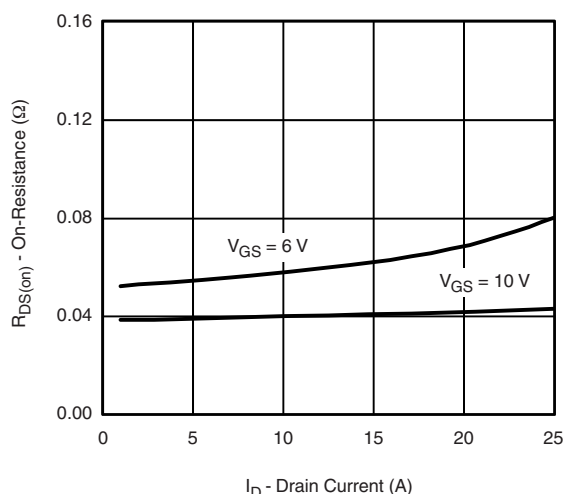
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



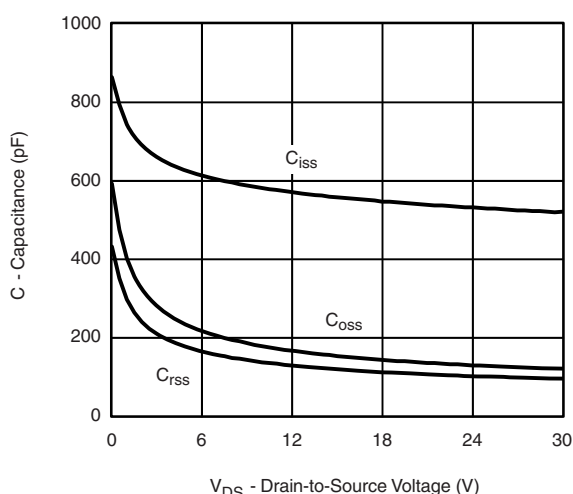
Output Characteristics



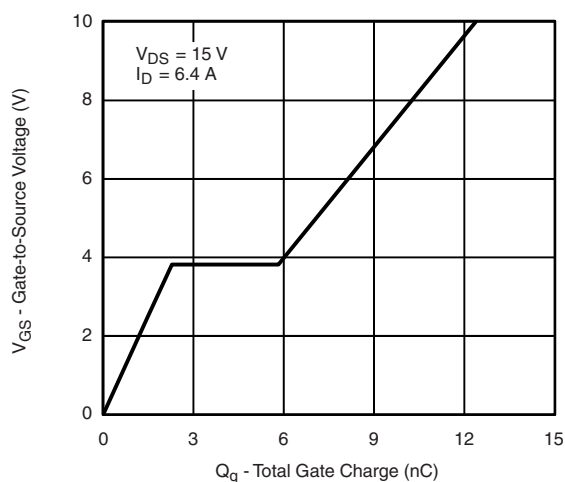
Transfer Characteristics



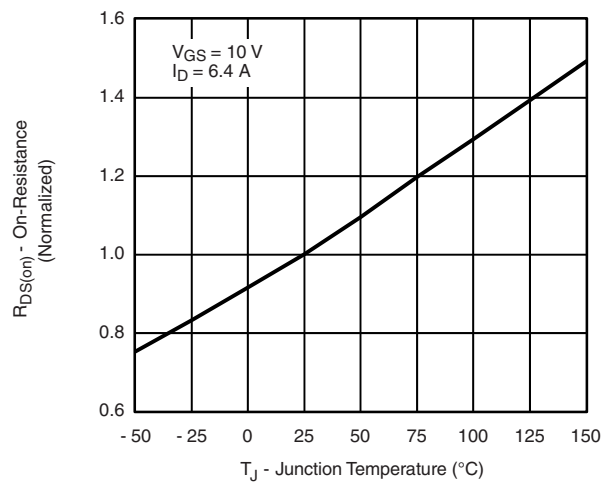
On-Resistance vs. Drain Current



Capacitance



Gate Charge



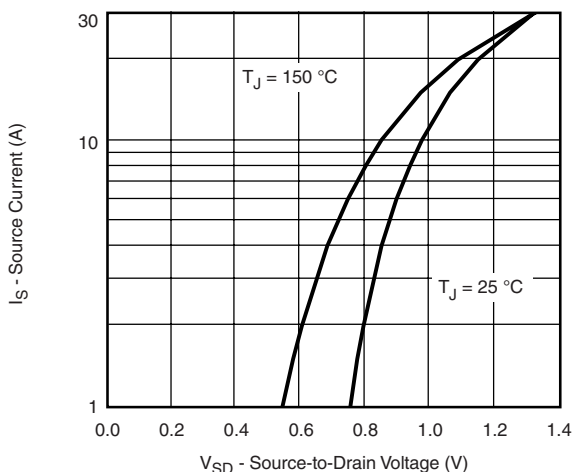
On-Resistance vs. Junction Temperature

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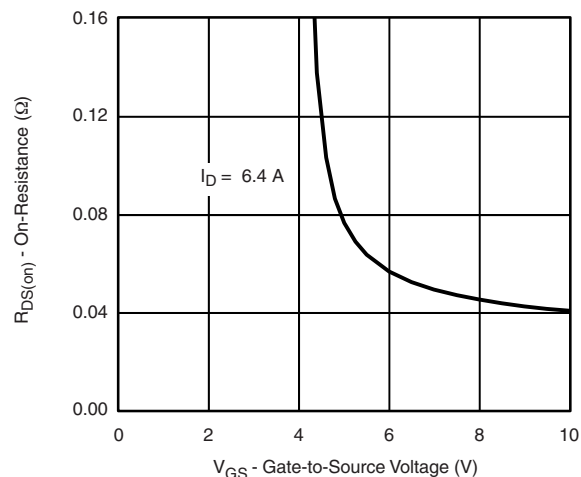
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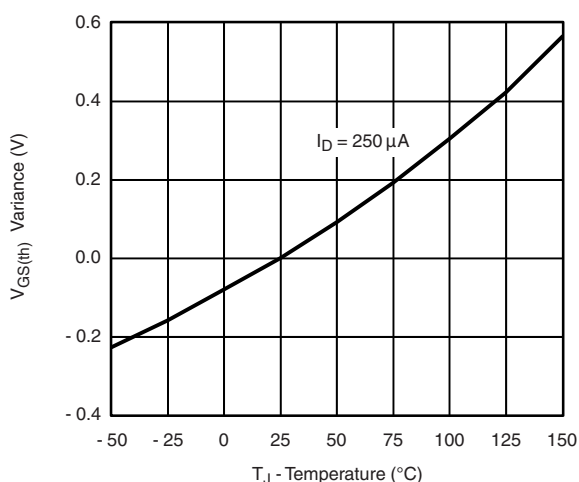
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



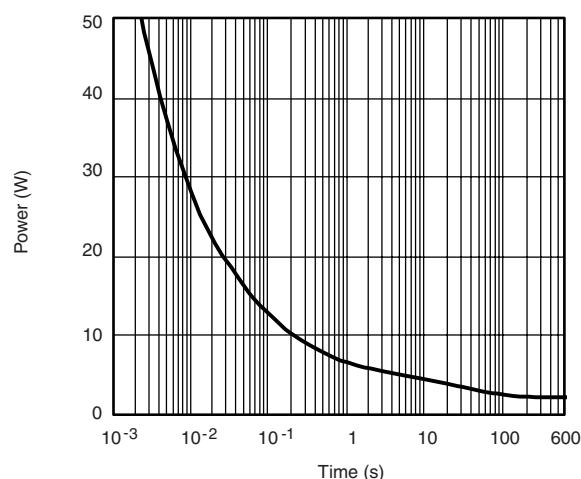
Source-Drain Diode Forward Voltage



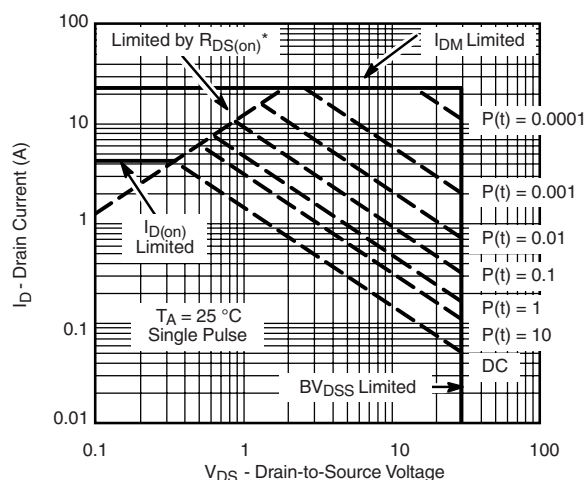
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

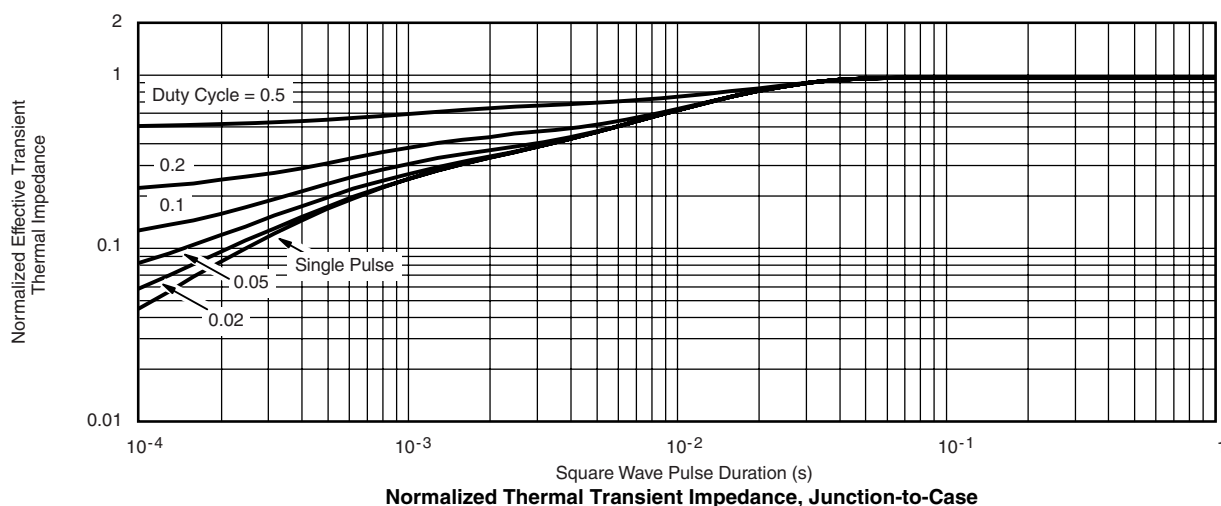
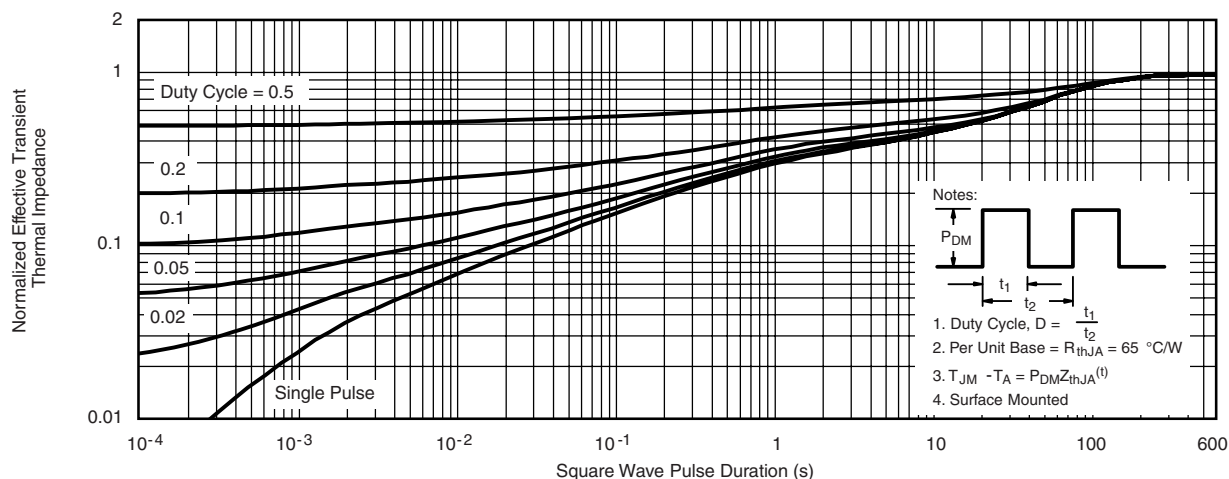
Safe Operating Area



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P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

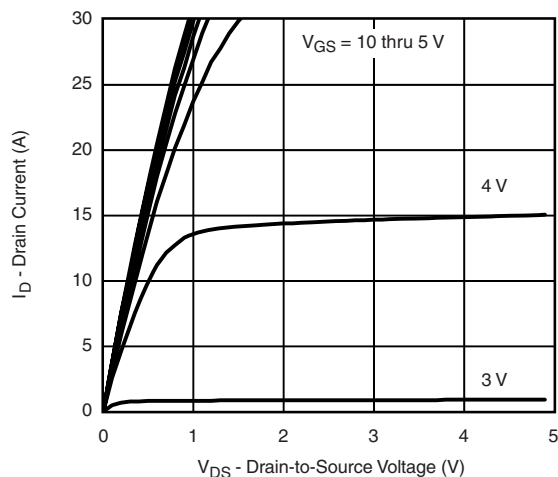


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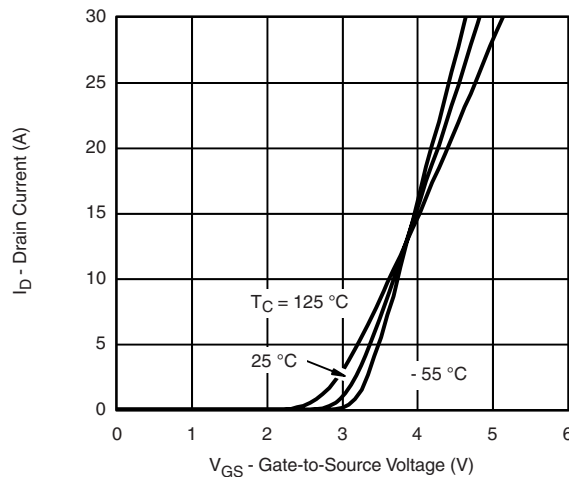
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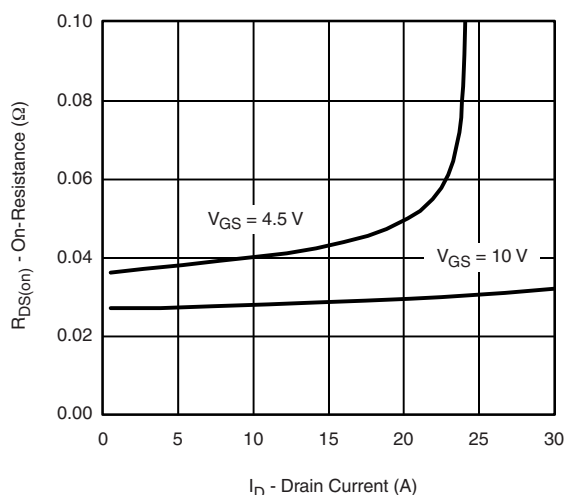
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



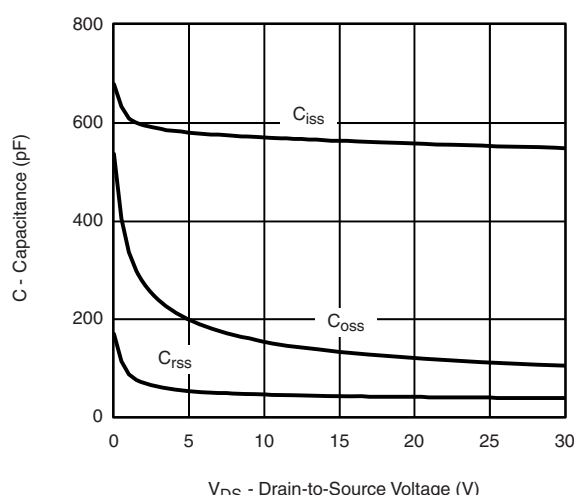
Output Characteristics



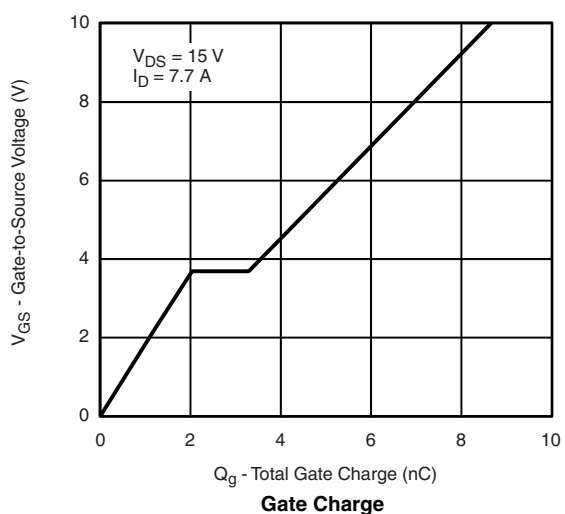
Transfer Characteristics



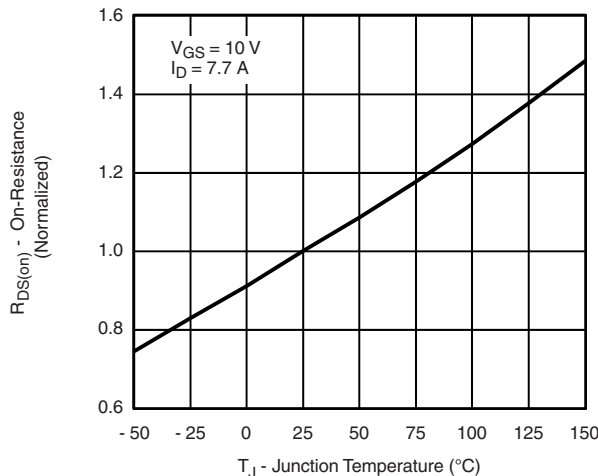
On-Resistance vs. Drain Current



Capacitance



Gate Charge



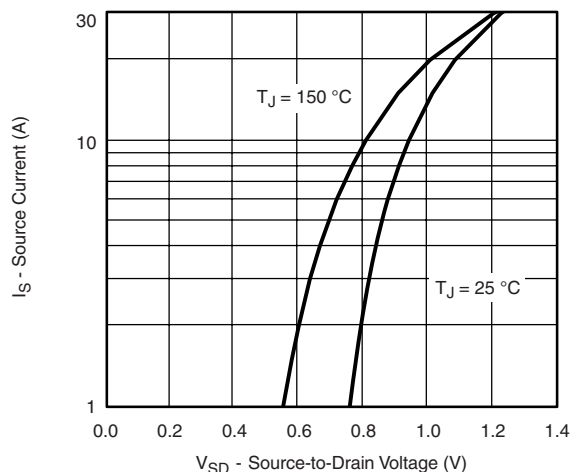
On-Resistance vs. Junction Temperature



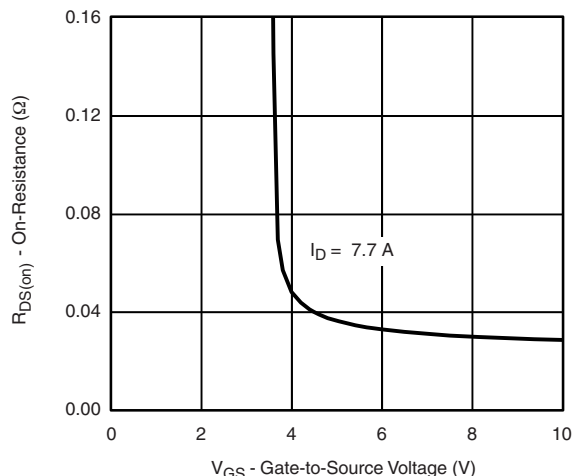
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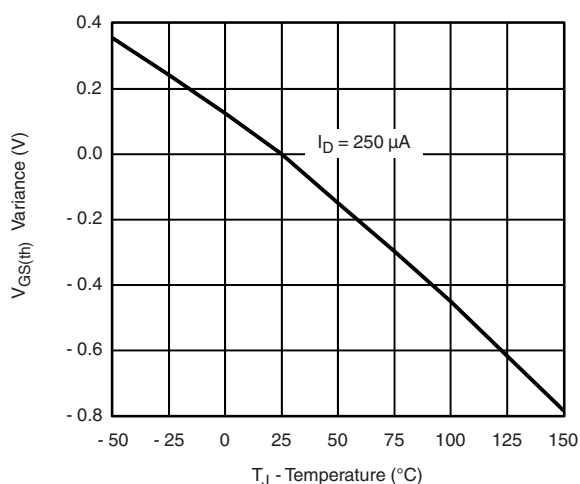
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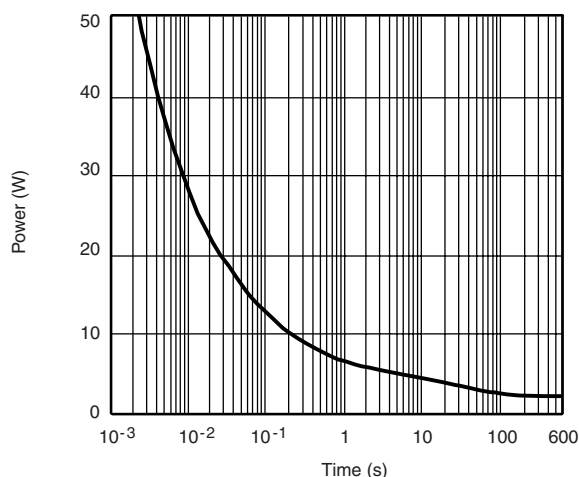
Source-Drain Diode Forward Voltage



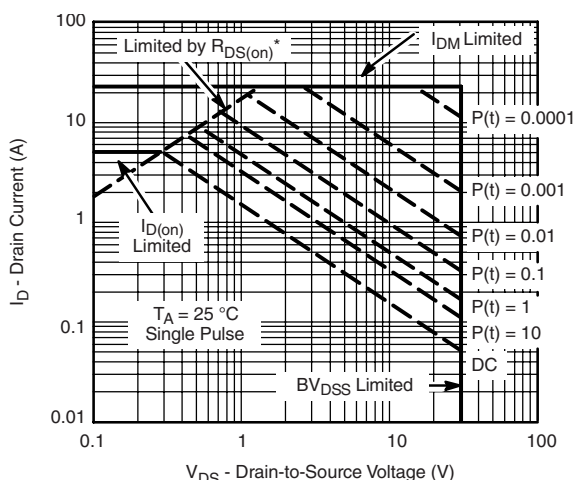
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

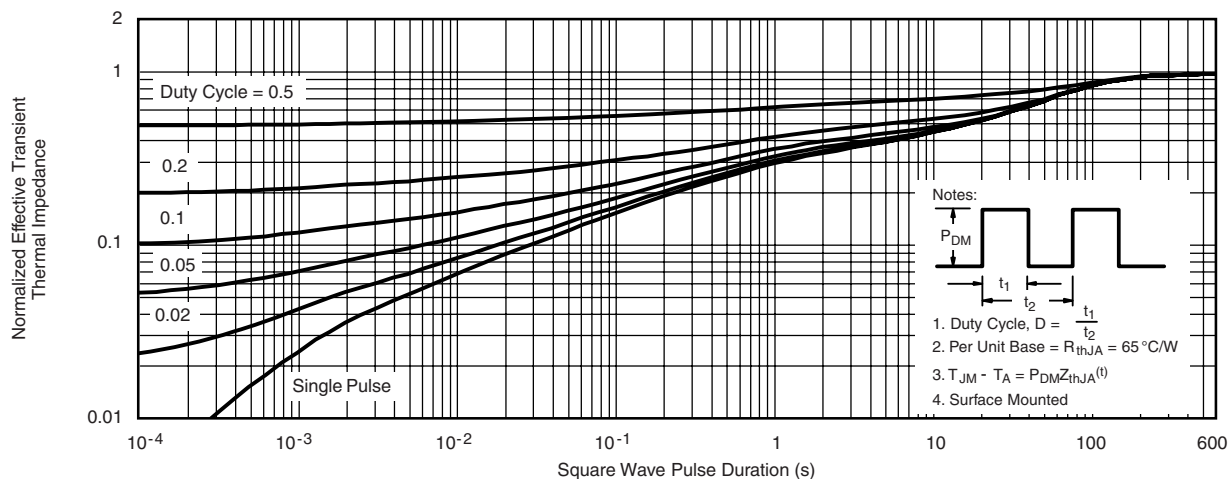
Safe Operating Area

Si7501DN

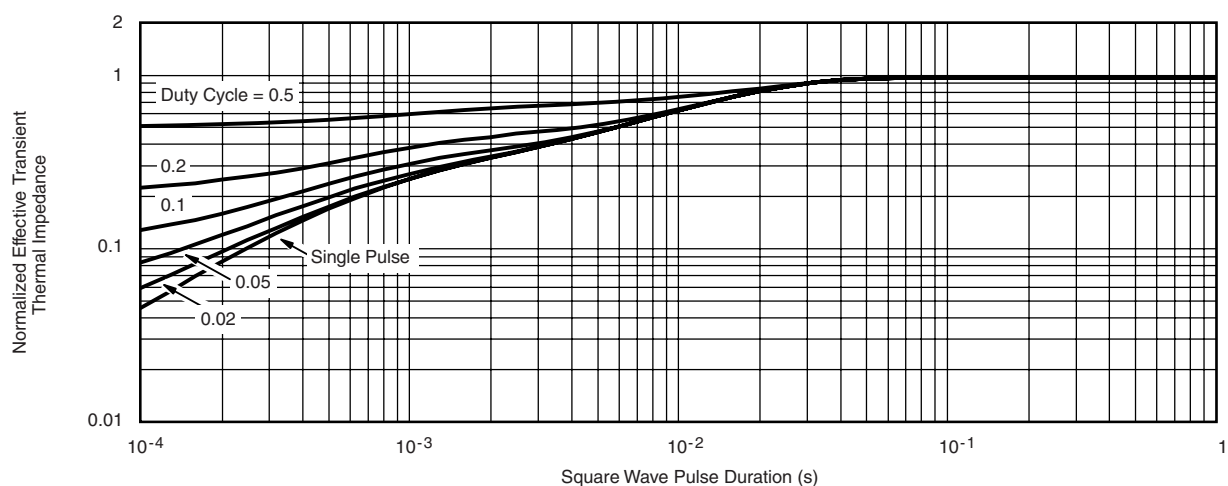
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N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72173>.



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