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[SN74LVTH245AIPWREP](#)

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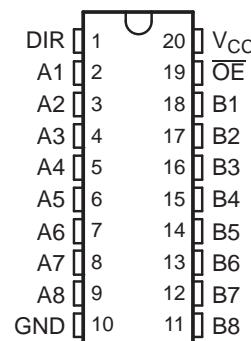
## FEATURES

- Controlled Baseline
  - One Assembly/Test Site, One Fabrication Site
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree <sup>(1)</sup>
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Supports Unregulated Battery Operation Down to 2.7 V
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

DB OR PW PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

This octal bus transceiver is designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device is designed for asynchronous communication between data buses. It transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## Device Components

## 3.3-V ABT OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCBS768A–NOVEMBER 2003–REVISED JUNE 2006



## ORDERING INFORMATION

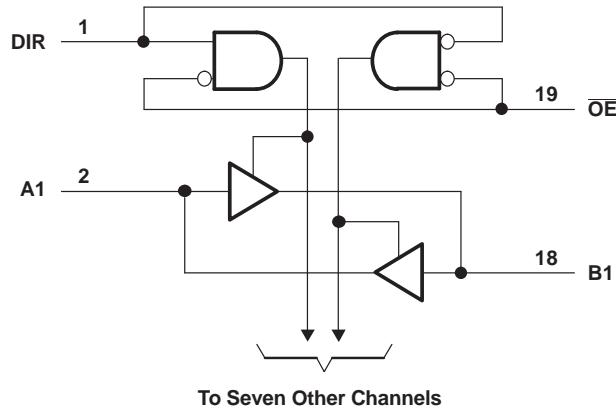
T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – PW	Tape and reel	SN74LVTH245AIPWREP	LH245AEP
-55°C to 125°C	SSOP – DB	Tape and reel	SN74LVTH245AMDBREP	LH245AMEP

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## LOGIC DIAGRAM (POSITIVE LOGIC)



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	–0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	–0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	–0.5	7	V
$V_O$	Voltage range applied to any output in the high state <sup>(2)</sup>	–0.5	$V_{CC} + 0.5$	V
$I_O$	Current into any output in the low state		128	mA
$I_O$	Current into any output in the high state <sup>(3)</sup>		64	mA
$I_{IK}$	Input clamp current	$V_I < 0$	–50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	–50	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DB package	69.5	°C/W
		PW package	83	
$T_{stg}$	Storage temperature range <sup>(5)</sup>	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See [http://www.ti.com/ep\\_quality](http://www.ti.com/ep_quality) for additional information on enhanced plastic packaging.

### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage		5.5	V
$I_{OH}$	High-level output current		–32	mA
$I_{OL}$	Low-level output current		64	mA
$\Delta t/\Delta V$	Input transition rise or fall rate	Outputs enabled	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200	μs/V
$T_A$	Operating free-air temperature	I temp	–40	85
		M temp	–55	125
				°C

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## SN74LVTH245A-EP

### 3.3-V ABT OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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#### Electrical Characteristics

over recommended operating free-air temperature ranges (I or M) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	M TEMP			I TEMP			UNIT
		MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 2.7 V, I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OH</sub> = -100 $\mu$ A	V <sub>CC</sub> - 0.2		V <sub>CC</sub> - 0.2				V
	V <sub>CC</sub> = 2.7 V, I <sub>OH</sub> = -8 mA	2.4		2.4				
	V <sub>CC</sub> = 3 V	I <sub>OH</sub> = -24 mA	2					
		I <sub>OH</sub> = -32 mA			2			
V <sub>OL</sub>	V <sub>CC</sub> = 2.7 V	I <sub>OL</sub> = 100 $\mu$ A		0.2			0.2	V
		I <sub>OL</sub> = 24 mA		0.5			0.5	
	V <sub>CC</sub> = 3 V	I <sub>OL</sub> = 16 mA		0.4			0.4	
		I <sub>OL</sub> = 32 mA		0.5			0.5	
		I <sub>OL</sub> = 48 mA		0.55				
		I <sub>OL</sub> = 64 mA					0.55	
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND		±1			±1	$\mu$ A
		V <sub>CC</sub> = 0 or 3.6 V, V <sub>I</sub> = 5.5 V		10			10	
	A or B port <sup>(2)</sup>	V <sub>I</sub> = 5.5 V		20			20	
		V <sub>I</sub> = V <sub>CC</sub>		1			1	
		V <sub>I</sub> = 0		-5			-5	
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 V to 4.5 V						±100	$\mu$ A
I <sub>I(hold)</sub>	A or B port	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0.8 V	75			75	$\mu$ A
			V <sub>I</sub> = 2 V	-75			-75	
		V <sub>CC</sub> = 3.6 V, <sup>(3)</sup>	V <sub>I</sub> = 0 V to 3.6 V				500 -750	
I <sub>OZPU</sub>	V <sub>CC</sub> = 0 to 1.5 V, V <sub>O</sub> = 0.5 V to 3 V, $\overline{OE}$ = don't care			±100			±100	$\mu$ A
I <sub>OZPD</sub>	V <sub>CC</sub> = 1.5 V to 0, V <sub>O</sub> = 0.5 V to 3 V, $\overline{OE}$ = don't care			±100			±100	$\mu$ A
I <sub>CC</sub>	V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
$\Delta I_{CC}$ <sup>(4)</sup>	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND			0.2			0.2	mA
C <sub>i</sub>	V <sub>I</sub> = 3 V or 0			4			4	pF
C <sub>o</sub>	V <sub>O</sub> = 3 V or 0			9			9	pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) Unused terminals are at V<sub>CC</sub> or GND.

(3) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

## Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	M TEMP				I TEMP				UNIT
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP <sup>(1)</sup>	MAX	MIN	MAX
$t_{PLH}$	A or B	B or A	1.2	5.5	6	1.2	2.3	3.5		4	ns
$t_{PHL}$			1.2	5.5	6	1.2	2.1	3.5		4	
$t_{PZH}$	$\overline{OE}$	A or B	1.3	7.9	9.5	1.3	3.2	5.5		7.1	ns
$t_{PZL}$			1.7	7	7.9	1.7	3.4	5.5		6.5	
$t_{PHZ}$	$\overline{OE}$	A or B	2.2	7.2	7.8	2.2	3.5	5.9		6.5	ns
$t_{PLZ}$			2.2	7.1	7.2	2.2	3.4	5		5.1	

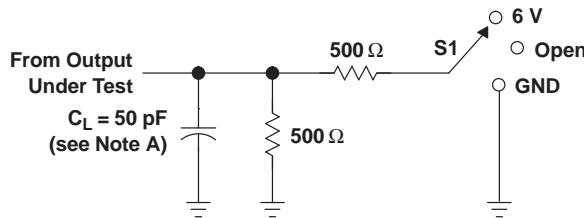
(1) All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## SN74LVTH245A-EP

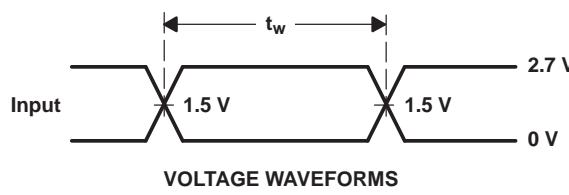
### 3.3-V ABT OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCBS768A—NOVEMBER 2003—REVISED JUNE 2006

### PARAMETER MEASUREMENT INFORMATION

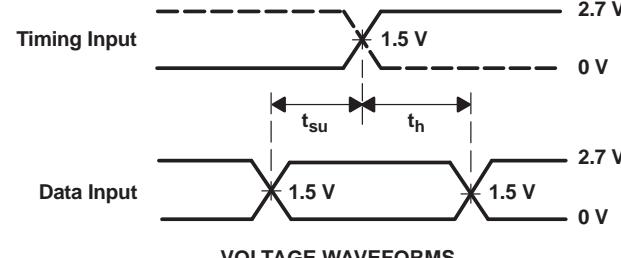


LOAD CIRCUIT

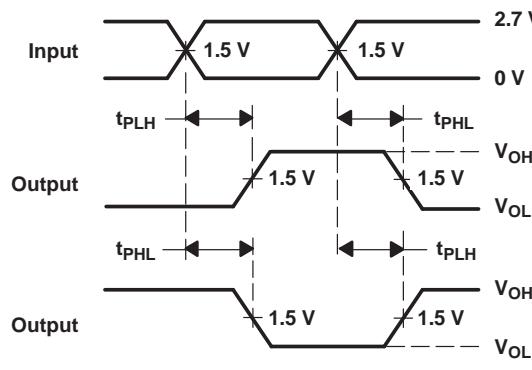


VOLTAGE WAVEFORMS  
PULSE DURATION

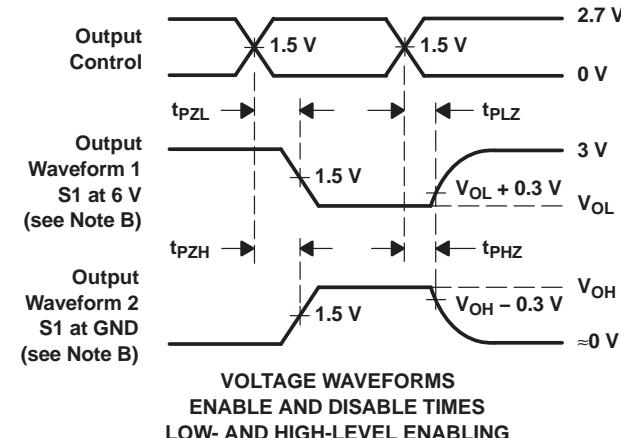
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LVTH245AIPWREP	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245AEP	<a href="#">Samples</a>
SN74LVTH245AMDBREP	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LH245AMEP	<a href="#">Samples</a>
V62/04723-01XE	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245AEP	<a href="#">Samples</a>
V62/04723-02YE	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LH245AMEP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN74LVTH245A-EP :**

• Catalog: [SN74LVTH245A](#)

• Military: [SN54LVTH245A](#)

NOTE: Qualified Version Definitions:

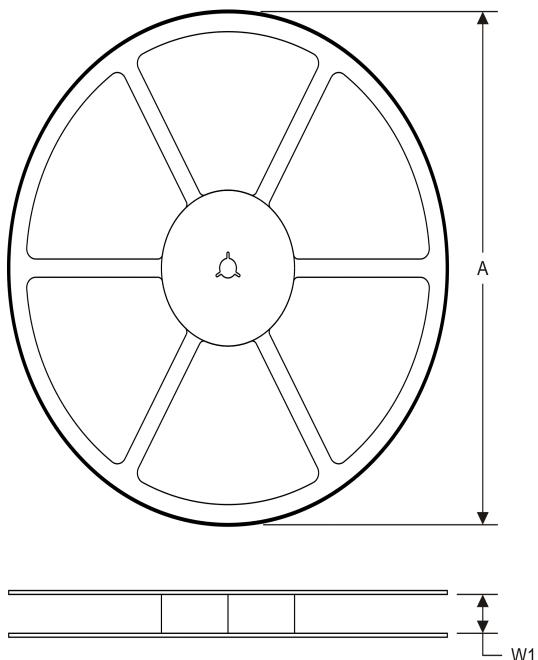
• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

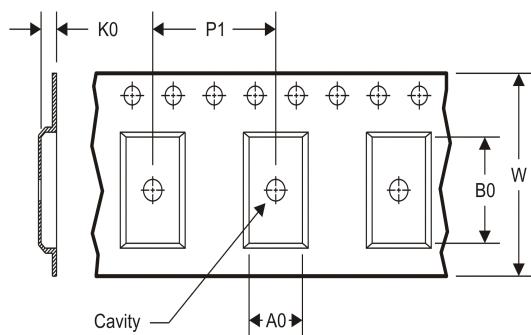
## PACKAGE MATERIALS INFORMATION

### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS



#### TAPE DIMENSIONS



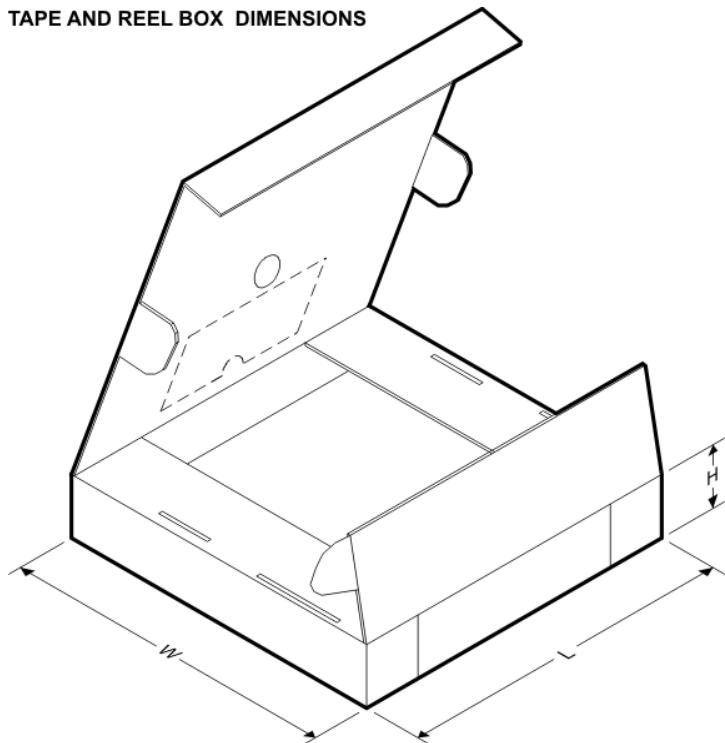
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### TAPE AND REEL INFORMATION

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH245AIPWREP	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVTH245AMDBREP	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



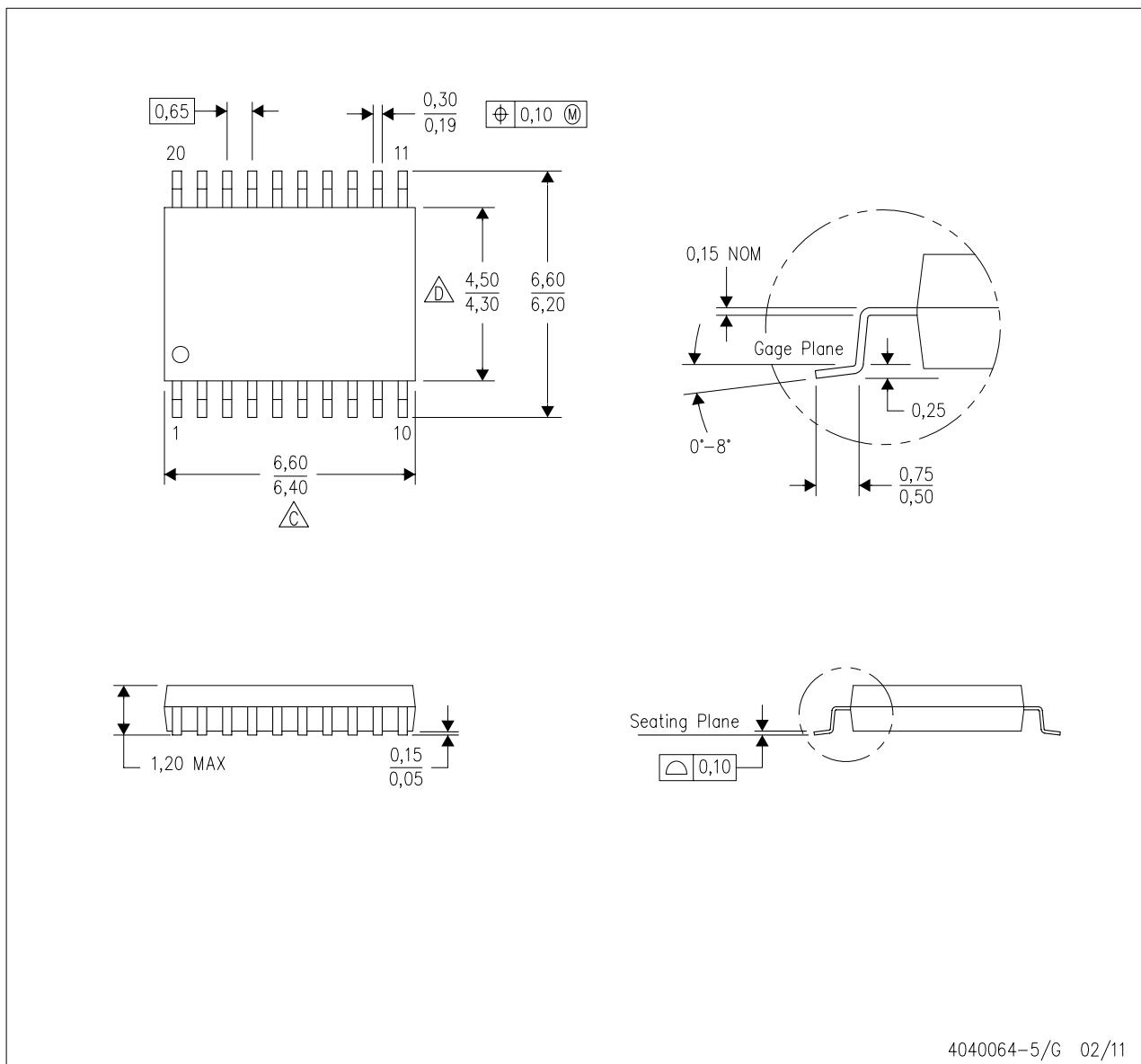
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH245AIPWREP	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74LVTH245AMDBREP	SSOP	DB	20	2000	367.0	367.0	38.0

## MECHANICAL DATA

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- Falls within JEDEC MO-153

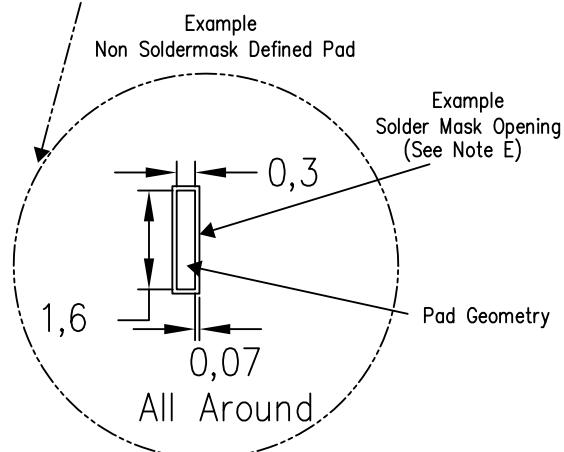
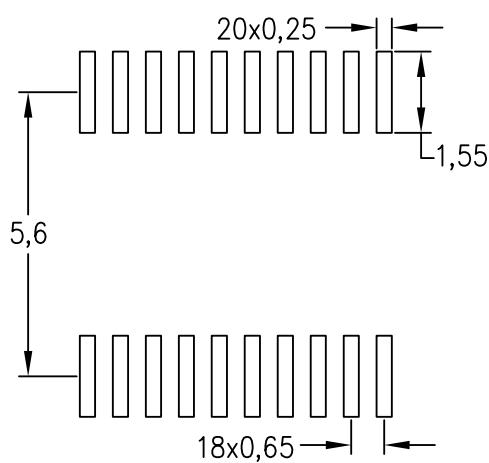
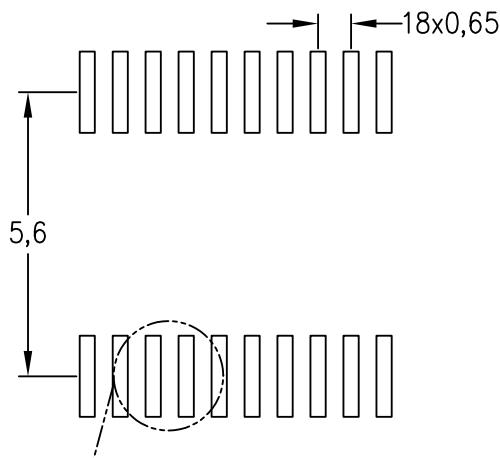
## LAND PATTERN DATA

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).



4211284-5/G 08/15

NOTES:

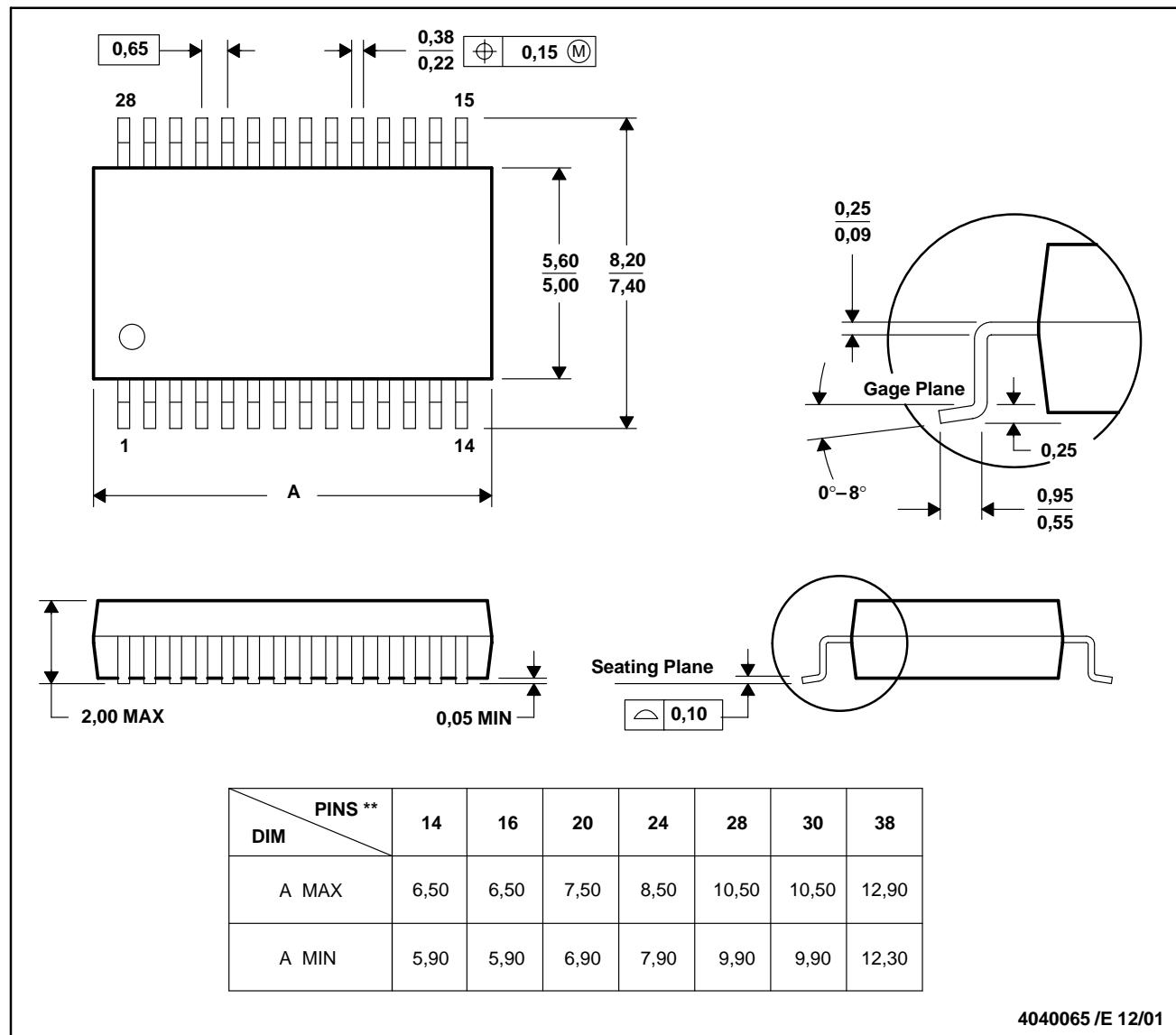
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSS002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G\*\*)**

28 PINS SHOWN

**PLASTIC SMALL-OUTLINE**



4040065 /E 12/01

**NOTES:**

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- Falls within JEDEC MO-150

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