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<u>Texas Instruments</u> <u>SN74LVTH543IPWREP</u>

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# **Distributor of Texas Instruments: Excellent Integrated System Limited**Datasheet of SN74LVTH543IPWREP - IC REGISTERED TRANSCVR 24TSSOP

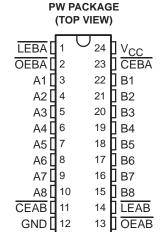
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### SN74LVTH543-EP 3.3-V ABT OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCBS772 - NOVEMBER 2003

- Controlled Baseline
  - One Assembly/Test Site, One Fabrication Site
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree†
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Supports Unregulated Battery Operation Down to 2.7 V
- I<sub>off</sub> and Power-Up 3-State Support Hot Insertion
- † Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)



### description/ordering information

This octal transceiver is designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The SN74LVTH543 contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register, to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the CEBA, LEBA, and OEBA inputs.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

### **ORDERING INFORMATION**

TA	PACK	AGE <sup>‡</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP - PW	Tape and reel	SN74LVTH543IPWREP	LH543EP

<sup>‡</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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### description/ordering information (continued)

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

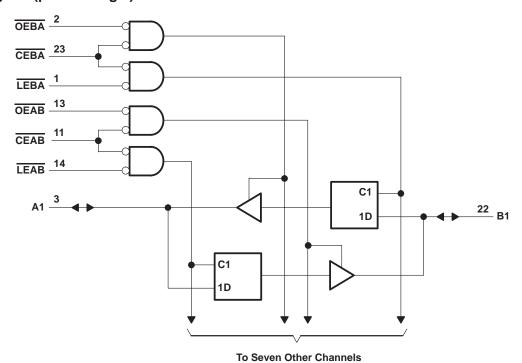
This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

#### **FUNCTION TABLE**†

	INPUTS									
CEAB	LEAB	OEAB	В							
Н	Χ	Х	Χ	Z						
Х	Χ	Н	Χ	Z						
L	Н	L	Χ	в <sub>0</sub> ‡						
L	L	L	L	L						
L	L	L	Н	Н						

<sup>†</sup> A-to-B data flow is shown; B-to-A flow control is the same, except that it uses CEBA, LEBA, and OEBA.

### logic diagram (positive logic)





<sup>‡</sup>Output level before the indicated steady-state input conditions were established



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance	
or power-off state, V <sub>O</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, VO (see Note 1)	0.5 V to $V_{CC}$ + 0.5 V
Current into any output in the low state, IO	128 mA
Current into any output in the high state, IO (see Note 2)	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Package thermal impedance, θ <sub>JA</sub> (see Note 3)	88°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 4)

		·	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
VIH	High-level input voltage		2		V
V <sub>IL</sub>	Low-level input voltage			8.0	V
VI	Input voltage			5.5	V
IOH	High-level output current			-32	mA
IOL	Low-level output current			64	mA
Δt/Δν	Input transition rise or fall rate Output	ıts enabled		10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200		μs/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.





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### SN74LVTH543-EP 3.3-V ABT OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITION	ONS	MIN	TYP <sup>†</sup>	MAX	UNIT
VIK		V <sub>CC</sub> = 2.7 V,	I <sub>I</sub> = -18 mA			-1.2	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V},$	I <sub>OH</sub> = -100 μA	V <sub>CC</sub> -0	.2		
Vон		$V_{CC} = 2.7 \text{ V},$	$I_{OH} = -8 \text{ mA}$	2.4			V
		V <sub>CC</sub> = 3 V,	$I_{OH} = -32 \text{ mA}$	2			
		V 27V	$I_{OL} = 100  \mu A$			0.2	
		V <sub>CC</sub> = 2.7 V	$I_{OL} = 24 \text{ mA}$			0.5	
VOL			$I_{OL} = 16 \text{ mA}$			0.4	V
		V <sub>CC</sub> = 3 V	$I_{OL} = 32 \text{ mA}$			0.5	
			$I_{OL} = 64 \text{ mA}$			0.55	
	Control inputs	$V_{CC} = 3.6 \text{ V},$	$V_I = V_{CC}$ or GND			±1	
	Control Inputs	V <sub>CC</sub> = 0 or 3.6 V,	V <sub>I</sub> = 5.5 V			10	
lį			V <sub>I</sub> = 5.5 V			20	μΑ
	A or B ports‡	V <sub>CC</sub> = 3.6 V	VI = VCC			1	
			V <sub>I</sub> = 0			-5	
l <sub>off</sub>		$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to 4.5 V			±100	μΑ
		V	V <sub>I</sub> = 0.8 V	75			
l(hold)	A or B ports	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 2 V	-75			μΑ
		V <sub>CC</sub> = 3.6 V§	$V_{I} = 0 \text{ to } 3.6 \text{ V}$			±500	
lozpu		$V_{CC} = 0$ to 1.5 V, $V_O = 0.5$ to 3 V, $\overline{OE} = don$				±100	μΑ
lozpd		$V_{CC} = 1.5 \text{ V to } 0, V_O = 0.5 \text{ to } 3 \text{ V}, \overline{OE} = \text{don}$	't care			±100	μΑ
			Outputs high			0.19	
ICC		$V_{CC} = 3.6 \text{ V}, I_O = 0, V_I = V_{CC} \text{ or GND}$	Outputs low			5	mA
			Outputs disabled			0.19	
∆ICC¶		$V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6	V, Other inputs at V <sub>CC</sub> or GND			0.2	mA
Ci		V <sub>I</sub> = 3 V or 0			4		pF
C <sub>io</sub>		V <sub>O</sub> = 3 V or 0			9		pF

<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .



<sup>‡</sup>Unused terminals are at V<sub>CC</sub> or GND.

<sup>§</sup> This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.



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# timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				V <sub>CC</sub> =		VCC =	UNIT	
				MIN	MAX	MIN	MAX	
t <sub>W</sub>	Pulse duration,	LEAB or LEBA low	I	3.3		3.3		ns
		A or B before	Data high	0.4		0.4		
١.	Catus times	LEAB or LEBA↑	Data low	1		1.5		
t <sub>su</sub>	Setup time	A or B before		0.2		0.2		ns
		CEAB or CEBA↑	Data low	0.7		1.2		
		A or B after	Data high	1.5		0.6		
4.	Hold time	LEAB or LEBA↑ D		1.3		1.5		ns
th	noid title	A or B after CEAB or CEBA↑		1.6		0.5		
				1.4		1.6		

# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO		± 0.3 V	V	V <sub>CC</sub> =	UNIT	
	(INPUT)	(OUTPUT)	MIN	TYP†	MAX	MIN	MAX	
t <sub>PLH</sub>	A D	D A	1.3	2.5	3.7		4.3	
t <sub>PHL</sub>	A or B	B or A	1.3	2.5	3.7		4.3	ns
t <sub>PLH</sub>	副	A D	1.3	2.9	4.7		5.9	
t <sub>PHL</sub>	LE	A or B	1.3	2.9	4.7		5.9	ns
<sup>t</sup> PZH	<u>OE</u>	A or D	1.1	2.9	4.9		6.2	20
t <sub>PZL</sub>	OE	A or B	1.1	3.2	4.9		6.2	ns
<sup>t</sup> PHZ	<u>O</u> E	A B	2	3.4	5.3		5.9	
tPLZ	OE	A or B	2	3.7	5.3		5.9	ns
<sup>t</sup> PZH	CE	A or B	1.3	3.2	5.3		6.8	20
t <sub>PZL</sub>	CE	A or B	1.3	3.5	5.3		6.8	ns
<sup>t</sup> PHZ	CE	A or B	2.3	3.8	5.4		5.9	ns
tPLZ	SE	AUID	2.3	3.9	5.4		5.6	115

 $<sup>\</sup>uparrow$  All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

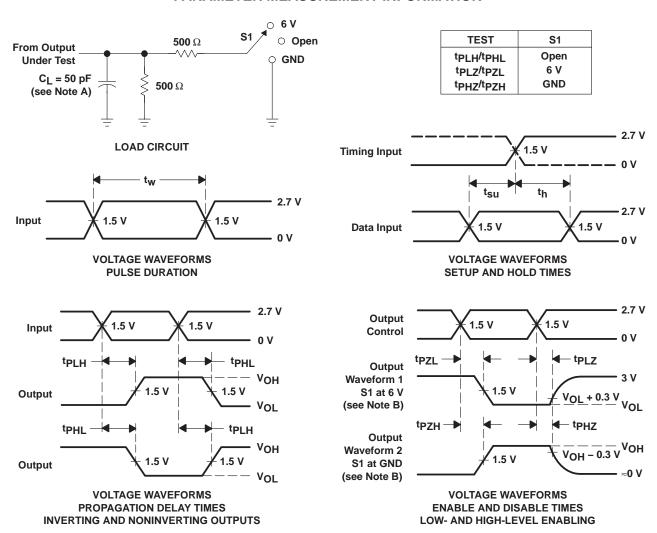


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### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \,\Omega$ ,  $t_r \leq 2.5 \,$  ns.  $t_t \leq 2.5 \,$  ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





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### PACKAGE OPTION ADDENDUM

18-Sep-2008

### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins F	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVTH543IPWREP	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04677-01XE	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in

a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Catalog: SN74LVTH543

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

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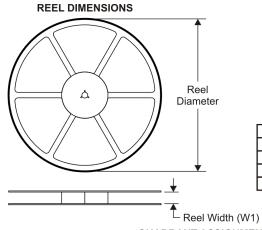
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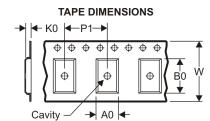
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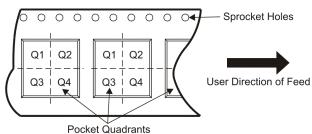
### TAPE AND REEL INFORMATION





A0 Dimension	
AU DIMENSION	designed to accommodate the component width
B0 Dimension	designed to accommodate the component length
K0 Dimension	designed to accommodate the component thickness
W Overall wid	Ith of the carrier tape
P1 Pitch between	een successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

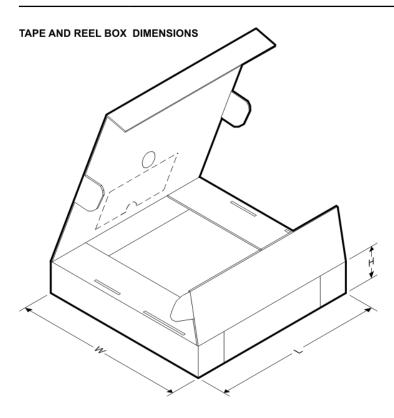
Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH543IPWREP	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH543IPWREP	TSSOP	PW	24	2000	346.0	346.0	33.0



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