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Texas Instruments
CD74HC08QM96Q1

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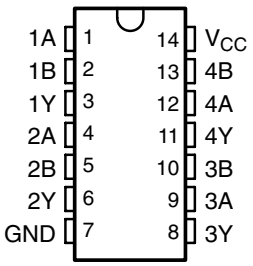
CD74HC08-Q1
QUADRUPLE 2-INPUT POSITIVE-AND GATE

SCLS512A – JULY 2003 – REVISED FEBRUARY 2008

- **Qualified for Automotive Applications**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Buffered Inputs**
- **Typical Propagation Delay 7 ns at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . 15 LSTTL Loads**
- **Extended Temperature Performance of –40°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction, Compared to LSTTL Logic ICs**
- **2-V to 6-V V_{CC} Operation**
- **High Noise Immunity N_{IL} or N_{IH} = 30% of V_{CC} at V_{CC} = 5 V**
- **CMOS Input Compatibility, $I_I \leq 1\ \mu A$ at V_{OL}, V_{OH}**

M PACKAGE
(TOP VIEW)



description/ordering information

The CD74HC08 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates, with the low power consumption of standard CMOS integrated circuits. The device can drive 10 LSTTL loads.

ORDERING INFORMATION†

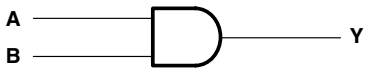
T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – M	Tape and reel	CD74HC08QM96Q1	HC08Q

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O > –0.5$ or $V_O < V_{CC} + 0.5$ V) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 180°C/W
Maximum junction temperature, T_J . . . . . 150°C
Lead temperature (during soldering):
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max . . . . . 300°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature		–40		125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

EIS electronic components
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I_O (mA)	V_{CC}	T_A = 25°C			CD74HC08-Q1		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	−0.02	2 V	1.9			1.9		V
			−0.02	4.5 V	4.4			4.4		
			−0.02	6 V	5.9			5.9		
		TTL loads	−4	4.5 V	3.98			3.7		
			−5.2	6 V	5.48			5.2		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	0.02	2 V			0.1		0.1	V
			0.02	4.5 V			0.1		0.1	
			0.02	6 V			0.1		0.1	
		TTL loads	4	4.5 V			0.26		0.4	
			5.2	6 V			0.26		0.4	
I_I	$V_I = V_{CC}$ or GND			6 V			±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND		0	6 V			2		40	µA
C_i							10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	V_{CC}	T_A = 25°C			CD74HC08-Q1		UNIT
					MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	C_L = 50 pF	2 V			90		135	ns
				4.5 V			18		27	
				6 V			15		23	
			C_L = 15 pF	5 V		7				
t_t		Y	C_L = 50 pF	2 V			75		110	ns
				4.5 V			15		22	
				6 V			13		19	

operating characteristics, T_A = 25°C, V_{CC} = 5V

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate (see Note 4)	No load	37	pF

NOTE 4: C_{pd} is used to determine the dynamic power consumption, per gate.
$P_D = V_{CC}^2 f_I (C_{pd} + C_L)$
f_I = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

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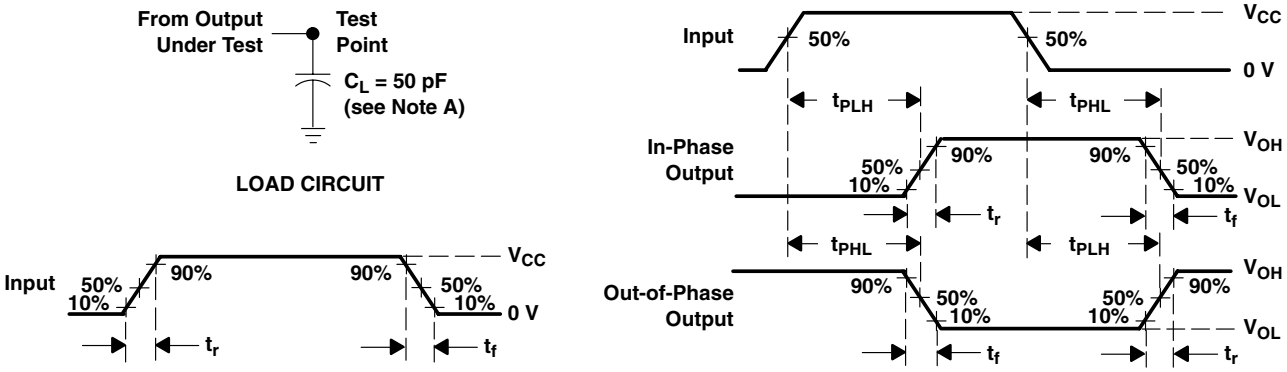
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC08QM96Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC08Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD74HC08-Q1 :

- Catalog: CD74HC08
- Enhanced Product: CD74HC08-EP
- Military: CD54HC08

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

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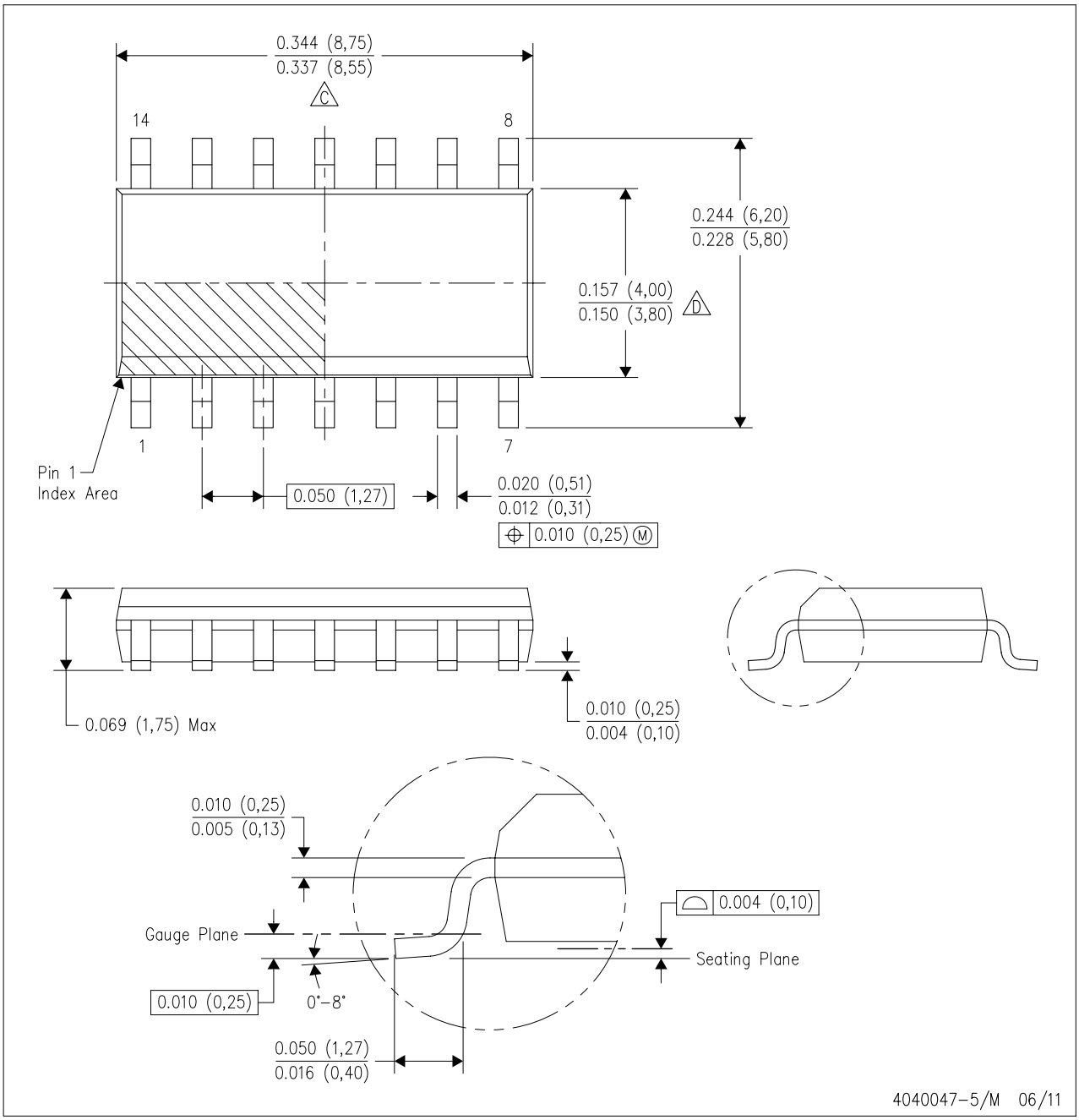
MECHANICAL DATA

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

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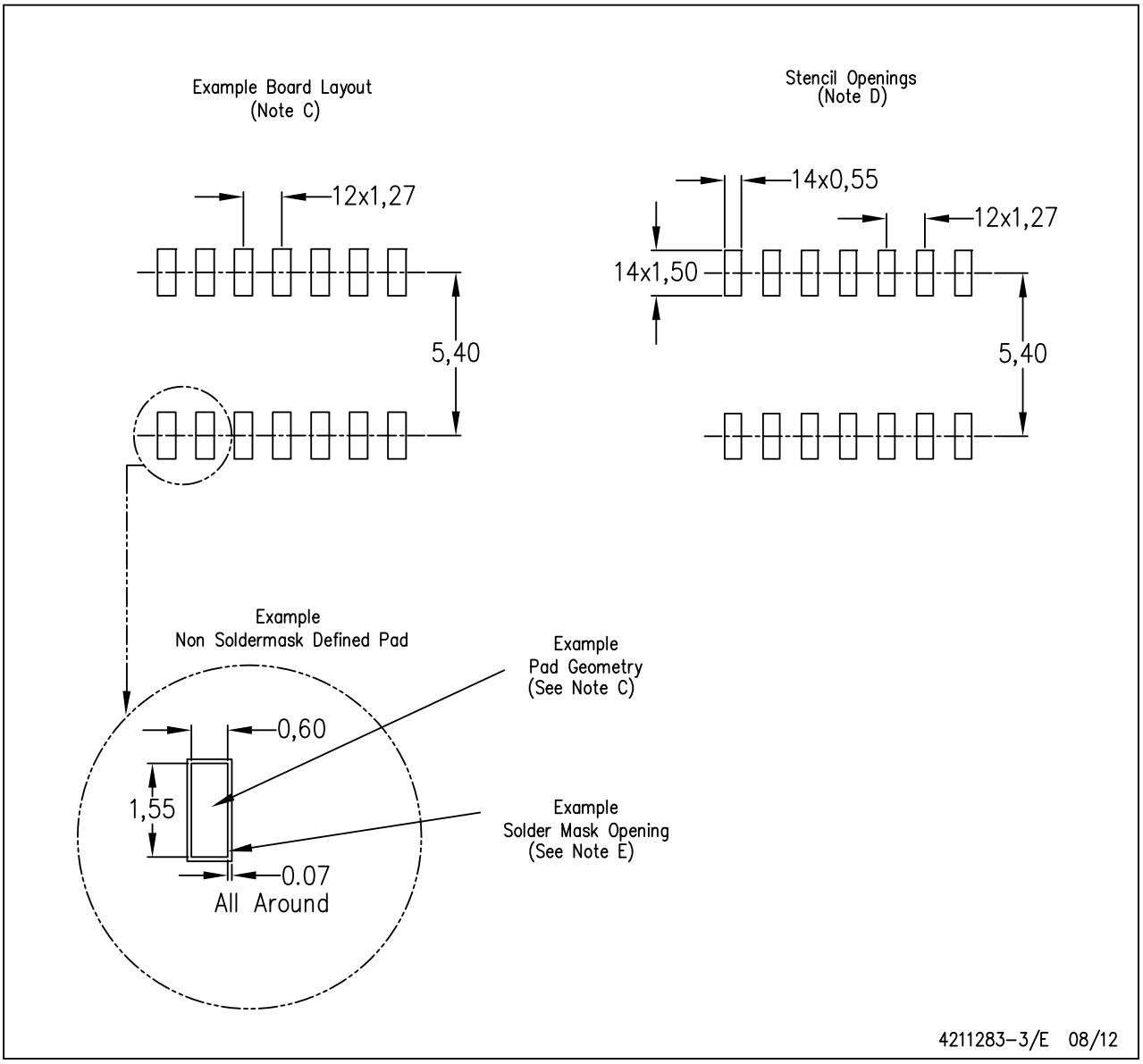
LAND PATTERN DATA

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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