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20 A Evaluation Board for Step-Down DC-to-DC Controller

EVAL-ADP1828HC

EVALUATION BOARD DESCRIPTION

This data sheet describes the design, operation, and test results of the 20 A ADP1828 evaluation board. The input range for this evaluation board is 6 V to 18 V, and the output voltage is 1.8 V with a maximum load current of 20 A. For this design, a switching frequency (f_{SW}) of 300 kHz is chosen to achieve a good balance between efficiency and the sizes of the power components.

ADP1828 DEVICE DESCRIPTION

The ADP1828 is a synchronous PWM voltage mode buck controller. It drives an all N-channel power stage to regulate an output voltage as low as 0.6 V to 85% of the input voltage and is sized to handle large MOSFETs for point-of-load regulators. The ADP1828 is ideal for a wide range of high power applications, such as DSP and processor core I/O power, as well as general-purpose power in telecommunications, medical imaging, PC, gaming, and industrial applications. It operates from an input voltage of 3 V to 18 V with an internal LDO that generates a 5 V output for a V_{IN} of 5.5 V to 18 V.

The ADP1828 operates at a pin-selectable, fixed switching frequency of either 300 kHz or 600 kHz, or at any frequency between 300 kHz and 600 kHz if a resistor is used. The frequency can also be synchronized to an external clock up to 2× the switching frequency. The clock output can be used for synchronizing the ADP1828 or another part, such the ADP1829, thus eliminating the need for an external clock source. The ADP1828 includes soft start protection (to limit inrush current from the input supply during startup), reverse current protection during soft start for a precharged output, voltage tracking, power good, as well as an adjustable lossless current-limit scheme utilizing external MOSFET sensing. The ADP1828 is offered in a 20-lead QSOP package.

DIGITAL PICTURE OF THE BOARD

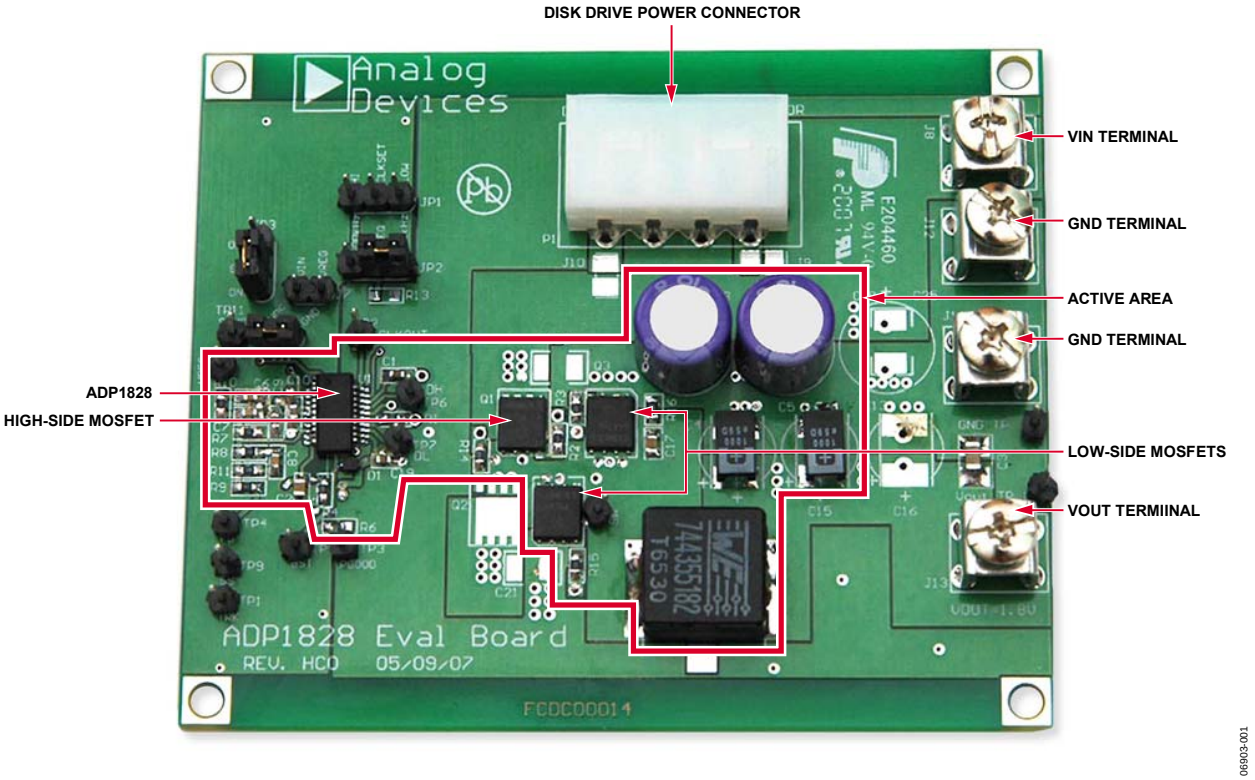

Figure 1.

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REVISION HISTORY

8/07—Revision 0: Initial Version

COMPONENT DESIGN

For information in selecting power components and calculating component values, see the ADP1828 data sheet.

INDUCTOR SELECTION

For this design, a 0.82 µH inductor with a 27 A saturation current rating (744355182 from Würth Elektronik Group) is selected. This is a compact flat-wire inductor with a ferrite core, which offers high performance in terms of low R_{DC} and low core loss.

INPUT CAPACITOR

For input voltages up to 18 V and a load up to 20 A, 35 V multilayer ceramic capacitors (MLCCs) can be used. However, the 35 V MLCCs are expensive and many of them are needed. An alternative solution is to use the inexpensive aluminum electrolytic capacitors, but they are fairly large and bulky and have large ESR at low temperatures. Another alternative is to use the OS-CON™ polymer capacitors from Sanyo or the equivalent from another manufacturer because such capacitors offer a relative small size, low ESR, and high current ripple rating.

For this design, if the input voltage is 18 V and the inductor is 0.82 µH, the inductor current ripple is calculated to be about 6.6 A. The current rating of the input capacitors must be greater than 6.6 A. Two OS-CON capacitors, 20SP180M (180 µF/20 V, each with 4.28 A ripple rating), connected in parallel provides an effective ripple rating of 8.56 A and satisfies this requirement.

OUTPUT CAPACITOR SELECTION

The output voltage ripple can be approximated as follows:

$$\Delta V_{OUT} = \Delta I_L \sqrt{ESR^2 + \left(\frac{1}{8 f_{SW} C_{OUT}}\right)^2 + (4 f_{SW} ESL)^2} \quad (1)$$

where:
ΔV_{OUT} is the output ripple voltage.
ΔI_L is the inductor ripple current.
ESR is the equivalent series resistance of the output capacitor.
ESL is the equivalent series inductance of the output capacitor.

MLCCs can be used in this design. However, for a 20 A step load, a large bulk capacitance (approximately 1000 µF) is required to suppress the current ripple. Using ten 100 µF MLCCs is an expensive solution. An alternative solution is to use the aluminum electrolytic OS-CON polymer or the POSCAP™ polymer capacitors. Because of the small footprint, low height, and low ESR of POSCAP capacitors, they have been selected for the output capacitors in this design.

A minimum capacitance at the output is needed to achieve a fast load-step response and reasonable overshoot voltage. The minimum capacitance can be calculated as

$$C_{OUT,min1} = \frac{\Delta I_{LOAD}{}^2 L}{2 V_{OUT} \Delta V_{up}} \quad (2)$$

$$C_{OUT,min2} = \frac{\Delta I_{LOAD}{}^2 L}{2(V_{IN} - V_{OUT}) \Delta V_{down}} \quad (3)$$

where:
ΔI_{LOAD} is the step load.
ΔV_{up} is the output voltage overshoot when the load is stepped down.
ΔV_{down} is the output voltage overshoot when the load is stepped up.
V_{IN} is the input voltage.
$C_{OUT,min1}$ is the minimum capacitance according to the overshoot voltage ΔV_{up}.
$C_{OUT,min2}$ is the minimum capacitance according to the overshoot voltage ΔV_{down}.

Select an output capacitance that is greater than both $C_{OUT, min1}$ and $C_{OUT, min2}$.

Two 1000 µF POSCAP capacitors, 2R5TPD1000M5 (100 µF/2.5 V with 5 mΩ and 6 A current ripple rating), and one 47 µF MLCC have been chosen for the output to satisfy a 20 A step load. These two POSCAP capacitors connected in parallel yield an effective current ripple rating of 12 A. The POSCAP capacitors suppress the large current ripples, and the 47 µF MLCC suppresses the high frequency ripples.

MOSFET SELECTION

In general, select the high-side MOSFET with fast rise and fall times and with low input capacitance. The fast rise and fall times are especially important for circuits with low duty cycles because switching loss is high. Select the low-side MOSFET with low R_{DSON}. Switching speed is not critical because there is no switching loss in the low-side MOSFET. A small amount of power is lost in the body diode of the low-side MOSFET during the dead time.

For this design, the duty cycle range is from 10% to 30% (V_{IN} = 6 V to 18 V); therefore, finding a high-side MOSFET with fast switching and low input capacitance and a low-side MOSFET with low R_{DSON} is critical. The BSC080N03LS from Infineon Technologies in the PG-TDSON-8, or Super-SO8 (comparable to the PowerPAK® SO-8 from Vishay Silliconix), package offers high performance in terms of fast rise and fall times (3 ns), low input capacitance (1.2 nF), and low R_{DSON} (12 mΩ at V_{GS} = 4.5 V), making it a great selection for the high-side MOSFET in this 20 A application. As for the low-side MOSFETs, two BSC030N03LS from Infineon Technologies connected in parallel are adequate to handle the power dissipation. The BSC030N03LS has a low R_{DSON} of 4.7 mΩ at a V_{GS} of 4.5 V.

Power MOSFETs in DPAK packages can also be used. Although DPAK has low thermal resistance, it has higher parasitic inductance than the PowerPAK, which may cause excessive ringing at the SW node and contribute to lower efficiency at heavy loads.

SOFT START

The soft start period is given by the following equation:

$$C_{SS} = 8.015 \times t_{SS} \quad (4)$$

where:
C_{SS} is the soft start capacitance in microfarads.
t_{SS} is the soft start period in seconds.

A C_{SS} of 150 nF, which yields a 19 ms soft start period, is chosen for this design.

CURRENT LIMIT

The external current-limit resistor can be calculated by the following equation:

$$R_{CL} = \frac{\left(I_{LIMIT} + \frac{\Delta I_L}{2}\right) R_{DSON} - 38\text{ mV}}{42\ \mu\text{A}} \quad (5)$$

where:
I_{LIMIT} is the output limit current.
ΔI_L is the ripple current in the inductor.
R_{DSON} is the on resistance of the low-side MOSFET.
−38 mV is the CSL threshold voltage.

ΔI_L can be approximated by

$$\Delta I_L = \frac{V_{OUT}(1-D)}{f_{SW} \times L} \quad (6)$$

where:
D is the duty cycle.
L is the inductance of the inductor.

In this design, R_{DSON} of the MOSFET BSC030N03LS is 4.7 mΩ at a V_{GS} of 4.5 V. Two BSC030N03LS MOSFETs in parallel yields an effective R_{DSON} of 2.35 mΩ. Because L is chosen to be 0.82 µH, ΔI_L is calculated to be 6.6 A with a V_{IN} of 18 V. If I_{LIMIT} is set to 25 A, R_{CL} is calculated to be 1.33 kΩ. Keep in mind that the R_{DSON} of the MOSFET can vary by more than 25% from part to part, and by more than 50% over the temperature range; therefore, the actual current limit can vary by more than 50% from part to part over the temperature range. For more information on this topic or if accurate current-limit sensing is needed, see the ADP1828 data sheet.

SWITCHING NOISE AND OVERSHOOT REDUCTION

An RC snubber can be added between SW and PGND to reduce noise and ringing at the SW node and at the drains of the external MOSFETs. In this design, an RC snubber is added with an R_{SNUB} of 3.01 Ω and a C_{SNUB} of 1.2 nF. Gate resistors can be added to reduce overshoot voltage at the drains of the MOSFETs. For more information, see the ADP1828 data sheet.

COMPENSATION DESIGN

Type III compensation is used in this design because each of the output POSCAP capacitors has a low ESR of 5 mΩ. For information on calculating the compensation component values, refer to the ADP1828 data sheet.

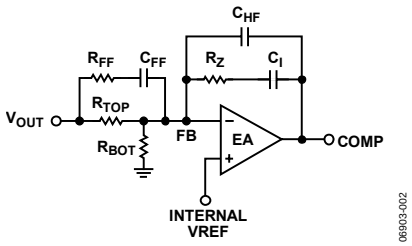

Figure 2. Type III Compensation

The compensation values for this evaluation board have been optimized as follows:

R_{FF} = 7.5 kΩ
C_{FF} = 680 pF
R_Z = 20 kΩ
C_I = 5.6 nF
C_{HF} = 33 pF
R_{TOP} = 20 kΩ
R_{BOT} = 10 kΩ

TEST RESULTS

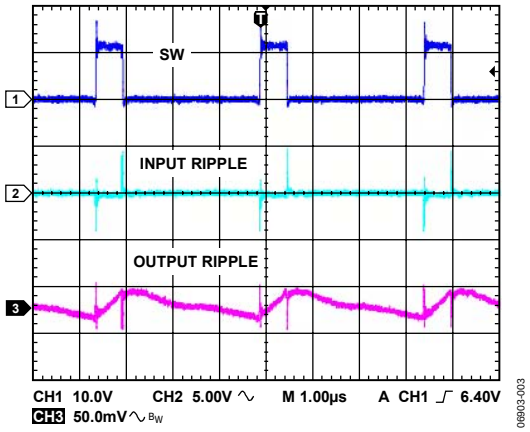

Figure 3. Output Ripple, V_{IN} = 12 V, Load = 22 A

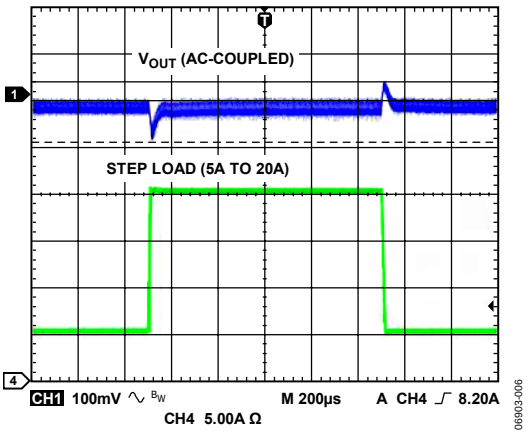

Figure 6. Load Transient, V_{IN} = 12 V, Load = 5 A to 20 A

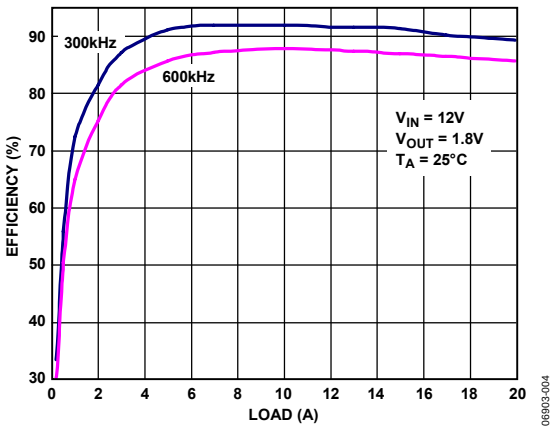

Figure 4. Efficiency vs. Load Current

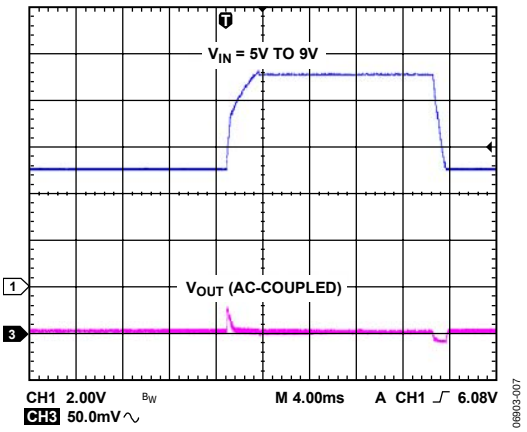

Figure 7. Line Transient, V_{IN} = 5 V to 9 V, No Load

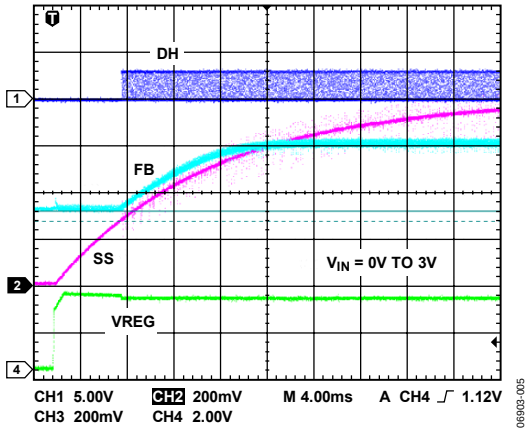

Figure 5. Soft Start into Precharged Load

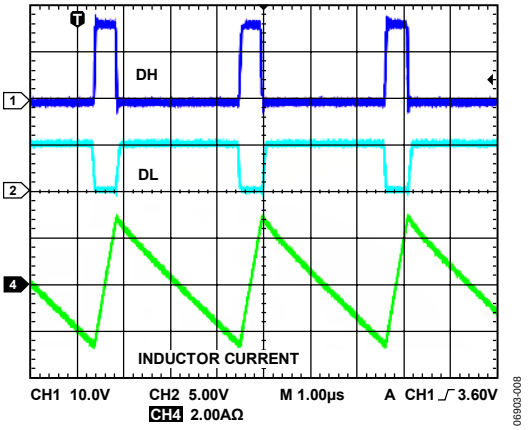

Figure 8. Inductor Current Waveform, V_{IN} = 12 V, No Load

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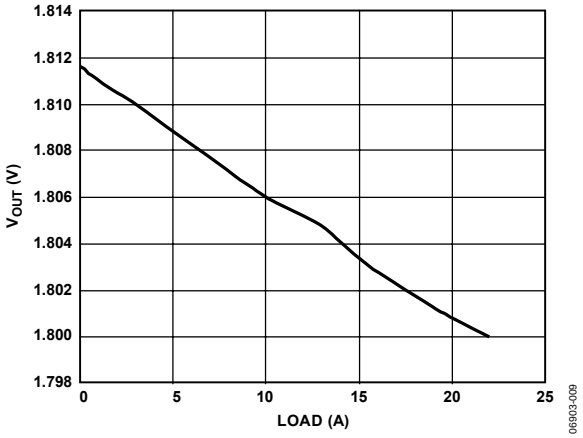

Figure 9. Load Regulation, V_{IN} = 12 V

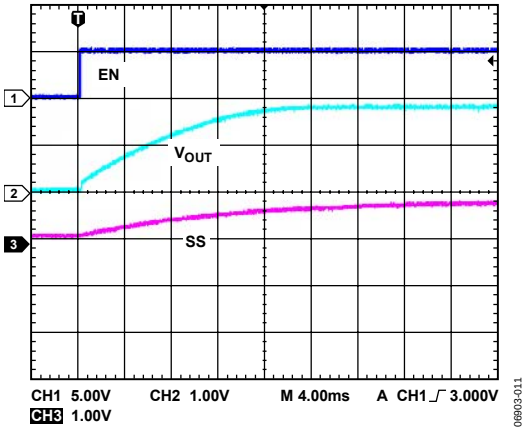

Figure 11. Soft Start, V_{IN} = 12 V

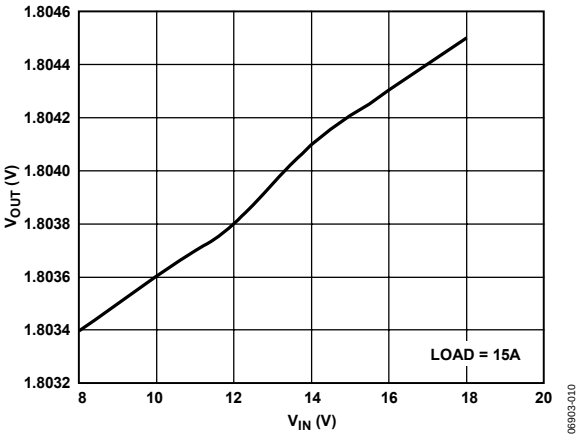

Figure 10. Line Regulation

EVALUATION BOARD OPERATING INSTRUCTIONS

1. Connect Jumper JP3 to the on position to enable the ADP1828.
2. Do not connect Jumper J7 (V_{IN} to VREG).
3. Connect Jumper JP2 (FREQ) to the 300 kHz position.
4. Connect Jumper J11 (SYNC) to GND (that is, if SYNC is not used). If SYNC is used, connect SYNC to an external clock or CLKOUT from another ADP1828.
5. Connect Jumper JP1 (CLKSET) to high, which sets CLKOUT to 2× the internal oscillator frequency and in phase with the oscillator, or to low, which sets CLKOUT to 1× the oscillator frequency and 180° out of phase.
6. Connect the positive terminal of the input power supply to the input terminal, J8.
7. Connect the load to the V_{OUT} terminal, J13.

Table 1. Jumper Descriptions

Jumper	Description	Function
JP1	CLKSET. Clock set input.	CLKSET = high sets CLKOUT to 2 × f_{OSC} CLKSET = low sets CLKOUT to 1 × f_{OSC}
JP2	Frequency selection. Connect to VREG for f_{SW} = 600 kHz.	VREG: f_{SW} = 600 kHz GND: f_{SW} = 300 kHz
JP3	EN. Connect to the on position to enable the ADP1828.	EN = on enables ADP1828 EN = off disables ADP1828
J7	VREG to V_{IN}. Do not connect this jumper when V_{IN} is more than 5.5 V.	Short VREG to V_{IN} when V_{IN} is less than 5.5 V
J11	SYNC. Connect SYNC to GND if the SYNC function is not used. If SYNC is used, connect SYNC to an external clock or to the CLKOUT from another ADP1828.	Synchronization
J9	12 V supply from the disk drive connector. Short this jumper if the 12 V input supply comes from the disk drive connector. Do not short J9 and J10 at the same time.	12 V supply from disk drive
J10	5 V supply from the disk drive connector. Short this jumper if the 5 V input supply comes from the disk drive connector. Do not short J9 and J10 at the same time.	5 V supply from disk drive

Table 2. Evaluation Board Operating Conditions

Parameter	Condition
V_{IN}	Input range 10 V to 18 V.
V_{OUT}	V_{OUT} = 1.8 V at 20 A.
f_{SW}	Switching frequency is set to 300 kHz.
Maximum Step Load	0 A to 20 A. This design can handle a 0 A to 20 A step load at the output.

Table 3. Temperature of the Power Components[1, 2]

ADP1828	Inductor (Würth Elektronik, 744355182)	High-Side MOSFET (Infineon Technologies, BSC080N03LS)	Low-Side MOSFETs (Infineon Technologies, 2 × BSC030N03LS)
61°C	65°C	87°C	76°C

[1] After the evaluation board ran for 30 minutes at a 20 A load, the surface temperatures of the power components were measured with an infrared thermometer.
[2] V_{IN} = 12 V, T_A = 25°C

Table 4. Miscellaneous Information

Parameter	Comment
Switching Frequency, f_{SW}	The switching frequency, f_{SW}, is set to 300 kHz (Jumper JP2) on the evaluation board. If a different f_{SW} is desired, the compensation and the power components need to be recalculated. If a f_{SW} other than 300 kHz or 600 kHz is desired, a resistor, R13, can be soldered onto the PCB to select any frequency between 300 kHz and 600 kHz.
Power MOSFETs: PG-TDSON-8 (Super-SO8) or PowerPAK SO-8	The footprint for the power MOSFETs is laid out to fit both the PowerPAK SO-8 and the standard SO-8 package. The board is laid out to fit two MOSFETs for the top side and two for the bottom side. Only one high-side MOSFET is fitted on the evaluation board.
Inductor	The footprint for the inductor is laid out to fit inductors smaller or larger than the on-board inductor.
VREG and V_{IN}	For input voltages less than 5.5 V, the user can connect Jumper J7 by shorting VREG to V_{IN}.
Snubber Circuit	A snubber RC circuit, R_{SNUB} and C_{SNUB}, is laid out on the evaluation board to help reduce switching noise and ringing at the SW node. The user can remove this RC snubber or try different RC values for a particular application. Note that the RC snubber dissipates power and slightly reduces the overall efficiency, generally in the range of 0.1% to 0.5%.
Gate Resistors	The dummy 0 Ω gate resistors, R2, R3, R14, and R15, are provided on the evaluation board for reducing overshoot voltage at the drains of the external MOSFETs. The user can change these 0 Ω resistors to different values (generally in the range of 1 Ω to 5 Ω) to achieve the desired reduction in overshoot voltage. Keep in mind that the gate resistor dissipates power and slightly reduces the overall efficiency.
Capacitor C22	A ceramic capacitor, C22, is placed very close to the drain of the high-side MOSFET. This capacitor, typically 0.1 µF to 1 µF, helps reduce input impedance during high frequency transients. C22 is not assembled on the evaluation board. The user can add this capacitor if needed for a particular application.
Voltage Divider	If a different output voltage other than 1.8 V is desired, the user needs to change the voltage feedback divider, R7 and R8, and rework the compensation component values as well as possibly the input and output capacitances.

Table 5. Suggestions of Power Components for Other Configurations

V_{IN} Range	V_{OUT} Range	Output Current	Inductor	High-Side MOSFETs[1]	Low-Side MOSFETs[1]	Input Capacitors[2]	Output Capacitors[3]
6 V to 18 V	1.2 V to 5 V	8 A to 13 A	1 µH[4] HC7-1R0-R	BSC080N03LS	BSC030N03LS	2 × 20SP180M	2R5TPD1000M5 + 22 µF/6.3 V/X5R
6 V to 18 V	1.2 V to 5 V	13 A to 22 A	0.82 µH[5] 744355182	BSC080N03LS	2 × BSC030N03LS	2 × 20SP180M	2 × 2R5TPD1000M5 + 47 µF/6.3 V/X5R
6 V to 18 V	1.2 V to 5 V	22 A to 27 A	0.47 µH[5] 744355147	2 × BSC080N03LS	2 × BSC030N03LS	3 × 20SP180M	3 × 2R5TPD1000M5 + 47 µF/6.3 V/X5R

[1] MOSFETS are from Infineon Technologies.
[2] Input capacitors are the OS-CON type from Sanyo.
[3] Output capacitors are the POSCAP type from Sanyo.
[4] From Coiltronics.
[5] From Würth Elektronik Group.

EVALUATION BOARD SCHEMATIC

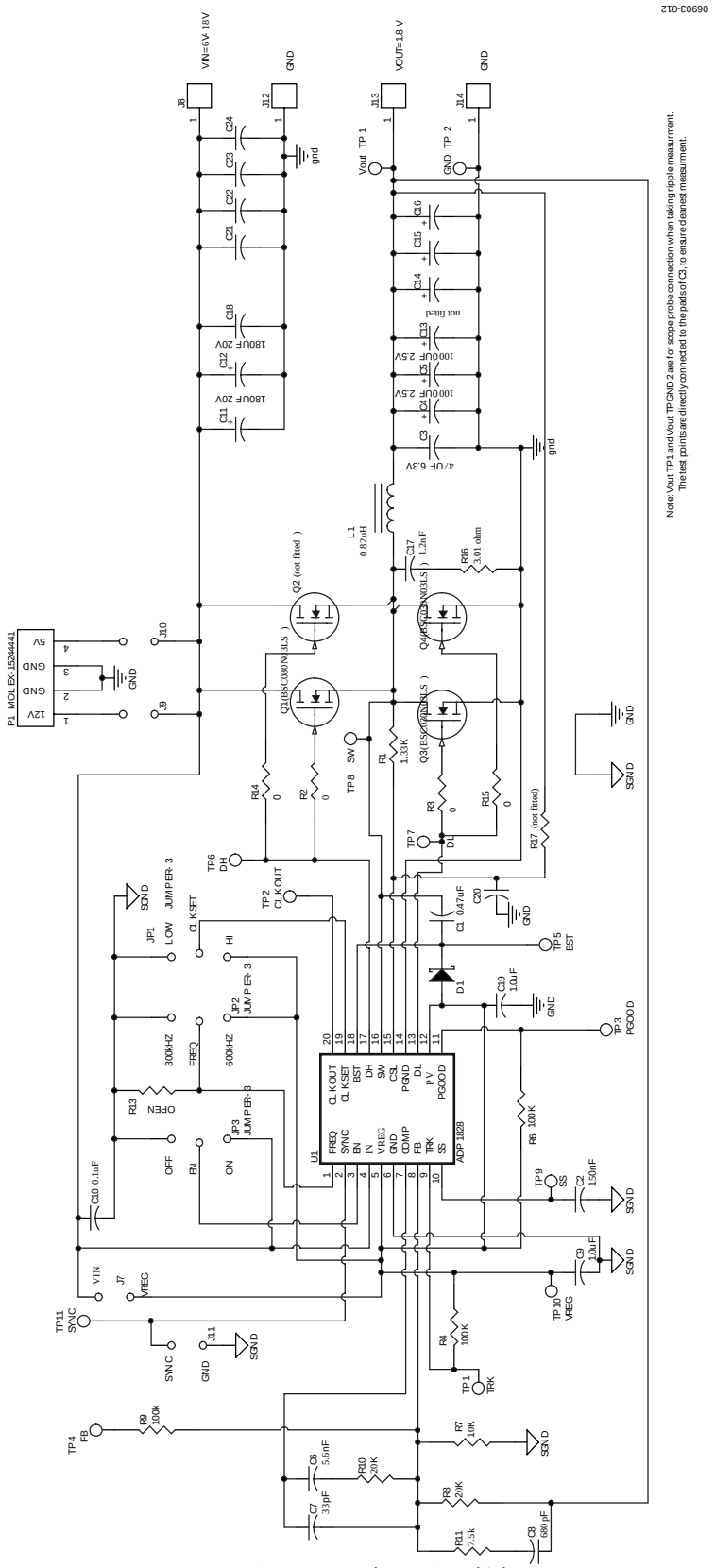

Figure 12. ADP1828 20 A Evaluation Board Schematic

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EVALUATION BOARD LAYOUT

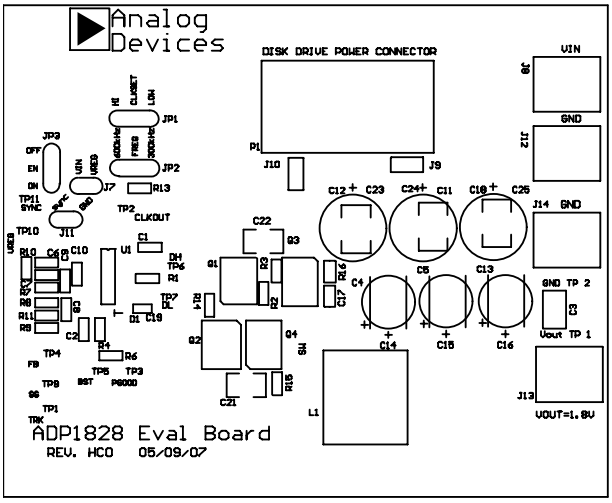

Figure 13. Silkscreen Layer

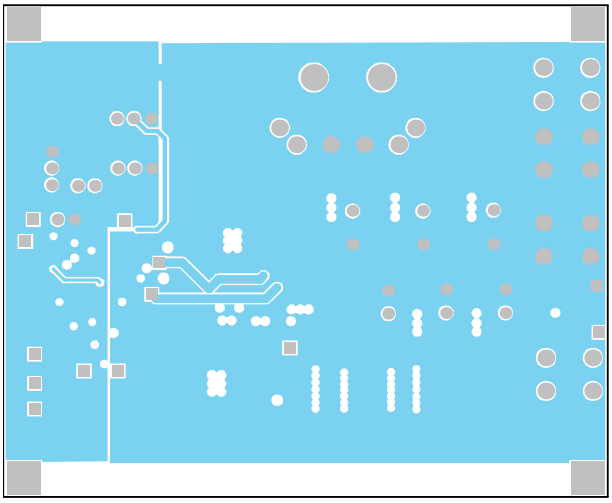

Figure 16. Third Layer (GND Layer)

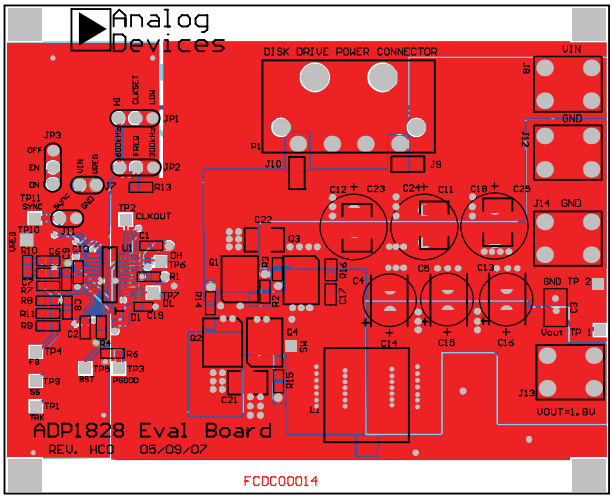

Figure 14. Top Layer

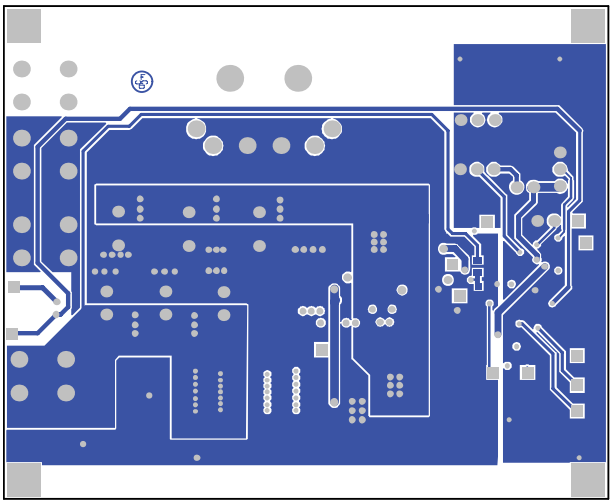

Figure 17. Bottom Layer

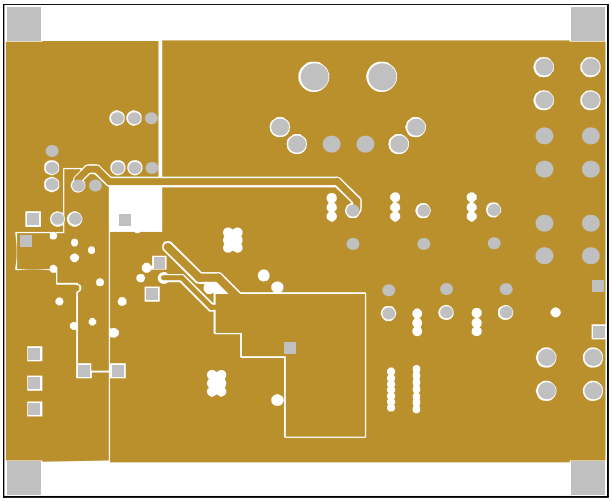

Figure 15. Second Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 6. Component Listing

Item	Qty	Designator	Description	Manufacturer	Part No.
1	2	C11, C12	Capacitor, OS-CON, 180 µF, 20 V, 4.28 A	Sanyo	20SP180M
2	2	C4, C5	Capacitor, POSCAP, 1000 µF, 2.5 V, 6 A, 5 mΩ	Sanyo	2R5TPD1000M5
3	1	C3	Capacitor, ceramic, 47 µF, 6.3 V, X5R, 1206	Murata	GRM31CR60J476ME19
4	1	C1	Capacitor, ceramic, 0.47 µF, 10 V, X5R, 0603	Taiyo Yuden Murata	LMK107BJ474MA-T GRM188R61A474KA61
5	1	C10	Capacitor, ceramic, 0.1 µF, 6.3 V, X5R, 0603	Vishay	VJ0603Y104MXQ
6	4	R2, R3, R14, R15	Resistor (dummy), 0 Ω, 1/10 W, 1%, 0603	Vishay	CRCW06030R00F
7	1	R8	Resistor, 20 kΩ, 1/10 W, 1%, 0603	Vishay	CRCW06032002F
8	1	R7	Resistor, 10 kΩ, 1/10 W, 1%, 0603	Vishay	CRCW06031002F
9	1	R11	Resistor, 7.5 kΩ, 1/10 W, 1%, 0603	Vishay	CRCW06037501F
10	1	R10	Resistor, 20 kΩ, 1/10 W, 1%, 0603	Vishay	CRCW06032002F
11	3	R4, R6, R9	Resistor, 100 kΩ, 1/10 W, 1%, 0603	Vishay	CRCW06031003F
13	1	R16	Resistor, 3.01 Ω, 0805 (snubber)	Vishay	CRCW08053R01F
14	1	R1	Resistor, 1.33 kΩ, 1/10 W, 1%, 0603 (current-limit resistor)	Vishay	CRCW06031331F
15	1	C2	Capacitor, ceramic, 150 nF, 16 V, X7R, 0603	Vishay	VJ0603Y154KXJA
16	1	C8	Capacitor, ceramic, 680 pF, 0603	Vishay	VJ0603Y681KXXA
17	1	C7	Capacitor, ceramic, 33 pF, 0603	Vishay	VJ0603A330KXXA
18	1	C6	Capacitor, ceramic, 5.6 nF, 0603	Vishay	VJ0603Y562KXXA
19	2	C9, C19	Capacitor, ceramic, 1.0 µF, 10 V, X5R, 0603	Taiyo Yuden Murata	LMK107BJ105MK-T GRM185R61A105KE36
21	1	C17	Capacitor, ceramic, 1.2 nF, 0805 (snubber)	Vishay	VJ0805Y122KXXA
22	1	L1	Inductor 0.82 µH, 27 A, 0.9 mΩ, HCA series	Würth Elektronik Group	744355182
23	1	D1	Schottky diode, 30 V, V_F = 0.5 V @ 30 mA, SOD323	Vishay	BAT54WS
24	1	Q1	Transistor, N-MOSFET, 30 V, Super-SO8, 12 mΩ @ 4.5 V, 30 A	Infineon Technologies	BSC080N03LS
25	2	Q3, Q4	Transistor, N-MOSFET, 30 V, Super-SO8, 4.7 mΩ @ 4.5 V, 30 A	Infineon Technologies	BSC030N03LS
26	1	P1	Disk drive power connector	Molex Inc.	15244441
27	3	JP1, JP2, JP3	3-terminal jumpers, 0.1" spacing	Any	
28	1	J11	2-terminal jumper, 0.1" spacing	Any	
29	13	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, VOUT TP 1, GND TP 2	Test points for VREG, SW, DH, DL, TRK, SS, PGOOD, BST, FB, SYNC, CLKOUT, GND, VOUT	Any	40 mil (1 mm) through hole
30	1	U1	DUT, 20-lead QSOP	Analog Devices	ADP1828

ORDERING GUIDE

Model	Description
ADP1828HC-EVALZ[1]	Evaluation Board

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.