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DS26303DK

3.3V, E1/T1/J1, Short-Haul, Octal LIU Design Kit

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GENERAL DESCRIPTION

The DS26303DK is a fully integrated design kit for the DS26303 3.3V, 8-port, E1/T1/J1 line interface unit (LIU). This design kit contains all the necessary circuitry to evaluate the DS26303 in all modes of operation. The design kit also includes an on-board microprocessor to run real-time code for further part evaluation.

DESIGN KIT CONTENTS

DS26303DK Board
 5V AC/DC Adapter
 3ft USB Cable

Download:

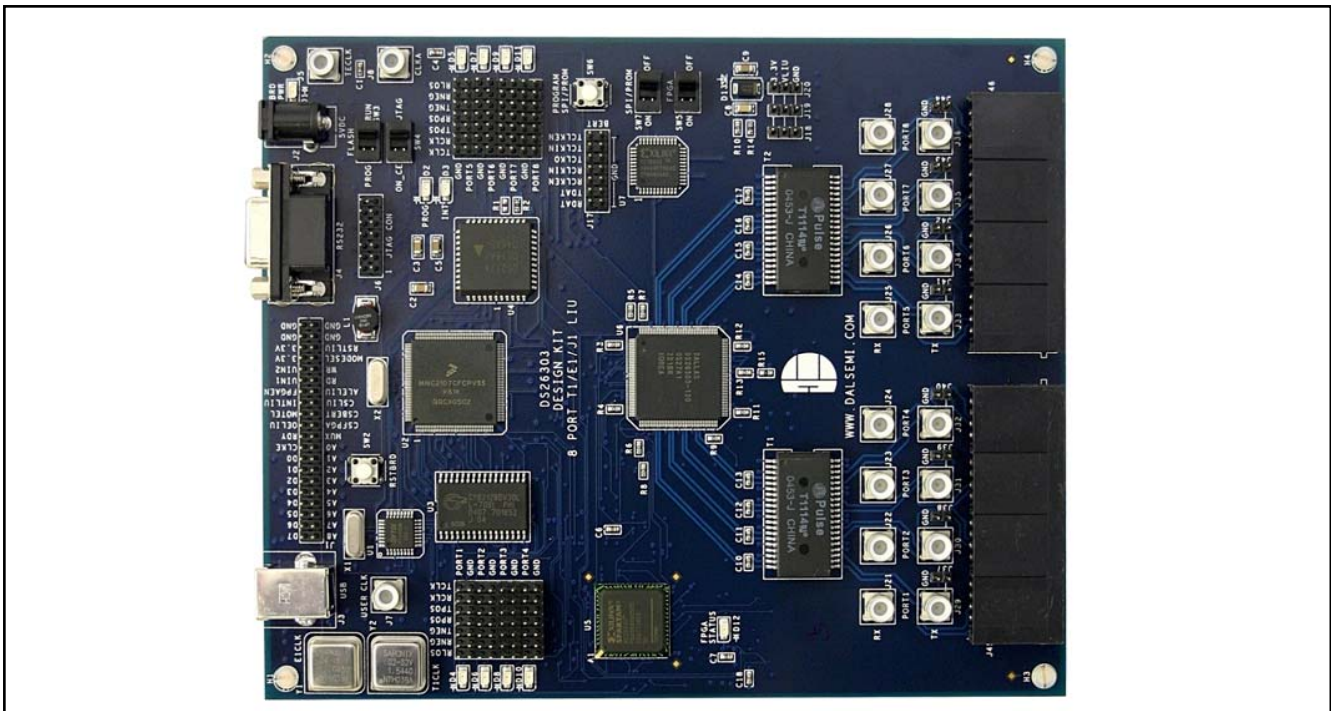
ChipView Software
 DS26303DK.def Definition Files
 DS26303DK Data Sheet

ORDERING INFORMATION

PART	DESCRIPTION
DS26303DK	DS26303 Design Kit Board

FEATURES

- Expedites New Designs by Eliminating First-Pass Prototyping
- Demonstrates Key Functions of the DS26303
- Includes DS26303 x 8-Port LIU, Transformers, 75Ω BNC Connectors, RJ-48 Connectors, and Termination Passives
- Communicates Directly with any PC with a USB or RS-232 Serial Interface
- High-Level Windows®-Based Software Provides Visual Access to All Registers
- Software-Controlled (Register) Mapped Configuration Switches Facilitate Real-Time Clock and Signal Routing
- Precision Test Points for All Clocks and Signals
- On-Board T1 and E1 Crystal Oscillators for Stable Clock Generation
- On-Board BERT for Testing and Pattern Generation



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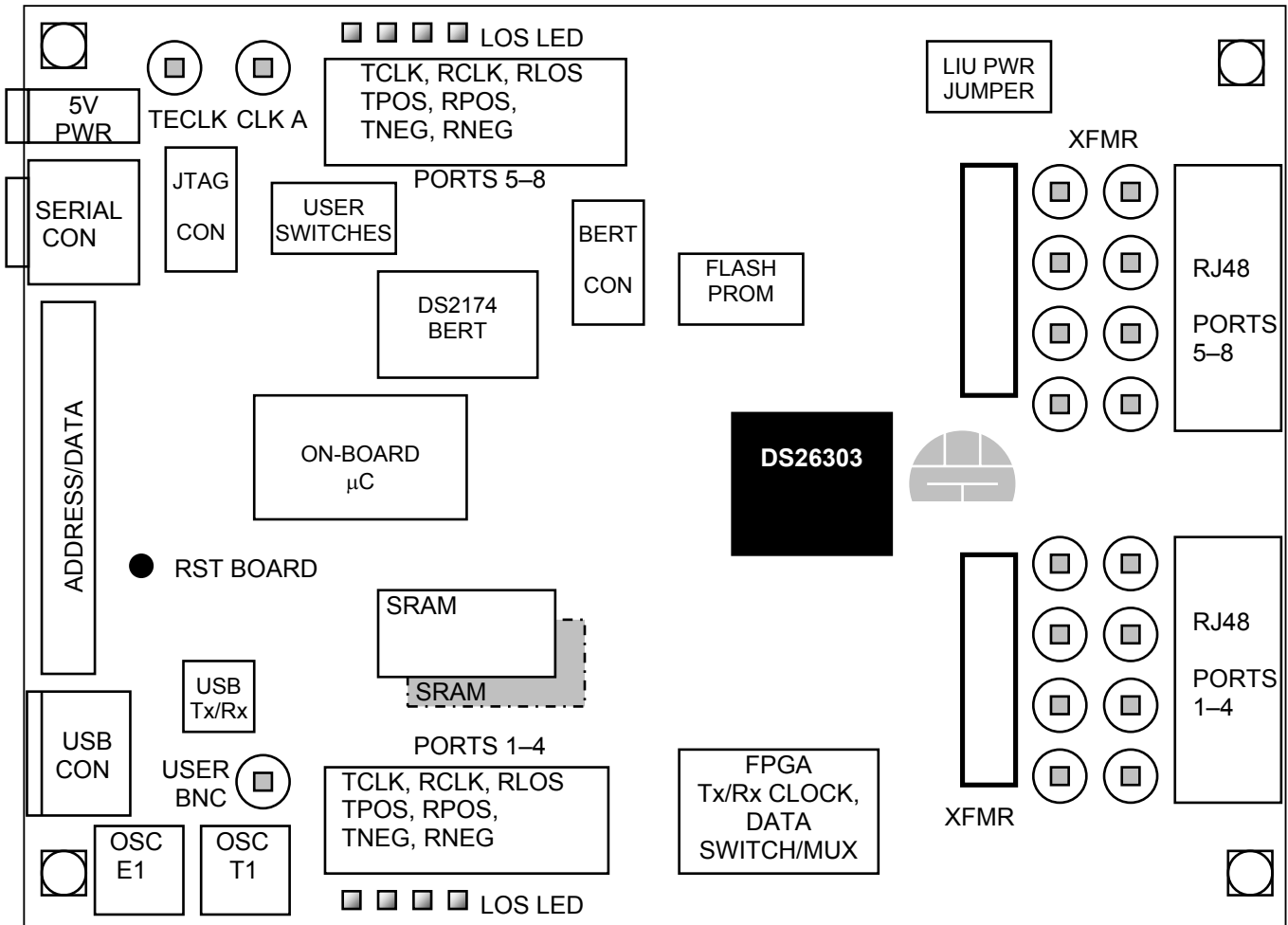
COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/ PART NUMBER
C1, C4, C6, C7, C18, C24, C26, C34, C36, C37, C38, C41, C43–C47, C49, C50, C51, C53–C59, C61–C83, C85, C86, C90	53	0.1 μ F \pm 20%, 16V X7R ceramic capacitors (0603)	AVX 0603YC104MAT
C2, C3, C22, C30, C35, C40, C42, C48, C52, C60, C84, C88, C89	13	1 μ F \pm 10%, 16V ceramic capacitors (1206)	Panasonic ECJ-3YB1C105K
C5, C9, C19, C21, C27, C28, C87	7	10 μ F \pm 20%, 10V ceramic capacitors (1206)	Panasonic ECJ-3YB1A106M
C8	1	6.8 μ F \pm 10%, 6.3V X5R ceramic capacitor (1206)	Panasonic ECJ-3YB0J685K
C10–C17	8	470pF \pm 10%, 100V ceramic capacitors (0603)	Panasonic ECJ-1VB2A471K
C20, C23, C25, C91, C92	5	68 μ F \pm 20%, 16V tantalum capacitors (D case)	Panasonic ECS-T1CD686R
C29, C31, C39	3	22pF \pm 5%, 25V ceramic capacitors (0603)	AVX 06033A220JAT
C32, C33	2	10pF \pm 5%, 50V ceramic capacitors (1206) (tall case)	Phycomp 1206CG100J9B200
D1, D12	2	Green LEDs (SMD)	Panasonic LN1351C
D2–D11	10	Red LEDs (SMD)	Panasonic LN1251C
D13, D14, D15	3	1A, 40V Schottky diodes	International Rectifier 10BQ040
H1–H4	4	KIT, 4-40 hardware 0.75 nylon standoff and 0.25 nylon screw	Not applicable 4-40KIT2
J1	1	40-pin terminal strip (dual row, vertical)	Samtec TSW-120-07-T-D
J2	1	2.1mm/5.5mm connector Power jack, right-angle PC board mount; closed frame, high current, 24V DC at 5A	CUI, Inc. PJ-002AH
J3	1	Black, single right angle (Type B)	Molex Not applicable
J4	1	DB9 right-angle connector (short case)	AMP 788750-2
J5, J7, J8, J21–J36	19	5-pin SMB connectors 50 Ω , vertical, gold	AMP 413990-1
J6, J9–J17	10	14-pin headers (dual row, vertical)	Samtec TSW-107-14-T-D
J18, J19, J20	3	100-mil 3-position jumpers	Samtec Not applicable
J37–J44	8	2-pin headers, 0.100in centers (vertical)	Samtec TSW-102-07-T-S
J45, J46	2	8-pin 4-port RJ45 jacks (right angle)	Molex 43223-8140
L1	1	1.0 μ H \pm 20%, 2-pin SMT inductor	Coiltronics UP1B-1R0

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/ PART NUMBER
R1, R58, R87	3	Resistors (0603) DO NOT POPULATE	—
R2, R14–R26, R28, R32–R43, R46– R50, R52, R54– R57, R63–R66, R68, R69, R71, R72, R73, R76, R77, R82, R85, R86, R88, R91, R93, R96, R97, R130	57	10k Ω \pm 5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ103V
R3–R9, R11, R12, R13, R29, R31, R44, R45, R60, R61, R62, R78, R79, R94, R95, R98–R102, R104, R117, R120, R121, R124–R129	36	33 Ω \pm 5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ330V
R10	1	22k Ω \pm 5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ223V
R27, R67, R70, R74, R75, R80, R81, R83, R84, R89, R90, R123	12	330 Ω \pm 5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ331V
R30, R59	2	15k Ω \pm 5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ153V
R51	1	Resistor (1206) DO NOT POPULATE	—
R53	1	470 Ω \pm 5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ471V
R92	1	51 Ω \pm 5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ510V
R103, R105–R116, R118, R119, R122	16	60.4 Ω \pm 1%, 1/16W resistors (0603)	Panasonic ERJ-3EKF60R4V
SW2, SW6	2	4-pin single-pole switch	Panasonic EVQPAE04M
SW3, SW4, SW5, SW7	4	6-pin slide switches (DPDT, through hole)	Tyco Electronics SSA22
T1, T2	2	Transformers (1:2 count transmitter/1:1 count receiver) (40-pin wide SO, -40°C to +85°C)	Pulse Engineering T1114
U1	1	8-bit FIFO USB UART (32-pin LQFP)	FTDI FT245BM
U2	1	MCORE Microcontroller (144-pin LQFP)	Motorola MMC2107PV
U3, U11	2	128k x 8 SRAM (32-pin SO)	Cypress CY62128VL-70SC
U4	1	DS2174 EBERT (44-pin PLCC, 0°C to +70°C)	Dallas Semiconductor DS2174Q
U5	1	Spartan-II 2.5V FPGA, 200k gate (256-pin BGA)	Xilinx XC2S200-5FG256C
U6	1	3.3V, E1/T1/J1 long-haul octal LIU (144-pin eLQFP, 0°C to +70°C)	Dallas Semiconductor DS26303L

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/ PART NUMBER
U7	1	PROM for FPGA (44-pin TQFP)	Xilinx XC18V02VQ44C
U8	1	Dual RS-232 transmitter/receiver (150-mil, 16-pin SO)	Dallas Semiconductor DS232AR
U9, U12	2	High-speed buffers	Fairchild Semiconductor NC7SZ86
U10, U18	2	1.5W, 3.3V or adj, 1A linear regulators (16-pin TSSOP-EP)	Maxim MAX1793EUE-33
U13, U15	2	Hex inverters (14-pin SO)	Toshiba TC74HC04AFN
U14	1	Quad 2-input NAND gate (14-pin SO)	Toshiba TC74HC00AFN
U16	1	Switch debouncer (4-pin SOT143)	Maxim MAX6816EUS-T
U17	1	2.5V or adj linear regulator (8-pin μ MAX/SO)	Maxim MAX1792EUA25
U19	1	Platform flash in-system programmable configuration PROM (2Mb, 20-pin TSSOP)	Xilinx XCF02SVO20C
X1	1	6.00MHz low-profile crystal	Pletronics LP49-26-6.00M
X2	1	8.000MHz low-profile crystal	Ecliptek Corp. EC1-8.000M
Y1	1	Oscillator, crystal clock 5V, 2.048MHz	SaRonix NTH039A-2.0480
Y2	1	Oscillator, crystal clock 5V, 1.544MHz	SaRonix NTH039A-1.5440

BOARD FLOORPLAN



BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/DS26303DK.

The support files are used with an evaluation program called ChipView, which is available for download at www.maxim-ic.com/telecom.

HARDWARE CONFIGURATION

Quick Start (Hardware Settings—Single Power Supply)

- For single power-supply operation, short jumpers J18, J19, and J20 between the 3.3V pin and the VLIU pin. This connects VDD of the DS26303 to the 3.3V supply on the design kit.
- Ensure that the FLASH switch (SW3) is in the *RUN* position.
- Ensure that the FPGA switch (SW5) is in the *ON* position.
- Ensure that the SPI/PROM switch (SW7) is in the *OFF* position.
- If using the serial port, connect a RS-232 serial cable from DS26303DK (J4) to the PC.
- If using the USB port, connect a USB cable from DS26303DK (J3) to the PC.
- Connect AC/DC adapter with an AC power source and the DS26303DK (J2). PWR LED should be on.

JTAG Configuration

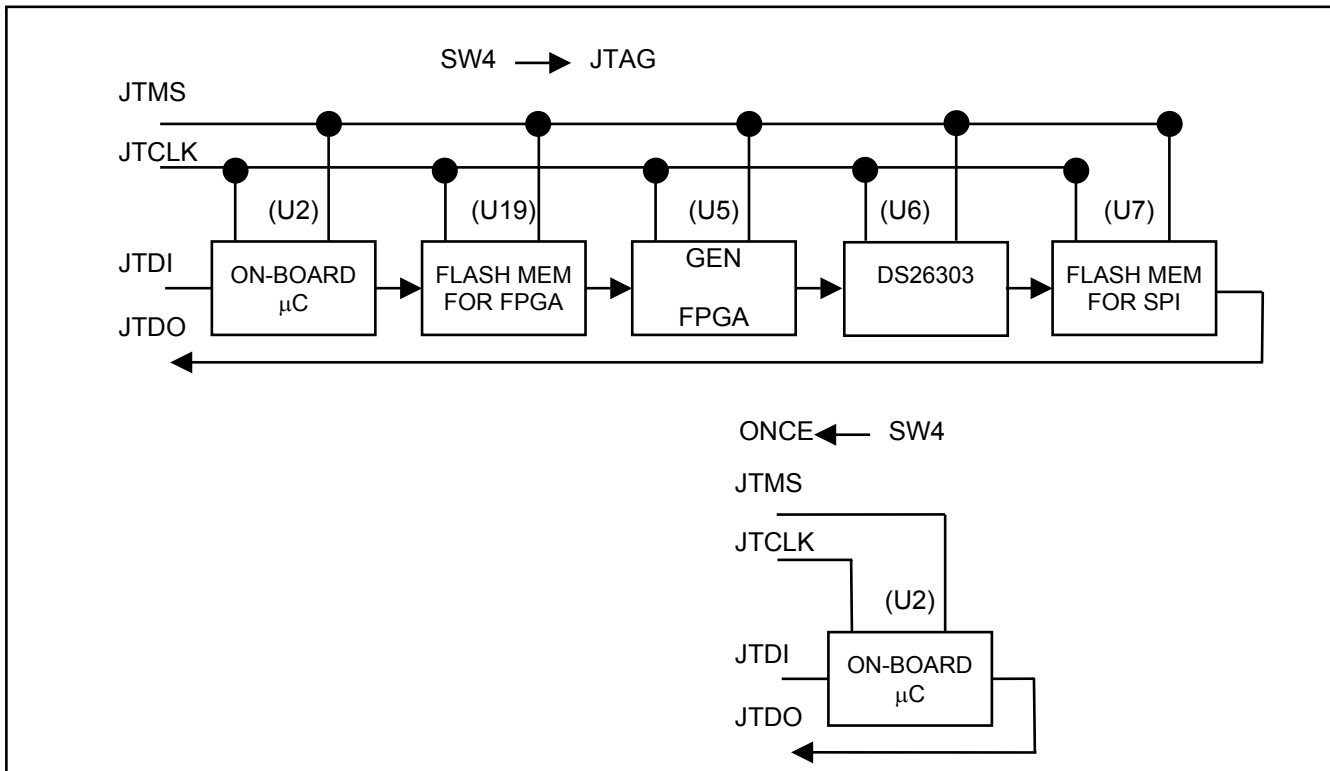
The JTAG chain is controlled by the connector JTAG CON (J6) and two on-board switches: FLASH (SW3) and ONCE/JTAG (SW4). Depending on the function, such as programming the internal microcontroller flash or performing boundary scan operations, the JTAG CON connector can be used and the switches can be configured to accomplish the desired task. For information on programming the internal flash of the on-board microcontroller, refer to the MMC2107 microcontroller user manual and board schematic.

For most purposes, having the complete JTAG chain is sufficient. [Figure 1](#) shows the complete chain as well as what order the devices appear during boundary scan. [Table 1](#) shows the pinout of the JTAG connector. Connect any JTAG cable to the connector to perform all operations. Note the JTAG chain changes depending on the switch SW4. The ONCE location of SW4 is used for programming the on-board microcontroller only.

Table 1. JTAG Connector (J6) Pinout

PIN	NAME
1	JTDI
2, 4, 6, 7	GND
3	JTDO
5	JTCLK
8	ALIGN KEY
9	BRD RST
10	JTMS
11	BRD V3.3
12	JDE
13	N.C.
14	JTRST

Figure 1. DS26303DK JTAG Chain



Address/Data Bus Connector

The DS26303DK has a connector (J1) to monitor all local bus activity for the design kit. All the signals can be captured with a high-impedance probe and displayed on an oscilloscope or logic analyzer. **Note:** If the FPGA switch (SW5) is in the “OFF” position, the on-board microcontroller will no longer drive any data onto the local bus. Therefore, the user can now connect the local bus of the DS26303 into another system without making any modifications to the hardware. See [Table 2](#) for specific pin information for connector J1.

Table 2. Address/Data Connector Pinout

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	A8	Local Address Bit 8	2	D0	Local Data Bit 0
3	A7	Local Address Bit 7	4	D1	Local Data Bit 1
5	A6	Local Address Bit 6	6	D2	Local Data Bit 2
7	A5	Local Address Bit 5	8	D3	Local Data Bit 3
9	A4	Local Address Bit 4	10	D4	Local Data Bit 4
11	A3	Local Address Bit 3	12	D5	Local Data Bit 5
13	A2	Local Address Bit 2	14	D6	Local Data Bit 6
15	A1	Local Address Bit 1	16	D7	Local Data Bit 7
17	A0	Local Address Bit 0	18	CLKE	SPI Clock Edge Select
19	MUX	Mux	20	RDY	Ready Handshake from LIU
21	CSFPGA	Chip Select FPGA	22	OE	Output Enable LIU
23	CSBERT	Chip Select DS2174	24	MOTEL	Motorola/Intel Select
25	CSLIU	Chip Select DS26303	26	INT	Interrupt for DS26303
27	ALELIU	Address Latch Enable	28	FPGAEN	FPGA Enable Pin
29	RD	Read Signal	30	UIN1	User Input 1
31	WR	Write Signal	32	UIN2	User Input 2
33	MODESEL	Mode Select	34, 36	3.3V	Board 3.3V
35	—	Not Used	37–40	GND	Ground

Telecom Clock and Data Test Points

The DS26303DK has high-impedance test points for all the telecom signals that are related to the LIU. These signals are split up by port number and marked with easy to read silkscreen labels. [Table 3](#) shows the telecom connector for port 1. The pinout for this connector is repeated for all 8 ports.

Table 3. Telecom Connector Pinout

PIN	NAME	FUNCTION
1	TCLK	Transmit Clock Input
2, 4, 6, 8, 10, 12, 14	GND	Ground
3	RCLK	Receive Clock Output
5	TPOS	Transmit Positive Data Input
7	RPOS	Receive Positive Data Output
9	TNEG	Transmit Negative Data Input
11	RNEG	Receive Positive Data Output
13	RLOS	Receive Loss-of-Signal Output

Note that the input signals in the telecom connector go from the connector to the on-board FPGA, then to the DS26303. The FPGA was designed to perform specific signal routing functions such as looping back RPOS to TPOS on a particular port or transferring data from the on-board BERT. If you are using user-defined data and drive the signal on the connector, be sure to tri-state the input signal in the FPGA. **FAILURE TO DO SO COULD CAUSE DAMAGE TO THE FPGA!**

On-Board Bit Error-Rate Tester (BERT)

The DS26303DK has an on-board bit error-rate tester (BERT) to generate and detect errors in either pseudorandom or user-defined patterns. The BERT on the DS26303DK is the DS2174. A header for the relevant signals related to the BERT is located on the board (J17). See [Table 4](#) for the pinout of the BERT connector. The BERT signals are routed into the FPGA and can be muxed into any of the 8 DS26303 LIU ports under software control. For all questions concerning the operation of the on-board BERT, refer to the device data sheet available online at www.maxim-ic.com/telecom. If you are using user-defined data and driver the signal on the connector, be sure to tri-state the input signal in the FPGA. **FAILURE TO DO SO COULD CAUSE DAMAGE TO THE FPGA!**

Table 4. BERT Connector Pinout

PIN	NAME	FUNCTION
1	TCLK_EN	BERT TCLK Enable
2, 4, 6, 8, 10, 12, 14	GND	Ground
3	TCLKIN	BERT TCLK Input
5	TCLKO	BERT TCLK Output
7	RCLKIN	BERT RCLK Input
9	RCLKEN	BERT RCLK Enable
11	TDAT	BERT TDAT Output
13	RDAT	BERT RDAT Input

PROM SPI Configuration

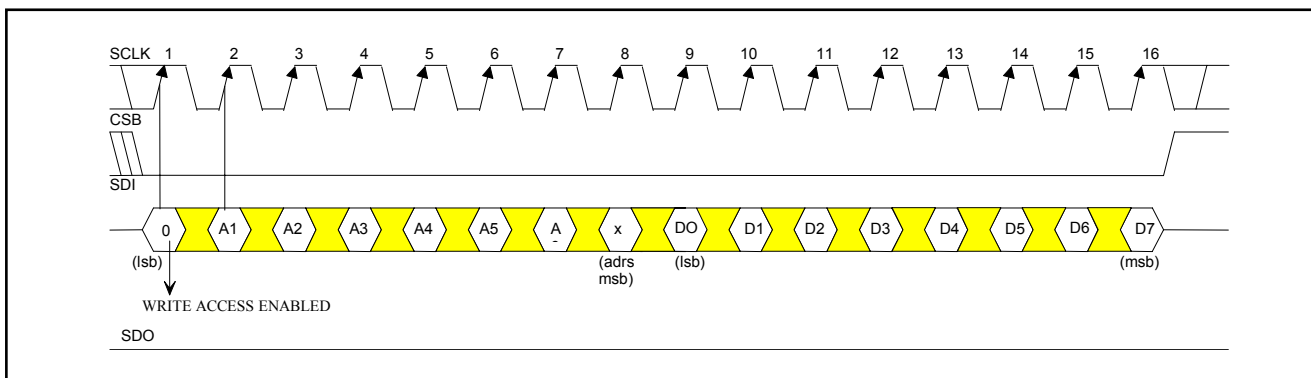
In software mode, it is possible to configure the DS26303 using a parallel interface or a serial peripheral interface (SPI). Most advanced microcontrollers have both a parallel interface and SPI interface such as the microcontroller on the DS26303DK. The command you send to the microcontroller through either the USB or serial port determines if that data is placed on the parallel or SPI bus. Refer to the data sheet for [Chipview](#) on the particular commands required to switch data ports.

A unique feature with the SPI port is that a PROM can be used to provide the LIU with the specific data needed for configuration. If the data in the PROM is formatted a certain way, it can seem as the PROM is acting like a controller with a SPI interface in master mode.

The most common PROMs to use for this type of application are those with an internal address accumulator. This feature for the PROM is important because the device must automatically jump to the next available address in the configuration memory. The Xilinx XC18V00 device family is a byte-wide nonvolatile memory with an autoincrement address function. The family of devices is available in 1Mb, 2Mb, and 4Mb densities. The PROM is also useful because the device can perform in-circuit programming with the JTAG port. Refer the data sheet for the XC18V00 for the JTAG codes for programming the configuration memory.

[Figure 2](#) shows a general relationship of the timing for a SPI bus. For this case, all data is clocked into the slave device on the rising edge of SCLK. This feature can be configurable on the DS26303.

Figure 2. SPI Timing Diagram



[Figure 3](#) shows a simplified diagram of the XC18V00 device and the DS26303 in SPI (serial) mode. Notice a few key points about this diagram. First, the CLK for the XC18V00 is the MCLK for the LIU, but this is not the SCLK for the SPI interface. The SCLK can be programmed as needed. See [Table 5](#) for an example of the memory map. Second, the programming for this device begins when OE on the XC18V00 goes high. Therefore, consideration must be taken if some delay is necessary. Generally, it is sufficient for the OE pin to be connected to some power-up delay device. The OE delay is not necessary on this DK.

Figure 3. SPI Configuration with PROM

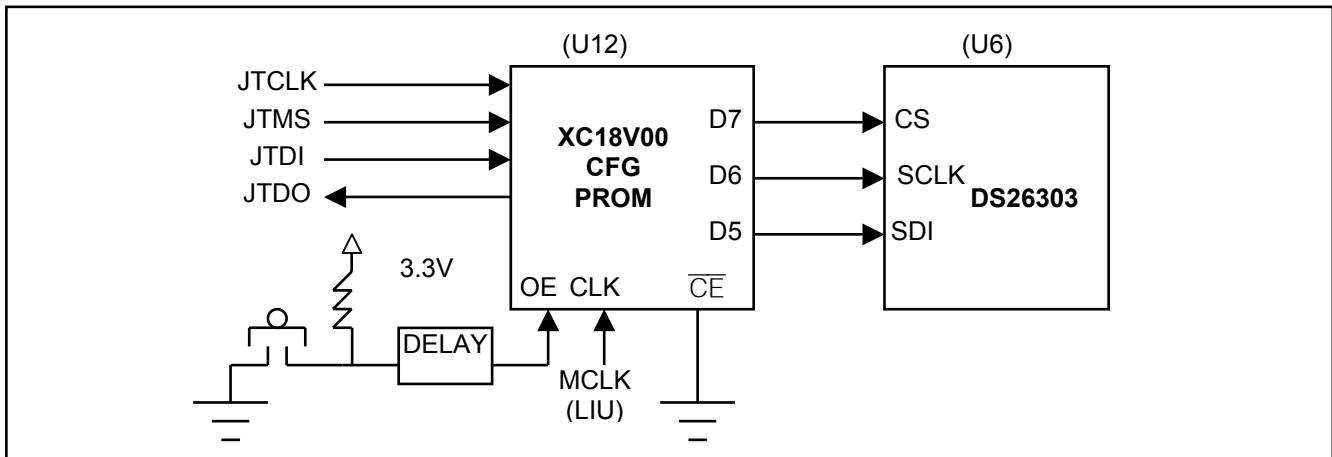


Table 5. Configuration Memory

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
	CSB	SCLK	SDI	X	X	X	X	X
0x00	1	0	0	Start of Write Cycle				
0x01	0	0	0	Bit A0				
0x02	0	1	0	(Always a "0" for a write)				
0x03	0	0	1	Bit A1				
0x04	0	1	1	Bit A2				
0x05	0	0	0	Bit A3				
0x06	0	1	0	Bit A4				
0x07	0	0	0	Bit A5				
0x08	0	1	0	Bit A6				
0x09	0	0	0	Bit A7				
0x0A	0	1	0	Bit D0 (LSB)				
0x0B	0	0	0	Bit D1				
0x0C	0	1	0	Bit D2				
0x0D	0	0	0	Bit D3				
0x0E	0	1	0	Bit D4				
0x0F	0	0	0	Bit D5				
0x10	0	1	0	Bit D6				
0x11	0	0	0	Bit D7				
0x12	0	1	0	End of Write Cycle				
0x13	0	0	1					
0x14	0	1	1					
0x15	0	0	1					
0x16	0	1	1					
0x17	0	0	0					
0x18	0	1	0					
0x19	0	0	0					
0x1A	0	1	0					
0x1B	0	0	1					
0x1C	0	1	1					
0x1D	0	0	1					
0x1E	0	1	1					
0x1F	0	0	0					
0x20	0	1	0					
0x21	1	0	X					
0x22	1	X	X					

SOFTWARE CONFIGURATION

Quick Start (Software—ChipView)

- Perform steps in the Quick Start (Hardware Configuration).
- Load ChipView software.
- Select COM port.
- Select Register View.
- From the Programs menu, launch the host application named ChipView.exe. If the default installation options were used, click the Start button on the Windows toolbar and select Programs -> ChipView -> ChipView.
- Load the DS26303DK.def file.
- Make sure that all the register settings are correct for the proper function desired for the DS26303DK.
- Refer to the DS26303 data sheet for all questions pertaining to device functionality.

MEMORY MAP

The on-board microcontroller is configured to start the user address space at 0x81000000. All offsets given below are relative to the beginning of the user address space.

Table 6. DS26303DK Relative Address Map

REF DES	DEVICE	OFFSET
U5	General-Purpose FPGA Tx/Rx Clock, Data Switch/Mux	0x0000
U4	DS2174 BERT	0x1000
U6	DS26303 8-Port T1/E1/J1 LIU	0x2000

All device registers can be easily modified using the ChipView.exe host-based user-interface software.

Table 7. General-Purpose FPGA Memory Map

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0x00	BRDID	Read-Only	Board ID
0x02	DSIDH	Read-Only	Dallas Extended ID Upper Nibble
0x03	DSIDM	Read-Only	Dallas Extended ID Middle Nibble
0x04	DSIDL	Read-Only	Dallas Extended ID Lower Nibble
0x05	BRDREV	Read-Only	Board Rev
0x06	ASMREV	Read-Only	Assembly Rev
0x07	FPGAREV	Read-Only	FPGA Firmware Rev
0x08	CTRL1	Control	Control Register 1
0x0A	ABSP	Control	Address Bank Select Pointer
0x0B	BTCLK	Control	BERT TCLK Input
0x0C	BRCLK	Control	BERT RCLK Input
0x0D	BRDAT	Control	BERT RDAT Input
0x10	TCLK	Control	Indirect Register for TCLK Source Control
0x11	TPOS	Control	Indirect Register for TPOS Source Control
0x12	TNEG	Control	Indirect Register for TPOS Source Control

ID REGISTERS

BID: BOARD ID (Offset = 0X0000)

BID is read-only with a value of 0xD.

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0X0002)

XBIDH is read-only with a value of 0x0.

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0X0003)

XBIDM is read-only with a value of 0x1.

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0X0004)

XBIDL is read-only with a value of 0x6.

BREV: BOARD FAB REVISION (Offset = 0X0005)

BREV is read-only and displays the current fab revision.

AREV: BOARD ASSEMBLY REVISION (Offset = 0X0006)

AREV is read-only and displays the current assembly revision.

PREV: FPGA REVISION (Offset = 0X0007)

PREV is read-only and displays the current PLD firmware revision.

CONTROL REGISTERS

Register Name: CTRL_1

Register Description: DS26303DK FPGA CONTROL REGISTER 1

Register Offset: 0x08

Bit #	7	6	5	4	3	2	1	0
Name	INT303	ENRLOS1	CLKE	SPI_SWAP	SPI	OE	MCLK1	MCLK0

Bit 7: INT303. This bit indicates the status of the INT303 line.

If INT303 = LOW, there is no hardware interrupt on the DS26303.

If INT303 = HIGH, there is a hardware interrupt on the DS26303.

Bit 6: ENRLOS1. This bit enables the RLOS1 LED. This should not be enabled when driving TECLK from the DS26303.

If ENRLOS1 = LOW, the RLOS1 LED is not enabled.

If ENRLOS1 = HIGH, the RLOS1 LED is enabled and lights when RLOS1 is high.

Bit 5: CLKE. This bit sets the CLKE pin on the DS26303. This is only active when SPI (Bit 0) is HIGH. If SPI (Bit 0) is low, CLKE is always low.

If CLKE = LOW, SDO is clocked out on the rising edge of SCLK.

If CLKE = HIGH, SDO is clocked out on the falling edge of SCLK.

Bit 4: SPI_SWAP. This bit sets the BSWP/A5 pin on the DS26303. This is only active when SPI (Bit 0) is HIGH.

If SPI_SWAP = LOW, the SPI bus is LSB first.

If SPI_SWAP = HIGH, the SPI bus is MSB first.

Bit 3: SPI. This bit sets up the FPGA to use serial mode. This bit also changes the mode pin on the DS26303.

If SPI = LOW, the parallel bus is used for all read/write access. This also sets the MODE pin on the DS26303 to logic 1.

If SPI = HIGH, the SPI bus is used for all read/write access. This also sets the MODE pin on the DS26303 to logic 0.

Bit 2: OE. This bit controls the OE pin to the DS26303.

Bits 1 and 0: MCLK1 and MCLK0. These bits control the MCLK pin to the DS26303.

MCLK1	MCLK0	DESCRIPTION OF MCLK
0	0	MCLK = high-impedance mode
0	1	MCLK = on-board T1 oscillator
1	0	MCLK = on-board E1 oscillator
1	1	MCLK = user clock input

Register Name: **ABSP**

Register Description: **ADDRESS BANK SWAP POINTER**

Register Offset: **0x0A**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the address bank for address 0x10 (TCLK N), 0x11 (TPOS), and 0x12 (TNEG).

ABSP	DESCRIPTION
0x00	Bank Address Value for Port 1
0x01	Bank Address Value for Port 2
0x02	Bank Address Value for Port 3
0x03	Bank Address Value for Port 4
0x04	Bank Address Value for Port 5
0x05	Bank Address Value for Port 6
0x06	Bank Address Value for Port 7
0x07	Bank Address Value for Port 8

Register Name: **BTCLK**

Register Description: **BERT TCLK SOURCE**

Register Offset: **0x0B**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the source of the TCLK for the BERT.

BTCLK	DESCRIPTION
0x00	RCLK Port 1
0x01	RCLK Port 2
0x02	RCLK Port 3
0x03	RCLK Port 4
0x04	RCLK Port 5
0x05	RCLK Port 6
0x06	RCLK Port 7
0x07	RCLK Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	TCLKBERT OUT
0x16–0xFF	HI-Z

Register Name: **BRCLK**

Register Description: **BERT RCLK SOURCE**

Register Offset: **0x0C**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the source of the RCLK for the BERT.

BTCLK	DESCRIPTION
0x00	RCLK Port 1
0x01	RCLK Port 2
0x02	RCLK Port 3
0x03	RCLK Port 4
0x04	RCLK Port 5
0x05	RCLK Port 6
0x06	RCLK Port 7
0x07	RCLK Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	TCLKBERT OUT
0x16–0xFF	HI-Z

Register Name: **BRDAT**

Register Description: **BERT RDAT SOURCE**

Register Offset: **0x0D**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the source of the RDAT for the BERT. Note that the DS26303 must be in single-rail mode for BERT to function properly.

BRDAT	DESCRIPTION
0x00	RPOS Port 1
0x01	RPOS Port 2
0x02	RPOS Port 3
0x03	RPOS Port 4
0x04	RPOS Port 5
0x05	RPOS Port 6
0x06	RPOS Port 7
0x07	RPOS Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	TCLKBERT OUT
0x16-0xFF	HI-Z

Register Name: **TCLK**

Register Description: **PORT TCLK SOURCE**

Register Offset: **0x10**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Note: This is an indirect register that is related to ABSP (0x0A). See register description.

Bits 7 to 0: D7 to D0. These bits control the source of the port TCLK for the DS26303.

TCLK	DESCRIPTION
0x00	RCLK Port 1
0x01	RCLK Port 2
0x02	RCLK Port 3
0x03	RCLK Port 4
0x04	RCLK Port 5
0x05	RCLK Port 6
0x06	RCLK Port 7
0x07	RCLK Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	TCLKBERT OUT
0x16–0xFF	HI-Z

Register Name: **TPOS**

Register Description: **PORT TPOS SOURCE**

Register Offset: **0x11**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Note: This is an indirect register that is related to ABSP (0x0A). See register description.

Bits 7 to 0: D7 to D0. These bits control the source of the port TPOS for the DS26303.

TPOS	DESCRIPTION
0x00	RPOS Port 1
0x01	RPOS Port 2
0x02	RPOS Port 3
0x03	RPOS Port 4
0x04	RPOS Port 5
0x05	RPOS Port 6
0x06	RPOS Port 7
0x07	RPOS Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	TDATBERT OUT
0x16–0xFF	HI-Z

Register Name: **TNEG**

Register Description: **PORT TNEG SOURCE**

Register Offset: **0x12**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Note: This is an indirect register that is related to ABSP (0x0A). See register description.

Bits 7 to 0: D7 to D0. These bits control the source of the port TNEG for the DS26303.

TNEG	DESCRIPTION
0x00	RNEG Port 1
0x01	RNEG Port 2
0x02	RNEG Port 3
0x03	RNEG Port 4
0x04	RNEG Port 5
0x05	RNEG Port 6
0x06	RNEG Port 7
0x07	RNEG Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	Drive Logic "0"
0x16–0xFF	HI-Z

DS26303 INFORMATION

For more information about the DS26303, refer to the DS26303 data sheet available on our website at www.maxim-ic.com/DS26303.

DS26303DK INFORMATION

For more information about the DS26303DK including software downloads, go to www.maxim-ic.com/DS26303DK.

TECHNICAL SUPPORT

For additional technical support, e-mail your questions to telecom.support@dalsemi.com.

SCHEMATICS

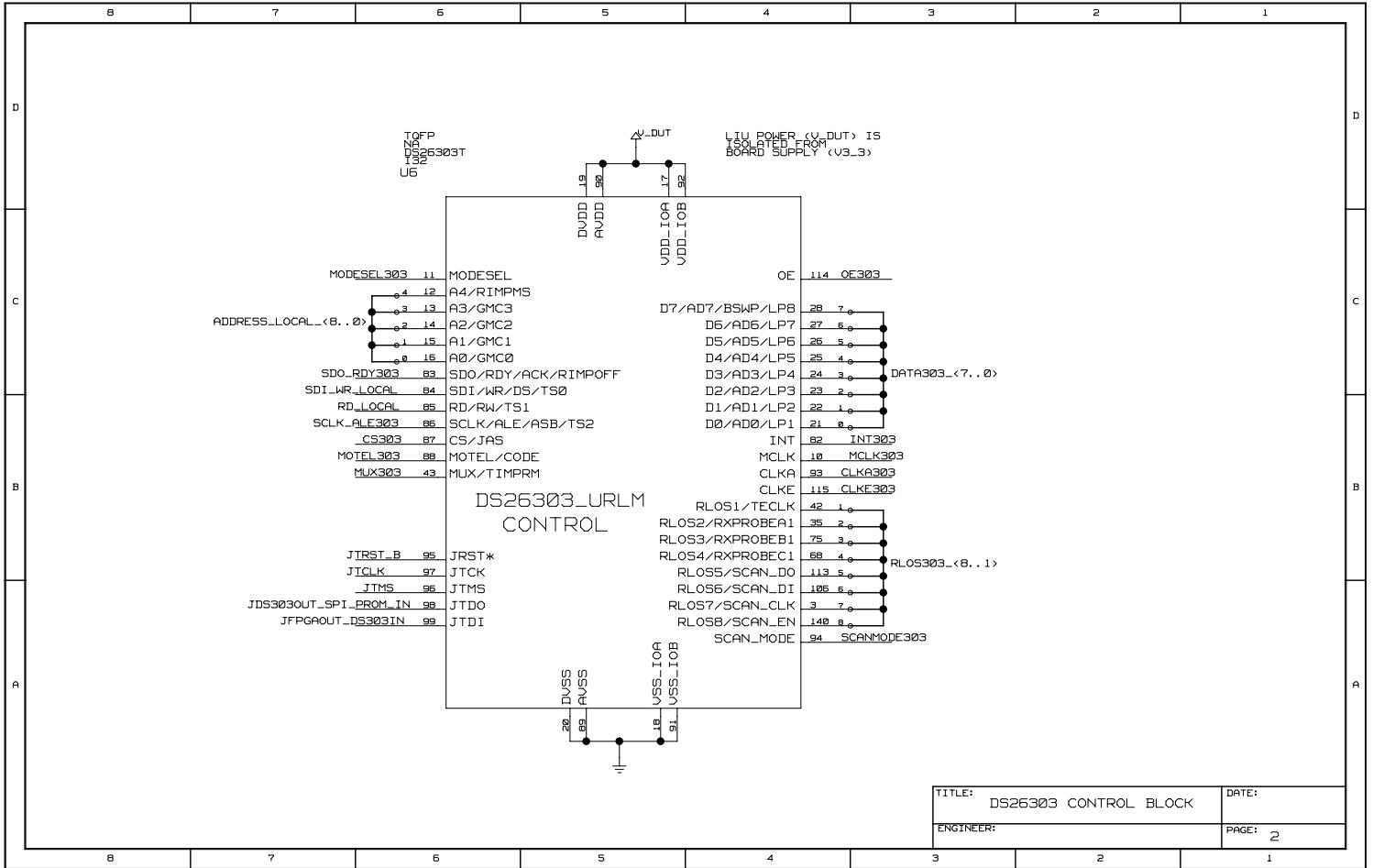
The DS26303DK schematics are featured in the following 22 pages.

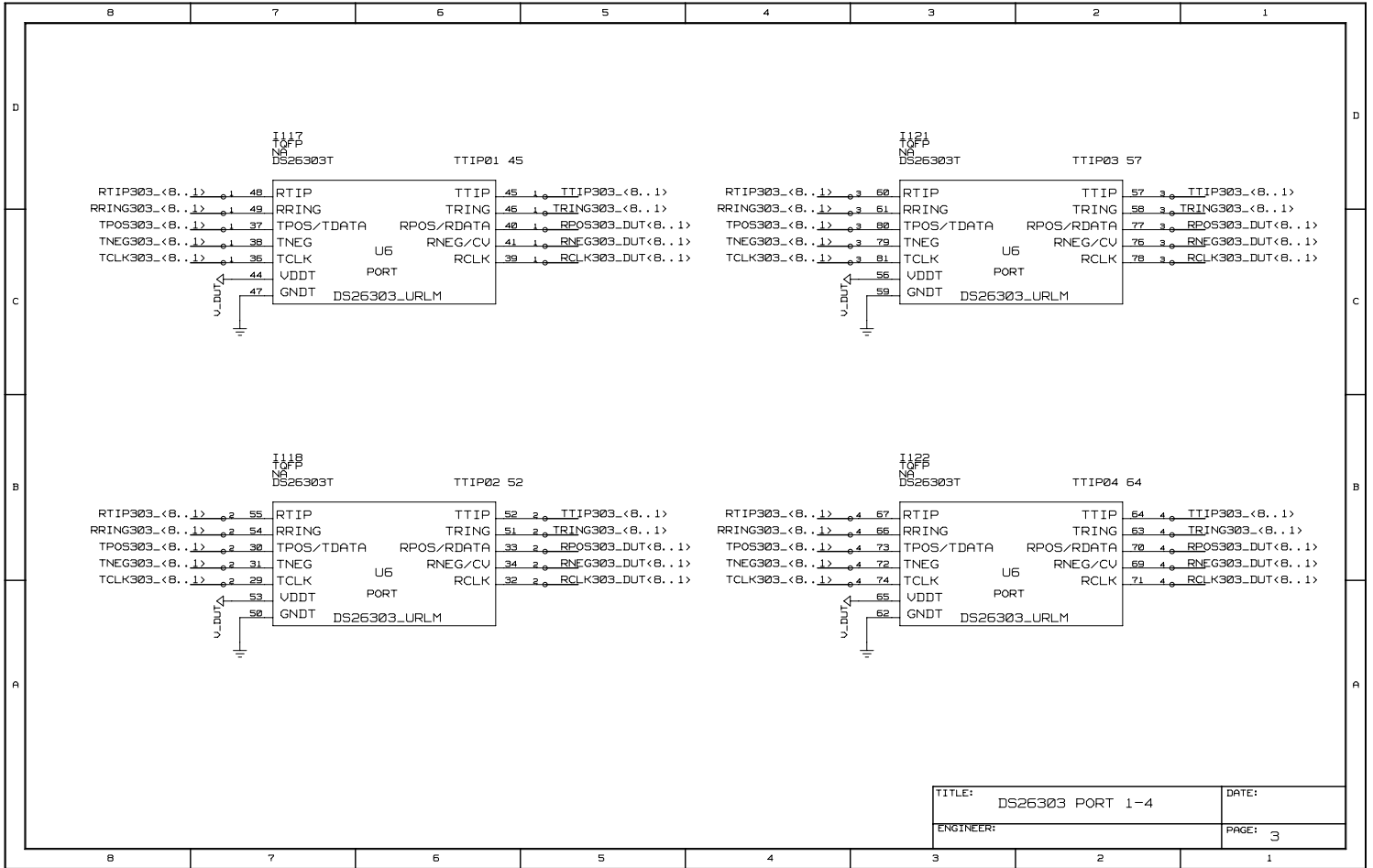
DS26303 DESIGN KIT
SCHEMATIC
DALLAS SEMICONDUCTOR / MAXIM
AUGUST 2005

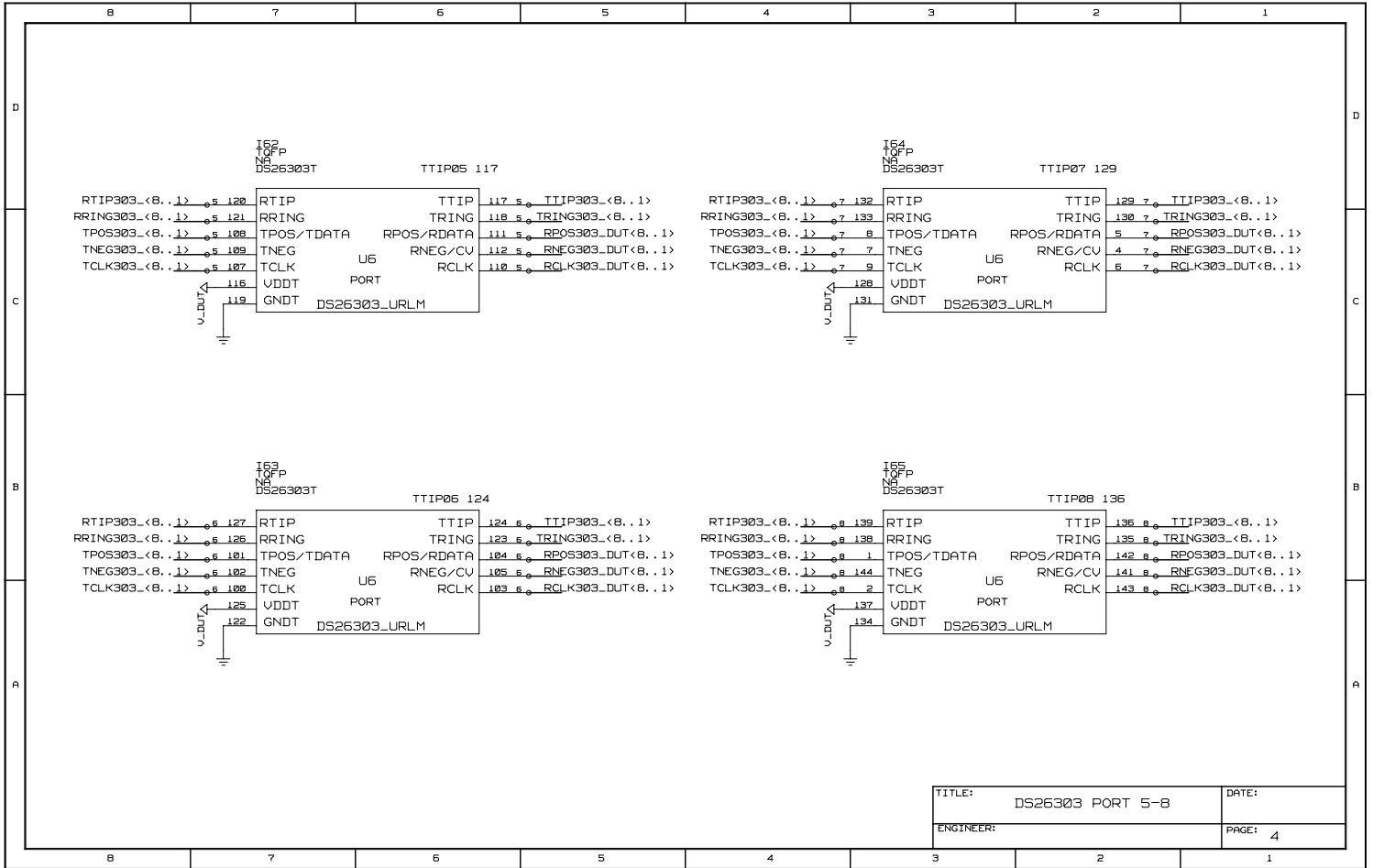
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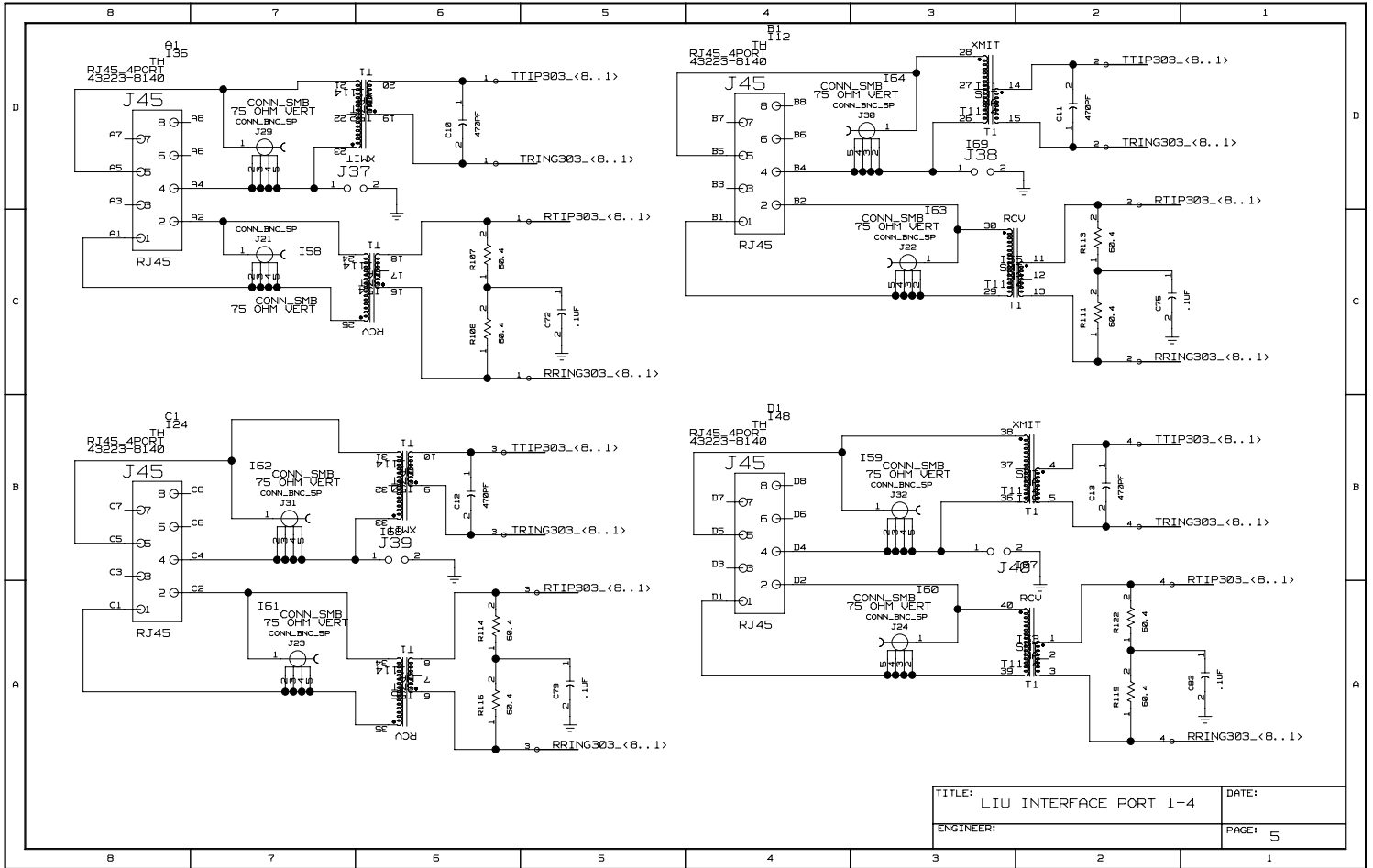
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2. DS26303 CONTROL BLOCK	10. FPGA PORT A	18. POWER CON
3. DS26303 PORT 1-4	11. FPGA PORT B	19. NOTES
4. DS26303 PORT 5-8	12. SERIAL, JTAG and USB	20. SIGNAL CROSS REF
5. LIU INTERFACE PORT 1-4	13. MICRO-CONTROLLER	21. PART CROSS REF P-1
6. LIU INTERFACE PORT 5-8	14. SRAM	
7. RLOS, INT and LEDs	15. TESTPOINTS	
8. BERT and SPI PROM	16. SERIAL TERMINATION	

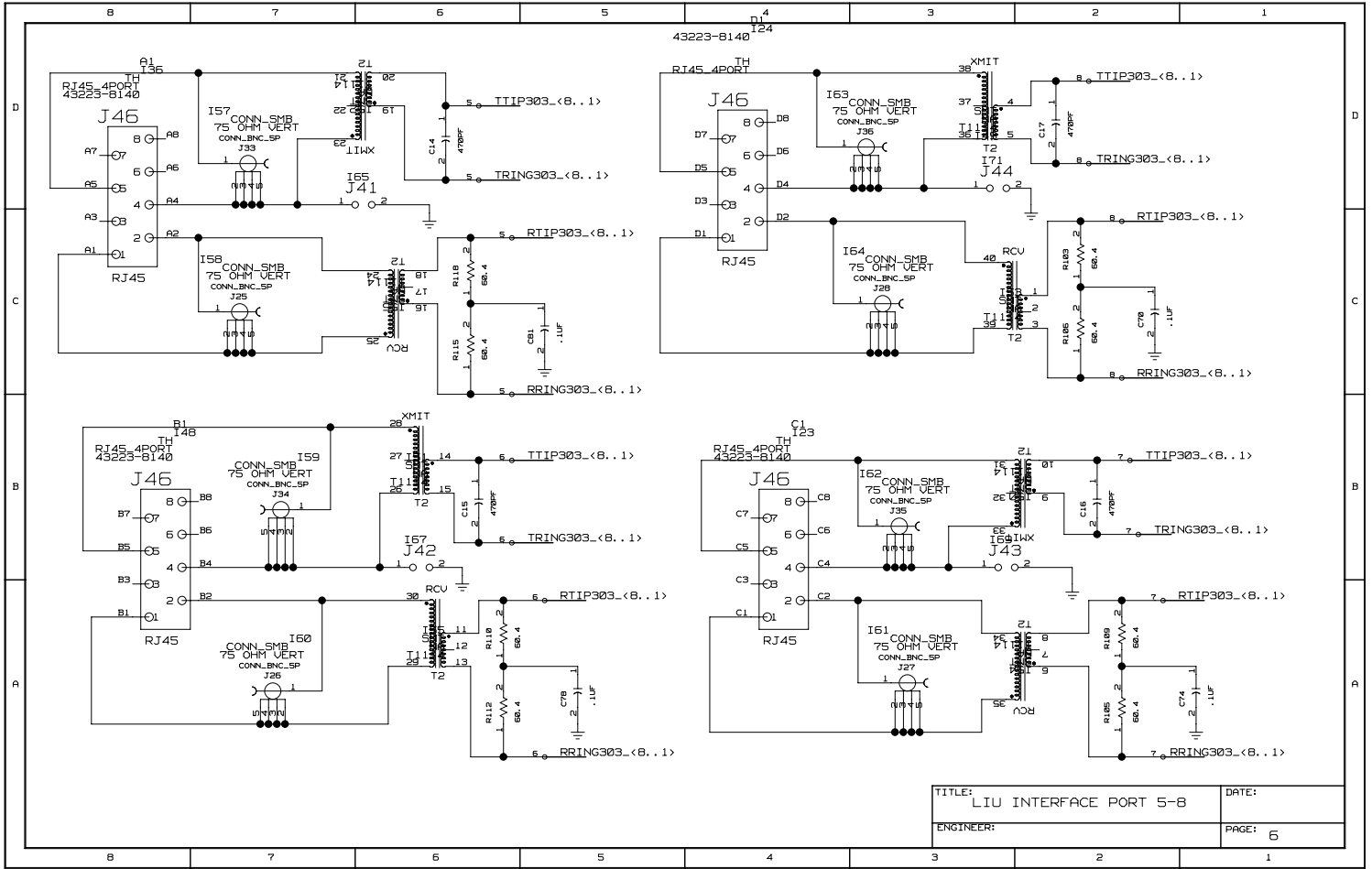
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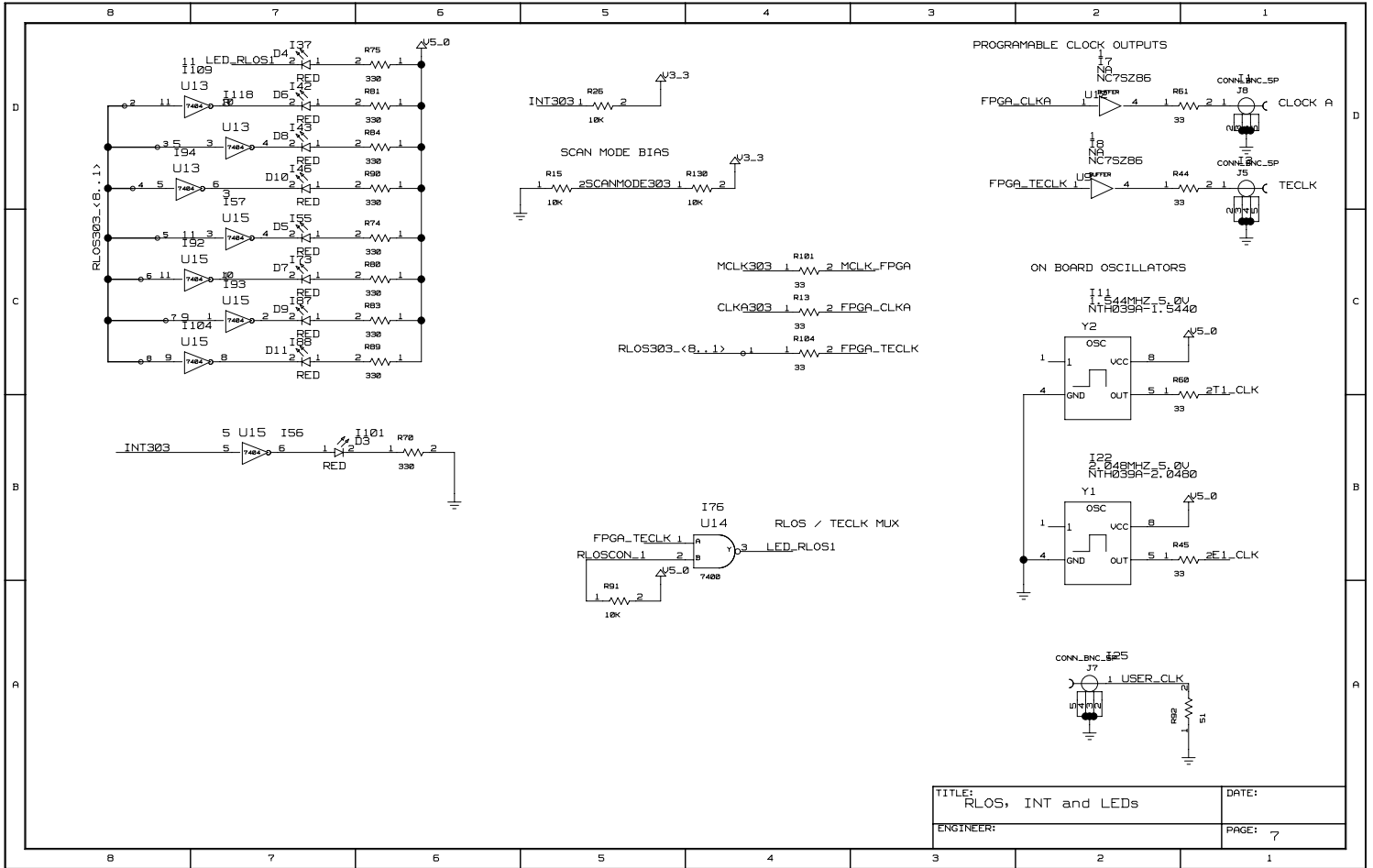




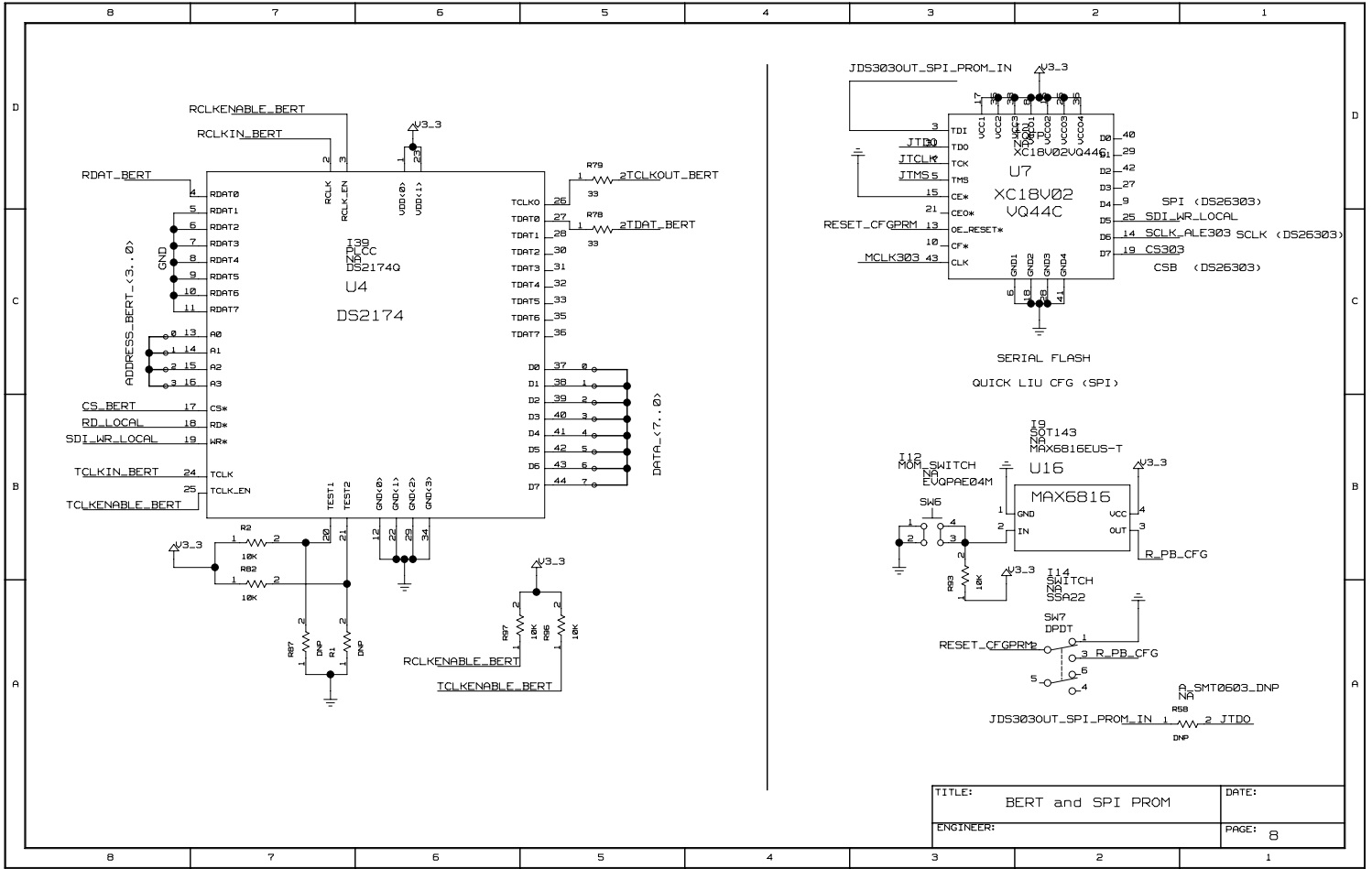




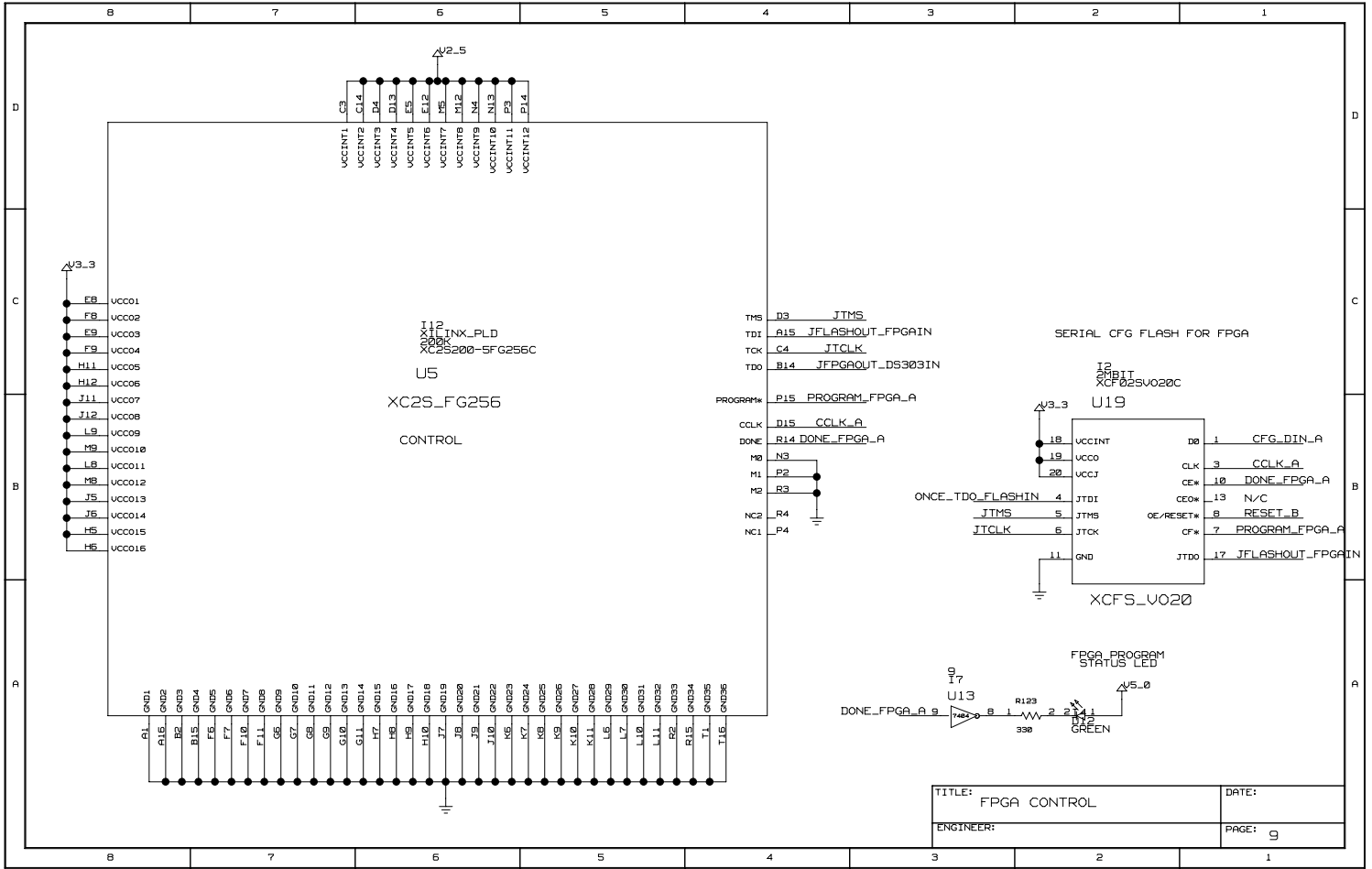


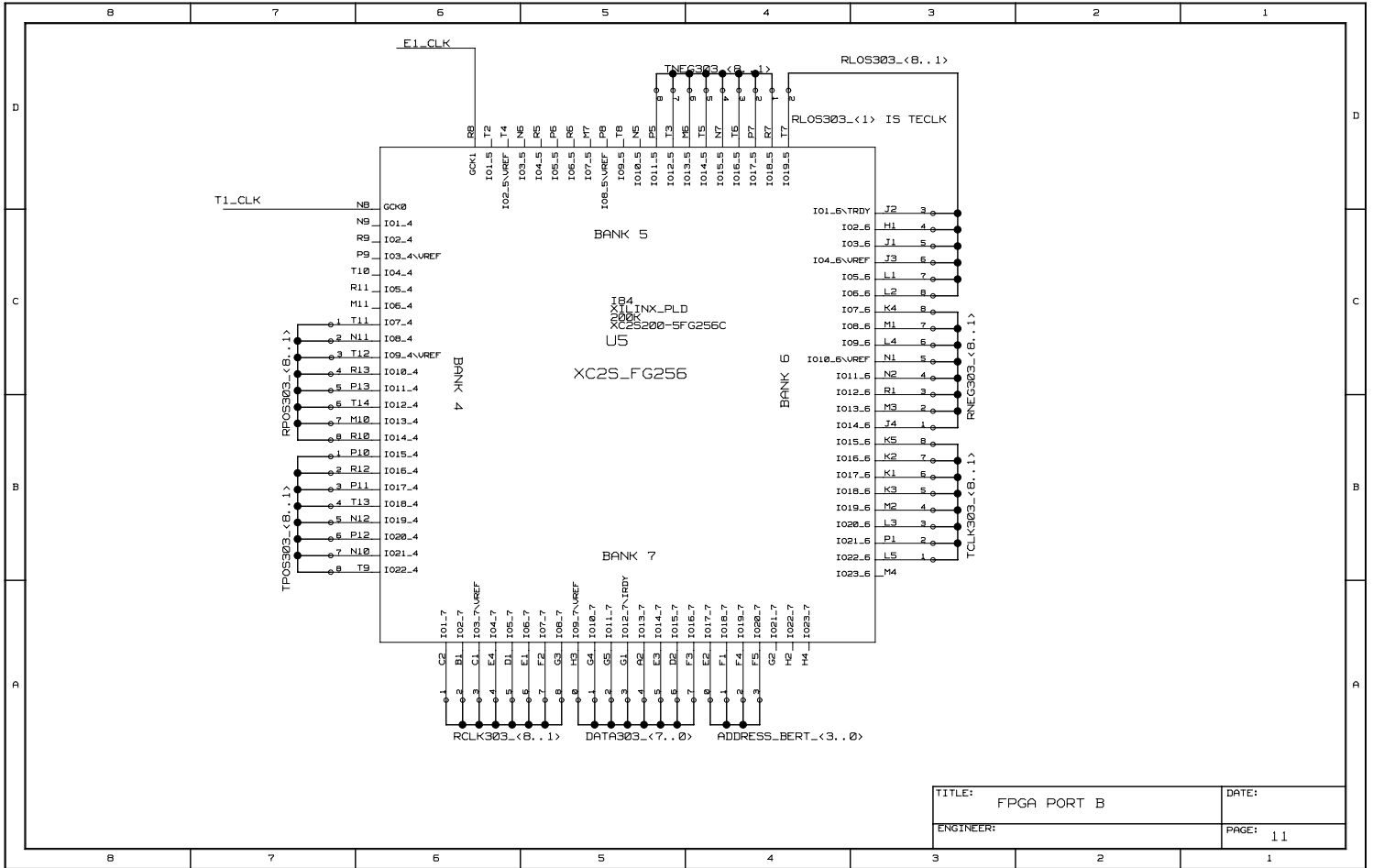


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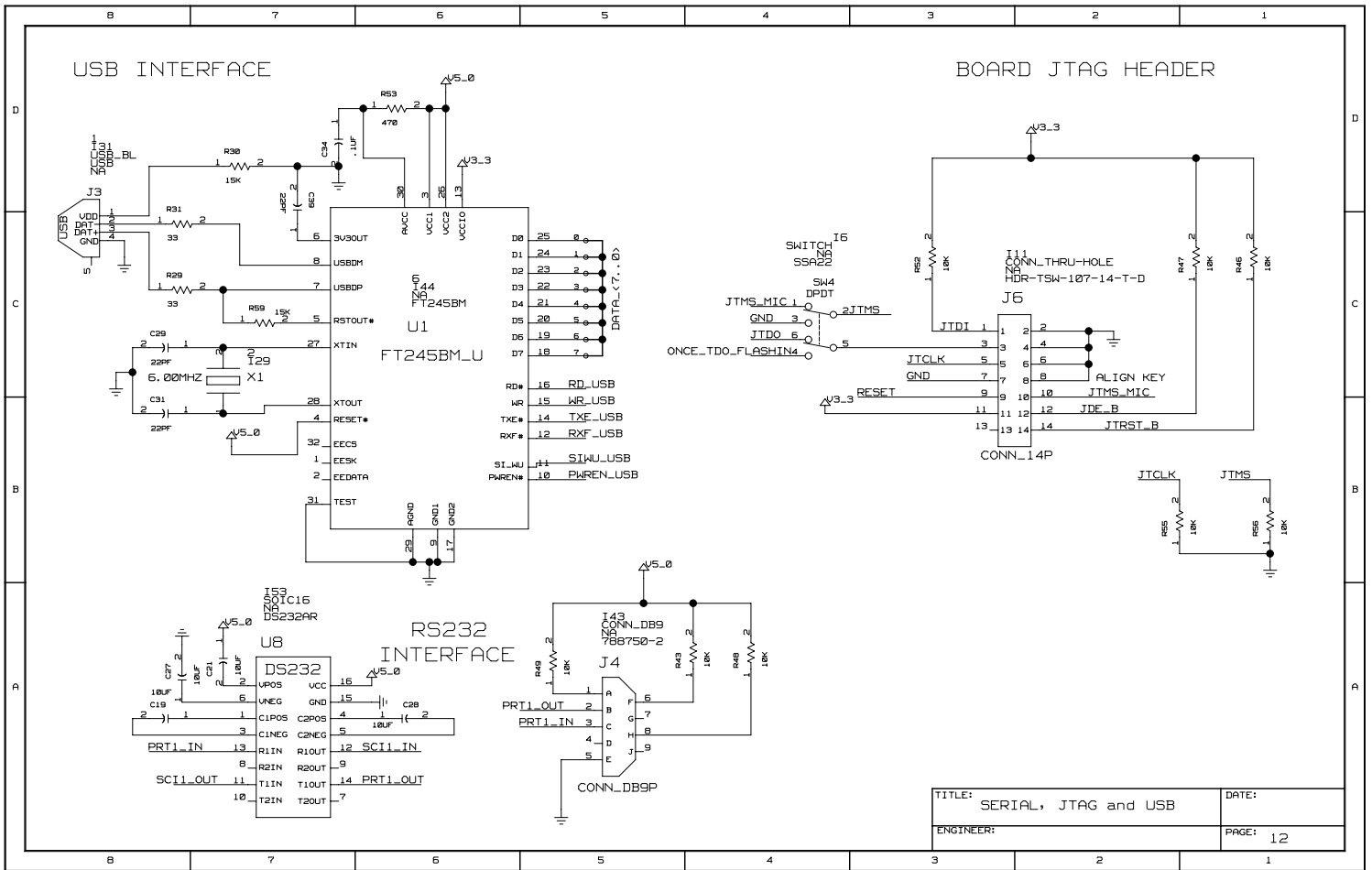


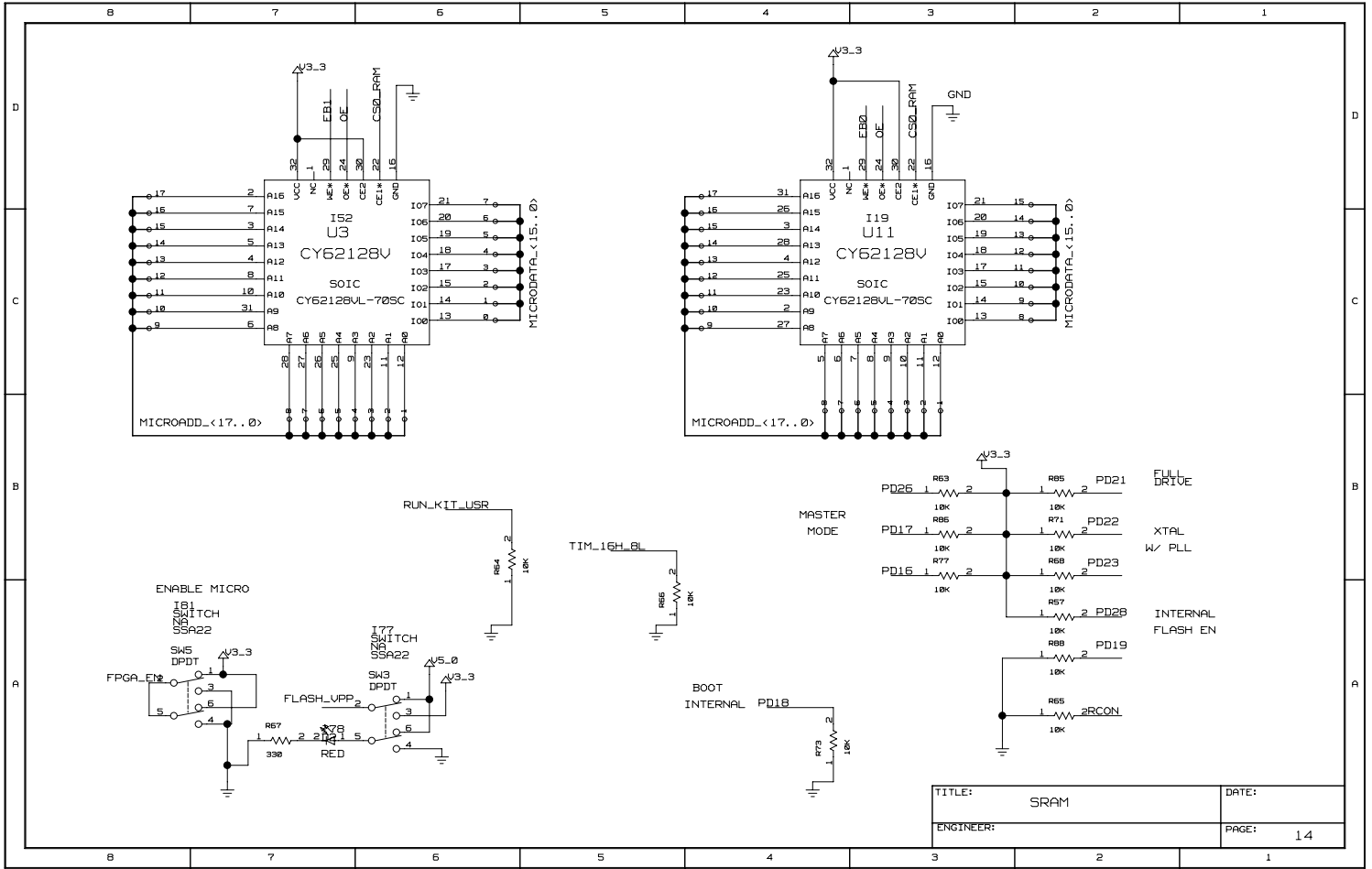
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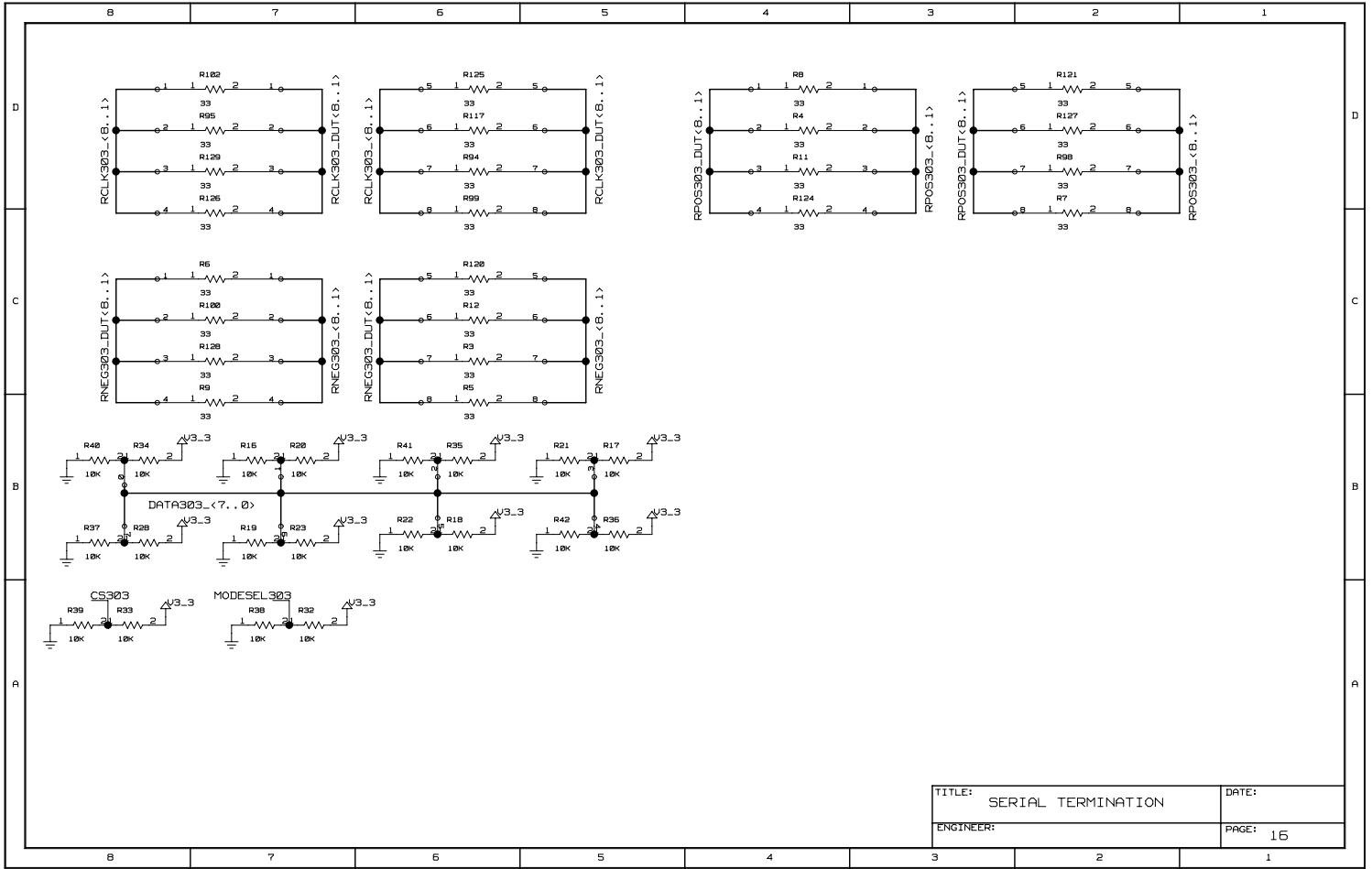


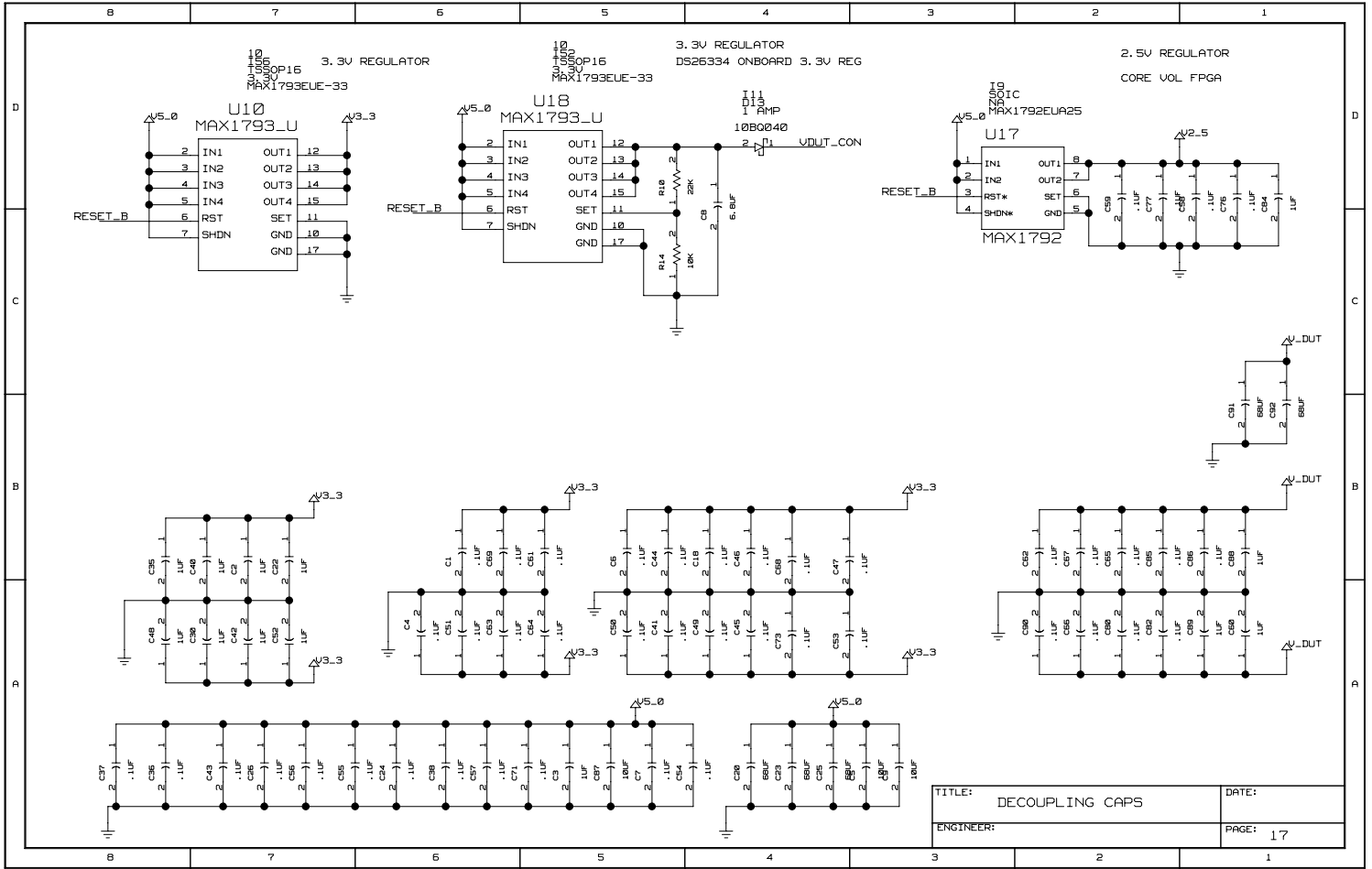


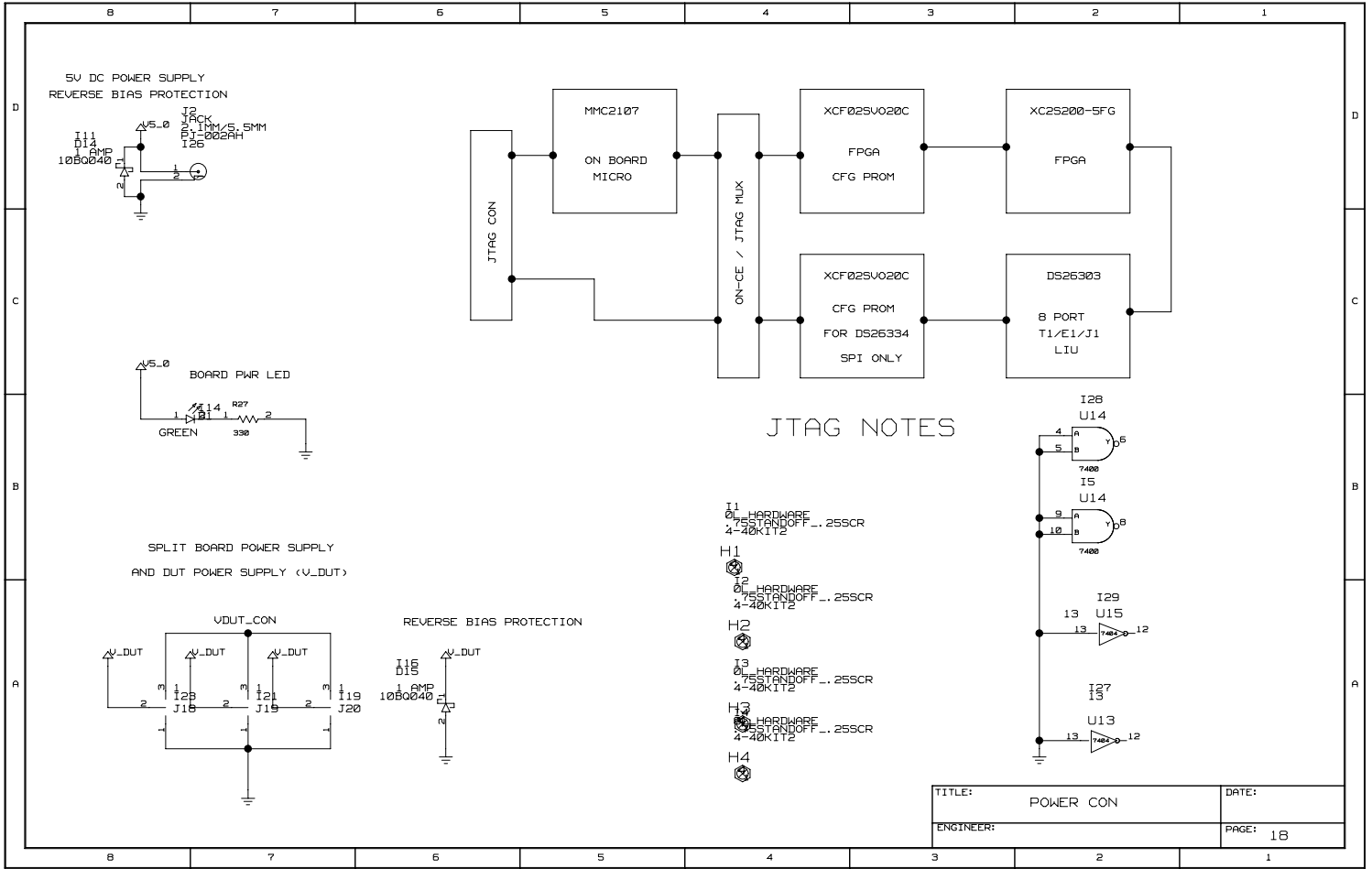
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ENGINEER:	PAGE: 11













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						ENGINEER:		PAGE:	

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	B	7	6	5	4	3	2	1
	*** Part Cross-Reference for the entire design ***							
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	C3 CXP1 1785	C83 CXP1 5A1	C84 CXP1 17C1	C85 CXP1 17B2	C86 CXP1 17B1	C87 CXP1 17A5	C88 CXP1 17B1	C89 CXP1 17A1
	C4 CXP1 17A5	C90 CXP1 17A2	C91 CXP1 17B1	C92 CXP1 17B1	D2 LED 14A7	D3 LED 7B7	D4 LED 7D7	D5 LED 7C7
	C5 CXP1 17A5	C93 CXP1 17B1	D6 LED 7D7	D7 LED 7C7	D8 LED 7D7	D9 LED 7C7	D10 LED 7D7	D11 LED 7C7
	C6 CXP1 17B5	C94 CXP1 17A1	D12 LED 9A2	D13 SCHOTTKYDIODE1 17D4	D14 SCHOTTKYDIODE1 18D8	D15 SCHOTTKYDIODE1 18A6	H1 4_48_HDMR 18B1	H2 4_48_HDMR 18B1
	C7 CXP1 17A5	C95 CXP1 17A7	H3 4_48_HDMR 18A1	H4 4_48_HDMR 18A1	J1 CONN_4BP 15A5	J2 POWER JACK 18D8	J3 USB_CONN_LJ 12D8	J4 CONN_DBSP 12A5
	C8 CXP1 17A3	C96 CXP1 12A8	J5 CONN_L4BP 12C3	J7 CONN_L4BP 7A2	J8 CONN_L4BP 7D1	J9 CONN_L4BP 15D7	J10 CONN_L4BP 15B8	J11 CONN_L4BP 15D7
	C9 CXP1 17A3	C97 CXP1 17A7	J12 CONN_L4BP 15C7	J13 CONN_L4BP 15D5	J14 CONN_L4BP 15B6	J15 CONN_L4BP 15D5	J16 CONN_L4BP 15C4	J17 CONN_L4BP 15A7
	C10 CXP1 5D5	C98 CXP1 17A4	J18 JMP3 18A7	J19 JMP3 18A7	J20 JMP3 18A7	J21 CONN_L4BP 5C7	J22 CONN_L4BP 5C3	J23 CONN_L4BP 5A7
	C11 CXP1 5D5	C99 CXP1 17A4	J24 CONN_L4BP 5A3	J25 CONN_L4BP 5C7	J26 CONN_L4BP 5A7	J27 CONN_L4BP 5A3	J28 CONN_L4BP 5C3	J29 CONN_L4BP 5D7
	C12 CXP1 5B2	C100 CXP1 17A4	J30 CONN_L4BP 5D3	J31 CONN_L4BP 5B7	J32 CONN_L4BP 5B3	J33 CONN_L4BP 5B7	J34 CONN_L4BP 5B7	J35 CONN_L4BP 5B3
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	C14 CXP1 5D6	C102 CXP1 17A4	J42 JMP_OPEN_LP 5B6	J43 JMP_OPEN_LP 5B3	J44 JMP_OPEN_LP 5D3	J45 RJ45_8 5B4 5B8 5D4 5D8	J46 RJ45_8 6B4 6B8 6D4 6D8	L1 COIL_LP 13D6
	C15 CXP1 5B6	C103 CXP1 17A4	R1 RES1 8A7	R2 RES1 8B7	R3 RES1 16C5	R4 RES1 16D4	R5 RES1 16C5	R6 RES1 16C7
	C16 CXP1 6B2	C104 CXP1 17A4	R7 RES1 16D4	R8 RES1 16D4	R9 RES1 16C7	R10 RES1 17D5	R11 RES1 16D4	R12 RES1 16C5
	C17 CXP1 6D2	C105 CXP1 17A4	R13 RES1 7C4	R14 RES1 17C5	R15 RES1 7D5	R16 RES1 16B7	R17 RES1 16B5	R18 RES1 16B5
	C18 CXP1 17A4	C106 CXP1 17A4	R19 RES1 16B7	R20 RES1 16B7	R21 RES1 16B5	R22 RES1 16B6	R23 RES1 16B7	R24 RES1 13A1
	C19 CXP1 12A8	C107 CXP1 17A4	R25 RES1 13A1	R26 RES1 7D5	R27 RES1 16B7	R28 RES1 16B8	R29 RES1 16B7	R30 RES1 12D7
	C20 CXP1 17A4	C108 CXP1 17A4	R31 RES1 12C3	R32 RES1 16A7	R33 RES1 16A8	R34 RES1 16B8	R35 RES1 16B6	R36 RES1 16B5
	C21 CXP1 12A7	C109 CXP1 17A4	R37 RES1 16B8	R38 RES1 16A7	R39 RES1 16A8	R40 RES1 16B8	R41 RES1 16B6	R42 RES1 16B5
	C22 CXP1 17B7	C110 CXP1 17A4	R43 RES1 12A5	R44 RES1 7B2	R45 RES1 7B2	R46 RES1 12C1	R47 RES1 12C1	R48 RES1 12A4
	C23 CXP1 17A4	C111 CXP1 17A4	R49 RES1 12A5	R50 RES1 13A7	R51 RES1 13A4	R52 RES1 12C3	R53 RES1 12B6	R54 RES1 13A7
	C24 CXP1 17A5	C112 CXP1 17A4	R55 RES1 12B2	R56 RES1 12B1	R57 RES1 14A2	R58 RES1 12C7	R59 RES1 7C2	R60 RES1 7C2
	C25 CXP1 17A4	C113 CXP1 17A4	R61 RES1 7D2	R62 RES1 13D4	R63 RES1 14B3	R64 RES1 14B6	R65 RES1 14A2	R66 RES1 14A5
	C26 CXP1 17A7	C114 CXP1 17A4	R67 RES1 14A7	R68 RES1 14B2	R69 RES1 13A1	R70 RES1 7B6	R71 RES1 14B2	R72 RES1 13A2
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	C29 CXP1 12C8	C117 CXP1 17A4	R85 RES1 14B2	R86 RES1 14B3	R87 RES1 8A7	R88 RES1 14A2	R89 RES1 7C5	R90 RES1 7D6
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	C32 CXP1 13A4	C120 CXP1 17A4	R103 RES1 15C7	R104 RES1 7C4	R105 RES1 6A2	R106 RES1 6C2	R107 RES1 5C5	R108 RES1 6A2
	C33 CXP1 17A4	C121 CXP1 17A4	R109 RES1 6A2	R110 RES1 6A6	R111 RES1 5C2	R112 RES1 6A6	R113 RES1 5C2	R114 RES1 5A6
	C34 CXP1 12D7	C122 CXP1 17A4	R115 RES1 5C5	R116 RES1 5A6	R117 RES1 15D6	R118 RES1 5C5	R119 RES1 5A2	R120 RES1 15C5
	C35 CXP1 17B8	C123 CXP1 17A4	R121 RES1 15D2	R122 RES1 5A2	R123 RES1 5A2	R124 RES1 15D4	R125 RES1 15D6	R126 RES1 15D7
	C36 CXP1 17A8	C124 CXP1 17A4	R127 RES1 15D2	R128 RES1 15C7	R129 RES1 15D7	R130 RES1 7D4	S42 PUSHBUTTON 13A8	S43 SWITCH_DPDT_SLIDE_GP 14A6
	C37 CXP1 17A8	C125 CXP1 17A4	R131 RES1 15C7	R132 RES1 15C7	R133 RES1 7D4	S44 SWITCH_DPDT_SLIDE_GP 12C4	S45 SWITCH_DPDT_SLIDE_GP 14A8	S46 PUSHBUTTON 8B3
	C38 CXP1 17A6	C126 CXP1 17A4	R134 RES1 15C7	R135 RES1 15C5	T1 XPRL_QUADPART_T1_LJ 5A2 5A6 5B2 5B6 5C2 5C5 5D3 5D5	T2 XPRL_QUADPART_T1_LJ 6A2 6A6 6B2 6B6 6C2 6C5	U1 FT245BLU 12C5	
	C39 CXP1 17A6	C127 CXP1 17A4	R136 RES1 14A5	R137 RES1 14A7	U2 HYC2187L1 13C2 13C6	U3 C74515N-2 14C7	U4 DS9174 8C7	U5 XC2B_F0256 9C5 10C5 11C5
	C40 CXP1 17A4	C128 CXP1 17A4	R138 RES1 13A1	R139 RES1 13A1	U6 XC2B0303C1 12B6 3A3 3B6 3C3 3C6 4B3 4B6 4C3 4C6	U7 XC18M2V044C 8D3		
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	C42 CXP1 17A7	C130 CXP1 17A4	R142 RES1 14A7	R143 RES1 14A7				
	C43 CXP1 17A7	C131 CXP1 17A4	R144 RES1 14A2	R145 RES1 14A2				
	C44 CXP1 17B5	C132 CXP1 17A4	R146 RES1 14A5	R147 RES1 14A7				
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		C206 CXP1 17A4	R2					

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