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Texas Instruments
ADS1174IPAPT

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TEXAS INSTRUMENTS

**ADS1174**
**ADS1178**

# Quad/Octal, Simultaneous Sampling, 16-Bit Analog-to-Digital Converters

## FEATURES

- **Simultaneously Sample Four/Eight Channels**
- **Selectable Operating Modes:**
  **High-Speed: 52kSPS Data Rate, 31mW/ch**
  **Low-Power: 10kSPS Data Rate, 7mW/ch**
- **AC Performance:**
  **25kHz Bandwidth**
  **97dB SNR**
  **−105dB THD**
- **DC Performance:**
  **2μV/°C Offset Drift**
  **2ppm/°C Gain Drift**
- **Digital Filter:**
  **Linear Phase Response**
  **Passband Ripple: ±0.005dB**
  **Stop Band Attenuation: 100dB**
- **Selectable SPI™ or Frame Sync Serial Interface**
- **Simple Pin-Driven Control**
- **Low Sampling Aperture Error**
- **Specified from −40°C to +105°C**
- **Analog Supply: 5V**
- **I/O Supply: 1.8V to 3.3V**
- **Digital Core Supply: 1.8V**

## APPLICATIONS

- **3-Phase Power Monitors**
- **Defibrillators and ECG Monitors**
- **Coriolis Flow Meters**
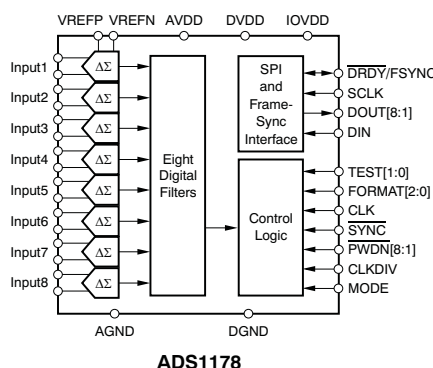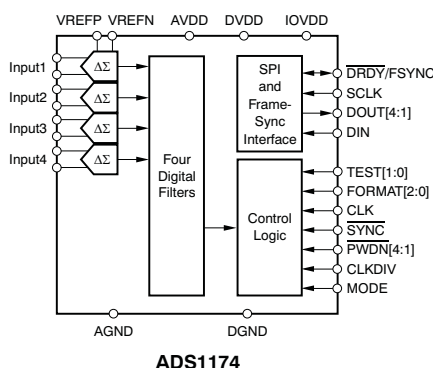- **Vibration/Modal Analysis**

## DESCRIPTION

The ADS1174 (quad) and ADS1178 (octal) are multiple delta-sigma (ΔΣ) analog-to-digital converters (ADCs) with data rates up to 52k samples-per-second (SPS), which allow synchronous sampling of four and eight channels. These devices use identical packages, and are also compatible with the high-performance 24-bit ADS1274 and ADS1278, permitting drop-in upgrades.

The delta-sigma architecture offers near ideal 16-bit ac performance (97dB SNR, −105dB THD, 1LSB linearity) combined with 0.005dB passband ripple and linear phase response.

The high-order, chopper-stabilized modulator achieves very low drift (2μV/°C offset, 2ppm/°C gain) and low noise (1LSB$_{PP}$). The on-chip finite impulse response (FIR) filter provides a usable signal bandwidth up to 90% of the Nyquist rate with 100dB of stop band attenuation while suppressing modulator and signal out-of-band noise.

Two operating modes allow for optimization of speed and power: High-speed mode (31mW/Ch at 52kSPS), and Low-power mode (7mW/Ch at 10kSPS).

A $\overline{\text{SYNC}}$ input control pin allows the device conversions to be started and synchronized to an external event. SPI and Frame-Sync serial interfaces are supported. The device is fully specified over the extended industrial range (−40°C to +105°C) and is available in an HTQFP-64 PowerPAD™ package.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

| PARAMETER | ADS1174, ADS1178 | UNIT |
|---|---|---|
| AVDD to AGND | −0.3 to +6.0 | V |
| DVDD, IOVDD to DGND | −0.3 to +3.6 | V |
| AGND to DGND | −0.3 to +0.3 | V |
| Input Current | 100, Momentary | mA |
| | 10, Continuous | mA |
| Analog Input to AGND | −0.3 to AVDD + 0.3 | V |
| Digital Input or Output to DGND | −0.3 to IOVDD + 0.3 | V |
| Maximum Junction Temperature | +150 | °C |
| Operating Temperature Range | −40 to +125 | °C |
| Storage Temperature Range | −60 to +150 | °C |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

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## ELECTRICAL CHARACTERISTICS

Limit specifications at $T_A$ = −40°C to +105°C. Typical specifications at $T_A$ = +25°C, AVDD = +5V, DVDD = +1.8V, IOVDD = +3.3V, $f_{CLK}$ = 27MHz, VREFP = 2.5V, VREFN = 0V, and all channels active, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | ADS1174, ADS1178 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **ANALOG INPUTS** | | | | | | |
| Full-scale input voltage (FSR[1]) | | $V_{IN}$ = (AINP − AINN) | | $\pm V_{REF}$ | | V |
| Absolute input voltage | | AINP or AINN to AGND | AGND − 0.1 | | AVDD + 0.1 | V |
| Common-mode input voltage | | $V_{CM}$ = (AINP + AINN)/2 | | 2.5 | | V |
| Differential input impedance | High-Speed mode | | | 28 | | kΩ |
| | Low-Power mode | | | 140 | | kΩ |
| **DC PERFORMANCE** | | | | | | |
| Resolution | | No missing codes | 16 | | | Bits |
| Data rate ($f_{DATA}$) | High-Speed mode | | | 52,734 | | SPS |
| | Low-Power mode | | | 10,547 | | SPS |
| Integral nonlinearity (INL)[2] | | Differential input | | ±0.3 | ±1 | LSB |
| Offset error | | | | 0.3 | 2 | mV |
| Offset drift | | | | 2 | | μV/°C |
| Gain error | | | | 0.1 | 0.5 | % |
| Gain drift | | | | 2 | | ppm/°C |
| Noise | | Shorted input | | 1 | | $LSB_{PP}$ |
| Common-mode rejection | | $f_{CM}$ = 60Hz[3] | | 100 | | dB |
| Power-supply rejection | AVDD | $f_{PS}$ = 60Hz[3] | | 75 | | dB |
| | DVDD | $f_{PS}$ = 60Hz[3] | | 85 | | dB |
| | IOVDD | $f_{PS}$ = 60Hz[3] | | 90 | | dB |
| $V_{COM}$ output voltage | | No load | | AVDD/2 | | V |
| **AC PERFORMANCE** | | | | | | |
| Crosstalk | | $V_{IN}$ = 1kHz, −0.5dBFS | | −107 | | dB |
| Signal-to-noise ratio (SNR) (unweighted) | | $V_{IN}$ = 1kHz, −0.5dBFS | 92 | 97 | | dB |
| Total harmonic distortion (THD)[4] | High-Speed mode | $V_{IN}$ = 1kHz, −0.5dBFS | | −105 | −96 | dB |
| Spurious-free dynamic range | | | | 106 | | dB |
| Passband ripple | | | | | ±0.005 | dB |
| Passband | | | | 0.453 $f_{DATA}$ | | Hz |
| −3dB Bandwidth | | | | 0.49 $f_{DATA}$ | | Hz |
| Stop band attenuation | | | 100 | | | dB |
| Stop band | | | 0.547 $f_{DATA}$ | | 63.453 $f_{DATA}$ | Hz |
| Group delay | | | | 38/$f_{DATA}$ | | s |
| Settling time (latency) | | Complete settling | | 76/$f_{DATA}$ | | s |

(1)  FSR = full-scale range = $2V_{REF}$
(2)  Best-fit method.
(3)  $f_{CM}$ is the input common-mode frequency. $f_{PS}$ is the power-supply frequency.
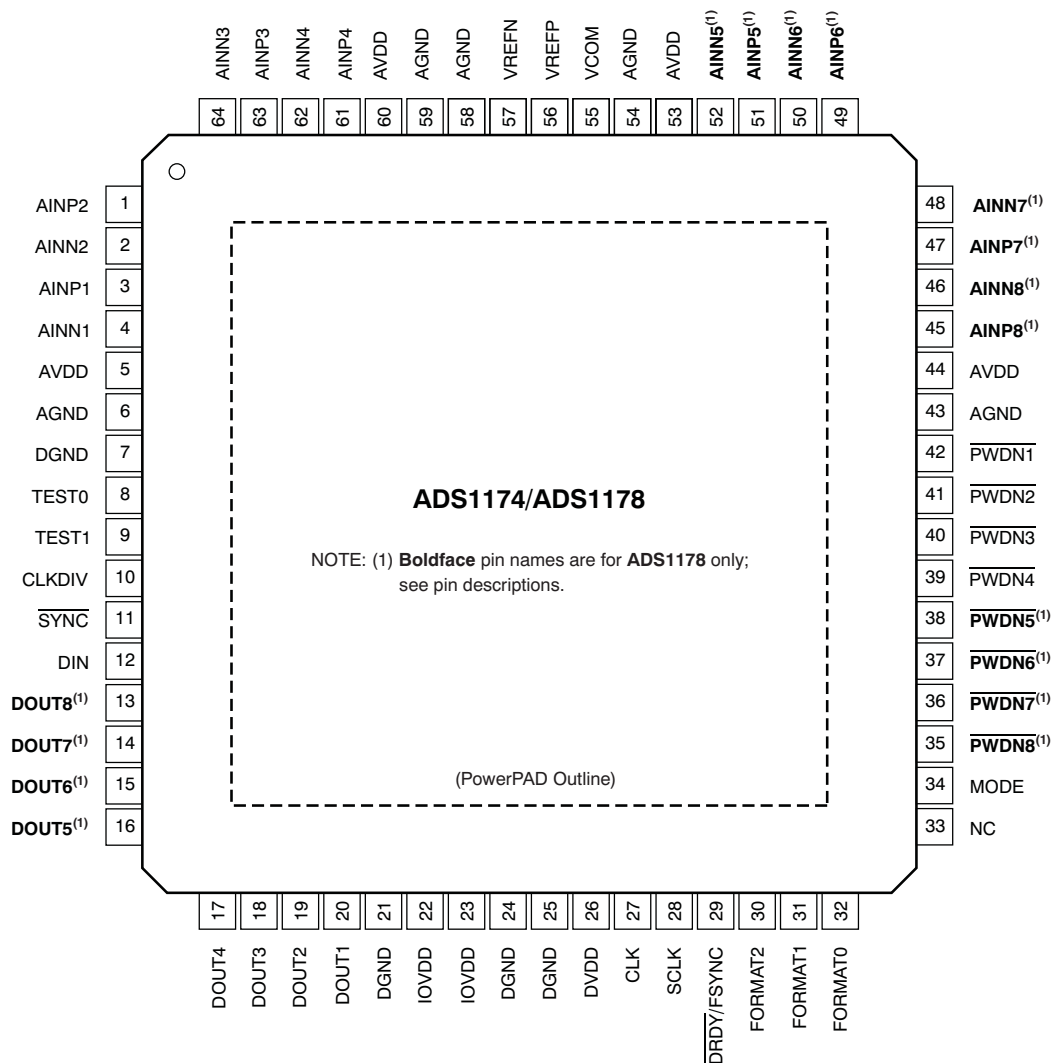(4)  THD includes the first nine harmonics of the input signal.

Product Folder Link(s): *ADS1174 ADS1178*

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## ELECTRICAL CHARACTERISTICS (continued)

Limit specifications at $T_A$ = −40°C to +105°C. Typical specifications at $T_A$ = +25°C, AVDD = +5V, DVDD = +1.8V, IOVDD = +3.3V, $f_{CLK}$ = 27MHz, VREFP = 2.5V, VREFN = 0V, and all channels active, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | ADS1174, ADS1178 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **VOLTAGE REFERENCE INPUTS** | | | | | | |
| Reference input voltage ($V_{REF}$) | | $V_{REF}$ = VREFP – VREFN | 0.5 | 2.5 | 3.1 | V |
| Negative reference input (VREFN) | | | AGND – 0.1 | | AGND + 0.1 | V |
| Positive reference input (VREFP) | | | VREFN + 0.5 | | VREFN + 3.1 | V |
| ADS1174 Reference Input impedance | High-Speed mode | | | 2.6 | | kΩ |
| | Low-Power mode | | | 13 | | kΩ |
| ADS1178 Reference Input impedance | High-Speed mode | | | 1.3 | | kΩ |
| | Low-Power mode | | | 6.5 | | kΩ |
| **DIGITAL INPUT/OUTPUT (IOVDD = 1.8V to 3.6V)** | | | | | | |
| $V_{IH}$ | | | 0.7 IOVDD | | IOVDD | V |
| $V_{IL}$ | | | DGND | | 0.3 IOVDD | V |
| $V_{OH}$ | | $I_{OH}$ = 4mA | 0.8 IOVDD | | IOVDD | V |
| $V_{OL}$ | | $I_{OL}$ = 4mA | DGND | | 0.2 IOVDD | V |
| Input leakage | | 0 < $V_{IN\ DIGITAL}$ < IOVDD | | | ±10 | µA |
| Master clock rate ($f_{CLK}$) | | | 0.1 | | 27 | MHz |
| **POWER SUPPLY** | | | | | | |
| AVDD | | | 4.75 | 5 | 5.25 | V |
| DVDD | | | 1.65 | 1.8 | 1.95 | V |
| IOVDD | | | 1.65 | | 3.6 | V |
| Power-down current | AVDD | | | 1 | 10 | µA |
| | DVDD | | | 1 | 15 | µA |
| | IOVDD | | | 1 | 10 | µA |
| **ADS1174** | | | | | | |
| ADS1174 AVDD current | High-Speed mode | | | 23 | 35 | mA |
| | Low-Power mode | | | 5 | 9 | mA |
| ADS1174 DVDD current | High-Speed mode | | | 10 | 15 | mA |
| | Low-Power mode | | | 2.5 | 4.5 | mA |
| ADS1174 IOVDD current | High-Speed mode | | | 0.075 | 0.3 | mA |
| | Low-Power mode | | | 0.02 | 0.15 | mA |
| ADS1174 Power dissipation | High-Speed mode | | | 135 | 210 | mW |
| | Low-Power mode | | | 30 | 55 | mW |
| **ADS1178** | | | | | | |
| ADS1178 AVDD current | High-Speed mode | | | 44 | 64 | mA |
| | Low-Power mode | | | 9 | 14 | mA |
| ADS1178 DVDD current | High-Speed mode | | | 12 | 17 | mA |
| | Low-Power mode | | | 3 | 4.5 | mA |
| ADS1178 IOVDD current | High-Speed mode | | | 0.125 | 0.5 | mA |
| | Low-Power mode | | | 0.035 | 0.2 | mA |
| ADS1178 Power dissipation | High-Speed mode | | | 245 | 355 | mW |
| | Low-Power mode | | | 50 | 80 | mW |

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## ADS1174/ADS1178 PIN ASSIGNMENTS

PAP PACKAGE
HTQFP-64
(TOP VIEW)



## ADS1174/ADS1178 PIN DESCRIPTIONS

| PIN | | | |
|---|---|---|---|
| NAME | NO. | FUNCTION | DESCRIPTION |
| AGND | 6, 43, 54, 58, 59 | Analog ground | Analog ground; connect to DGND using a single plane. |
| AINP1 | 3 | Analog input | |
| AINP2 | 1 | Analog input | |
| AINP3 | 63 | Analog input | **ADS1178:** AINP[8:1] Positive analog input, channels 8 through 1. |
| AINP4 | 61 | Analog input | |
| AINP5 | 51 | Analog input | **ADS1174:** AINP[8:5] Connected to internal ESD rails. The inputs may float. |
| AINP6 | 49 | Analog input | AINP[4:1] Positive analog input, channels 4 through 1. |
| AINP7 | 47 | Analog input | |
| AINP8 | 45 | Analog input | |

Product Folder Link(s): *ADS1174 ADS1178*

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## ADS1174/ADS1178 PIN DESCRIPTIONS (continued)

| PIN | | | |
|---|---|---|---|
| **NAME** | **NO.** | **FUNCTION** | **DESCRIPTION** |
| AINN1 | 4 | Analog input | |
| AINN2 | 2 | Analog input | |
| AINN3 | 64 | Analog input | **ADS1178:** AINN[8:1] Negative analog input, channels 8 through 1. |
| AINN4 | 62 | Analog input | |
| AINN5 | 52 | Analog input | **ADS1174:** AINN[8:5] Connected to internal ESD rails. The inputs may float. |
| AINN6 | 50 | Analog input | AINN[4:1] Negative analog input, channels 4 through 1. |
| AINN7 | 48 | Analog input | |
| AINN8 | 46 | Analog input | |
| AVDD | 5, 44, 53, 60 | Analog power supply | Analog power supply (4.75V to 5.25V). |
| VCOM | 55 | Analog output | AVDD/2 Unbuffered analog output. |
| VREFN | 57 | Analog input | Negative reference input. |
| VREFP | 56 | Analog input | Positive reference input. |
| CLK | 27 | Digital input | Master clock input (maximum 27MHz). |
| CLKDIV | 10 | Digital input | CLK input divider control: 1 = 27MHz<br>0 = 13.5MHz (high-speed) / 5.4MHz (low-power) |
| DGND | 7, 21, 24, 25 | Digital ground | Digital ground power supply. |
| DIN | 12 | Digital input | Daisy-chain data input. |
| DOUT1 | 20 | Digital output | DOUT1 is TDM data output (TDM mode). |
| DOUT2 | 19 | Digital output | |
| DOUT3 | 18 | Digital output | **ADS1178:** DOUT[8:1] Data output for channels 8 through 1. |
| DOUT4 | 17 | Digital output | |
| DOUT5 | 16 | Digital output | **ADS1174:** DOUT[8:5] Internally connected to active circuitry; outputs are driven. |
| DOUT6 | 15 | Digital output | DOUT[4:1] Data output for channels 4 through 1. |
| DOUT7 | 14 | Digital output | |
| DOUT8 | 13 | Digital output | |
| $\overline{\text{DRDY}}$/ FSYNC | 29 | Digital input/output | Frame-Sync protocol: frame clock input; SPI protocol: data ready output. |
| DVDD | 26 | Digital power supply | Digital core power supply (+1.65V to +1.95V). |
| FORMAT0 | 32 | Digital input | FORMAT[2:0] Selects between Frame-Sync/SPI protocol, TDM/discrete data outputs, fixed/dynamic position TDM data, and modulator mode/normal operating mode. |
| FORMAT1 | 31 | Digital input | |
| FORMAT2 | 30 | Digital input | |
| IOVDD | 22, 23 | Digital power supply | I/O power supply (+1.65V to +3.6V). |
| MODE | 34 | Digital input | MODE: 0 = High-Speed mode<br>1 = Low-Power mode. |
| NC | 33 | — | Internally connected to IOVDD (connect to IOVDD or leave open). |
| $\overline{\text{PWDN1}}$ | 42 | Digital input | |
| $\overline{\text{PWDN2}}$ | 41 | Digital input | |
| $\overline{\text{PWDN3}}$ | 40 | Digital input | **ADS1178:** $\overline{\text{PWDN}}$[8:1] Power-down control for channels 8 through 1. |
| $\overline{\text{PWDN4}}$ | 39 | Digital input | |
| $\overline{\text{PWDN5}}$ | 38 | Digital input | **ADS1174:** $\overline{\text{PWDN}}$[8:5] must = 0V. |
| $\overline{\text{PWDN6}}$ | 37 | Digital input | $\overline{\text{PWDN}}$[4:1] Power-down control for channels 4 through 1. |
| $\overline{\text{PWDN7}}$ | 36 | Digital input | |
| $\overline{\text{PWDN8}}$ | 35 | Digital input | |
| SCLK | 28 | Digital input | Serial clock input. |
| $\overline{\text{SYNC}}$ | 11 | Digital input | Synchronize input (all channels). |
| TEST0 | 8 | Digital input | TEST[1:0] Test mode select: 00 = normal operation |
| TEST1 | 9 | Digital input | 11 = test mode |

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## TIMING CHARACTERISTICS: SPI FORMAT



## TIMING REQUIREMENTS: SPI FORMAT

For $T_A$ = −40°C to +105°C, IOVDD = 1.65V to 3.6V, and DVDD = 1.65V to 1.95V.

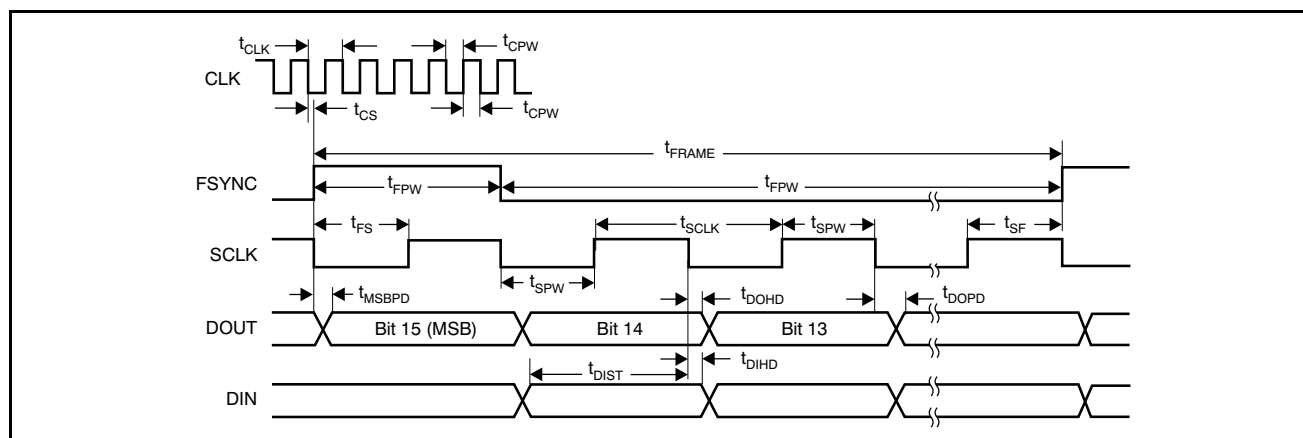| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{CLK}$ | CLK period (1/$f_{CLK}$)[1] | 37 | | 10,000 | ns |
| $t_{CPW}$ | CLK positive or negative pulse width | 15 | | | ns |
| $t_{CONV}$ | Conversion period (1/$f_{DATA}$)[2] | 256 | | 2560 | $t_{CLK}$ |
| $t_{CD}$[3] | Falling edge of CLK to falling edge of $\overline{DRDY}$ | | 22 | | ns |
| $t_{DS}$[3] | Falling edge of $\overline{DRDY}$ to rising edge of first SCLK to retrieve data | 1 | | | $t_{CLK}$ |
| $t_{MSBPD}$ | $\overline{DRDY}$ falling edge to DOUT MSB valid (propagation delay) | | | 16 | ns |
| $t_{SD}$[3] | Falling edge of SCLK to rising edge of $\overline{DRDY}$ | | 18 | | ns |
| $t_{SCLK}$[4] | SCLK period | 1 | | | $t_{CLK}$ |
| $t_{SPW}$ | SCLK positive or negative pulse width | 0.4 | | | $t_{CLK}$ |
| $t_{DOHD}$[3][5] | SCLK falling edge to new DOUT invalid (hold time) | 10 | | | ns |
| $t_{DOPD}$[3] | SCLK falling edge to new DOUT valid (propagation delay) | | | 32 | ns |
| $t_{DIST}$ | New DIN valid to falling edge of SCLK (setup time) | 6 | | | ns |
| $t_{DIHD}$[5] | Old DIN valid to falling edge of SCLK (hold time) | 6 | | | ns |

(1)  $f_{CLK}$ = 27MHz maximum.
(2)  Depends on MODE[1:0] and CLKDIV selection. See Table 4 ($f_{CLK}/f_{DATA}$).
(3)  Load on $\overline{DRDY}$ and DOUT = 20pF.
(4)  For best performance, limit $f_{SCLK}/f_{CLK}$ to ratios of 1, 1/2, 1/4, 1/8, etc.
(5)  $t_{DOHD}$ (DOUT hold time) and $t_{DIHD}$ (DIN hold time) are specified under opposite worst-case conditions (digital supply voltage and ambient temperature). Under equal conditions, with DOUT connected directly to DIN, the timing margin is >4ns.

Product Folder Link(s): *ADS1174 ADS1178*

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## TIMING CHARACTERISTICS: FRAME-SYNC FORMAT



## TIMING REQUIREMENTS: FRAME-SYNC FORMAT

For $T_A$ = −40°C to +105°C, IOVDD = 1.65V to 3.6V, and DVDD = 1.65V to 1.95V.

| SYMBOL | PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{CLK}$ | CLK period (1/$f_{CLK}$) | | 37 | | 10,000 | ns |
| $t_{CPW}$ | CLK positive or negative pulse width | | 12 | | | ns |
| $t_{CS}$ | Falling edge of CLK to falling edge of SCLK | | −0.25 | | 0.25 | $t_{CLK}$ |
| $t_{FRAME}$ | Frame period (1/$f_{DATA}$)[1] | | 256 | | 2560 | $t_{CLK}$ |
| $t_{FPW}$ | FSYNC positive or negative pulse width | | 1 | | | $t_{SCLK}$ |
| $t_{FS}$ | Rising edge of FSYNC to rising edge of SCLK | | 5 | | | ns |
| $t_{SF}$ | Rising edge of SCLK to rising edge of FSYNC | | 5 | | | ns |
| $t_{SCLK}$ | SCLK period[2] | | 1 | | | $t_{CLK}$ |
| $t_{SPW}$ | SCLK positive or negative pulse width | | 0.4 | | | $t_{CLK}$ |
| $t_{DOHD}$[3][4] | SCLK falling edge to old DOUT invalid (hold time) | | 10 | | | ns |
| $t_{DOPD}$[4] | SCLK falling edge to new DOUT valid (propagation delay) | | | | 31 | ns |
| $t_{MSBPD}$ | FSYNC rising edge to DOUT MSB valid (propagation delay) | | | | 31 | ns |
| $t_{DIST}$ | New DIN valid to falling edge of SCLK (setup time) | | 6 | | | ns |
| $t_{DIHD}$[3] | Old DIN valid to falling edge of SCLK (hold time) | | 6 | | | ns |

(1) Depends on MODE[1:0] and CLKDIV selection. See Table 4 ($f_{CLK}/f_{DATA}$).
(2) SCLK must be continuously running and limited to ratios of 1, 1/2, 1/4, and 1/8 of $f_{CLK}$.
(3) $t_{DOHD}$ (DOUT hold time) and $t_{DIHD}$ (DIN hold time) are specified under opposite worst-case conditions (digital supply voltage and ambient temperature). Under equal conditions, with DOUT connected directly to DIN, the timing margin is >4ns.
(4) Load on DOUT = 20pF.

Product Folder Link(s): *ADS1174 ADS1178*

# OVERVIEW

The ADS1174 (quad) and ADS1178 (octal) are 16-bit, delta-sigma ADCs. They offer the combination of excellent linearity, low noise, and low power consumption. Figure 1 shows the block diagram. Note that both devices are the same, except the ADS1174 has four ADCs, and the ADS1178 has eight ADCs. The pinout and package of the ADS1178 are compatible with the ADS1174 (and the 24-bit ADS1274 and ADS1278), permitting drop-in expandability or upgrades. The converters are comprised of either four (ADS1174) or eight (ADS1178) advanced, 6th-order, chopper-stabilized, delta-sigma modulators followed by low-ripple, linear phase FIR filters. The modulators measure the differential input signal, $V_{IN}$ = (AINP – AINN), against the differential reference, $V_{REF}$ = (VREFP – VREFN). The digital filters receive the modulator signal and provide a low-noise digital output.

To allow tradeoffs between speed and power, two modes of operation are supported: High-Speed and Low-Power. Table 1 summarizes the performance of each mode.

In High-Speed mode, the data rate is 52kSPS, and in Low-Power mode, the power dissipation is only 7mW/channel at 10.5kSPS.

The ADS1174/78 is configured by simply setting the appropriate I/O pins—there are no registers to program. Data are retrieved over a serial interface that supports both SPI and Frame-Sync formats. The ADS1174/78 has a daisy-chainable output and the ability to synchronize externally, so it can be used conveniently in systems requiring more than eight channels.
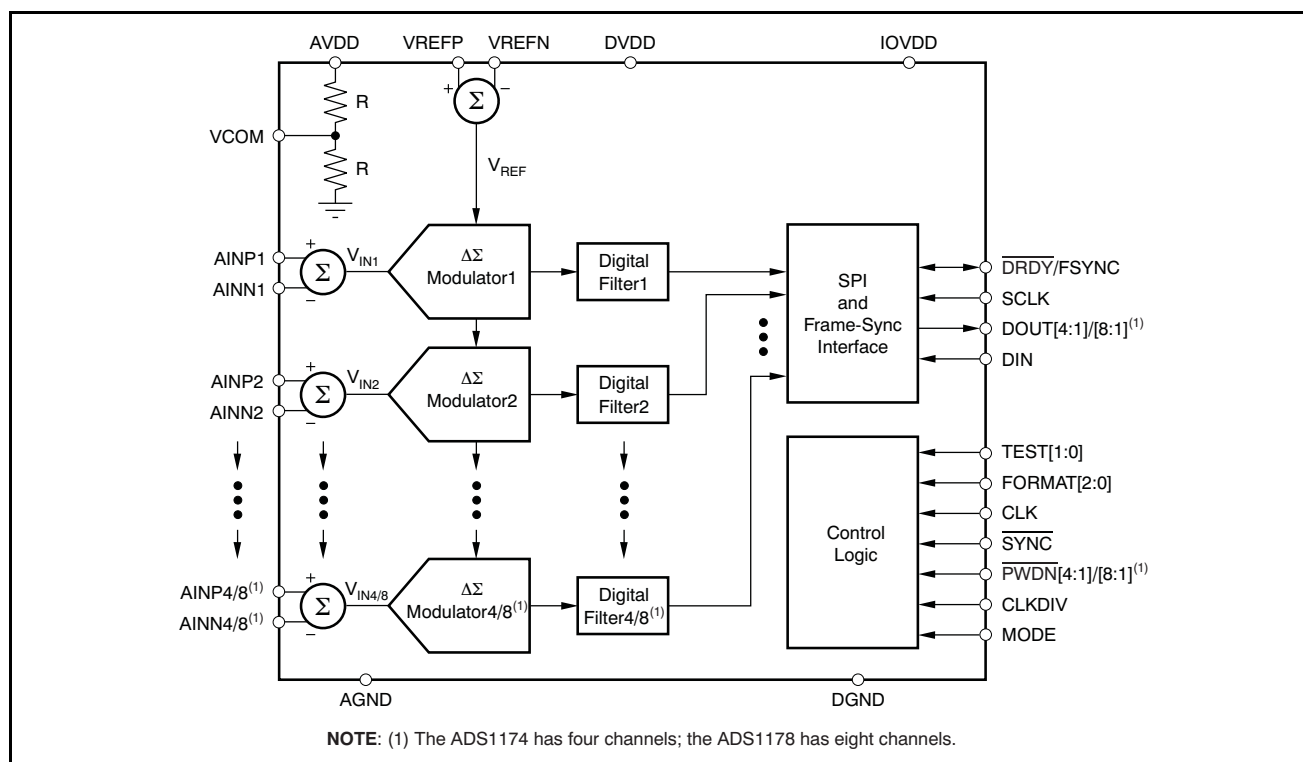


**NOTE**: (1) The ADS1174 has four channels; the ADS1178 has eight channels.

**Figure 1. ADS1174/ADS1178 Block Diagram**

**Table 1. Operating Mode Performance Summary**

| MODE | DATA RATE (SPS) | PASSBAND (Hz) | SNR (dB) | NOISE (LSB$_{PP}$) | POWER DISSIPATION PER CHANNEL[1] (mW) |
|---|---|---|---|---|---|
| High-Speed | 52,734 | 23,889 | 97 | 1 | 31 |
| Low-Power | 10,547 | 4,778 | 97 | 1 | 7 |

(1)   Measured with all channels operating.

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## FUNCTIONAL DESCRIPTION

The ADS1174 and ADS1178 are 16-bit delta/sigma ADCs consisting of independent converters that digitize input signals simultaneously. The ADS1174 consists of four independent converters, while the ADS1178 has eight independent converters.

The converter is composed of two main functional blocks to perform the ADC conversions: the modulator and the digital filter. The modulator samples the input signal together with sampling the reference voltage to produce a 1's density output stream. The density of the output stream is proportional to the analog input level relative to the reference voltage. The pulse stream is filtered by the internal digital filter where the output conversion result is produced.

In operation, the signal inputs and reference inputs are sampled by the modulator at a high rate (typically 64x higher than the final output data rate). The quantization noise of the modulator is moved to a higher frequency range where the internal digital filter removes it. This process results in very low levels of noise within the signal passband.

Because the input signal is sampled at a very high rate, input signal aliasing does not occur until the input signal frequency approaches the modulator sampling rate. The high sampling rate of the modulator greatly relaxes the requirement of external antialiasing filters, thus eliminating passband phase errors that otherwise may be caused by the analog filter.

## SAMPLING APERTURE MATCHING

The converters of the ADS1174/78 operate from the same CLK input. The CLK input controls the timing of the modulator sampling instant. The converter is designed so that the sampling skew (or modulator sampling aperture match) between channels is controlled. Furthermore, the digital filters are synchronized to start the convolution phase at the same modulator clock cycle. This design results in excellent phase match among the ADS1174/78 channels.

The phase match of one four-channel ADS1174 to that of another ADS1174 may not have the same degree of sampling match (the same is true for two 8-channel ADS1178s). As a result of manufacturing variations, differences in internal propagation delay of the internal CLK signal coupled with differences of the arrival of the external CLK signal to each device may cause larger sampling match errors. Equal length CLK traces or external clock distribution devices can be used to control the arrival of the CLK signals to help reduce the sampling match error.

## FREQUENCY RESPONSE

The digital filter sets the overall frequency response. The filter uses a multi-stage FIR topology to provide linear phase with minimal passband ripple and high stop band attenuation. The oversampling ratio of the digital filter (that is, the ratio of the modulator sampling to the output data rate: $f_{MOD}/f_{DATA}$) is 64 for both High-Speed and Low-Power modes.

Figure 2 shows the frequency response of the ADS1174/78 normalized to $f_{DATA}$. Figure 3 shows the passband ripple. The transition from passband to stop band is illustrated in Figure 4. The overall frequency response repeats at 64x multiples of the modulator frequency $f_{MOD}$, as shown in Figure 5.
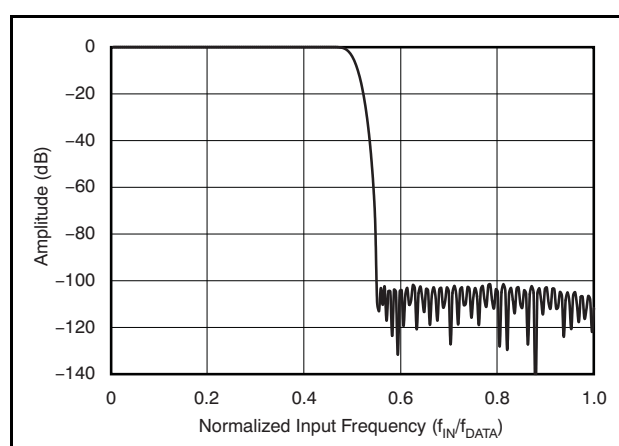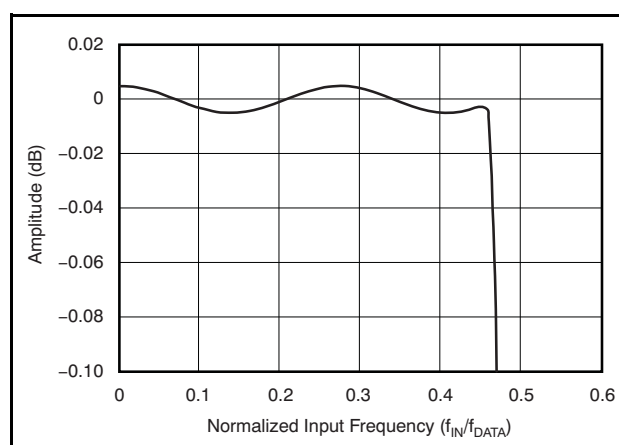


**Figure 2. Frequency Response**



**Figure 3. Passband Response**

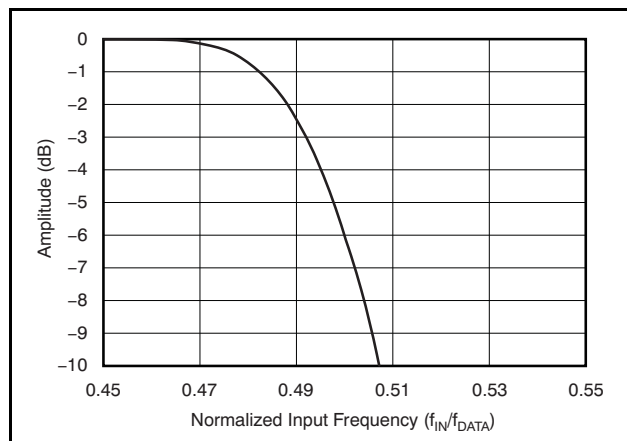Product Folder Link(s): *ADS1174 ADS1178*

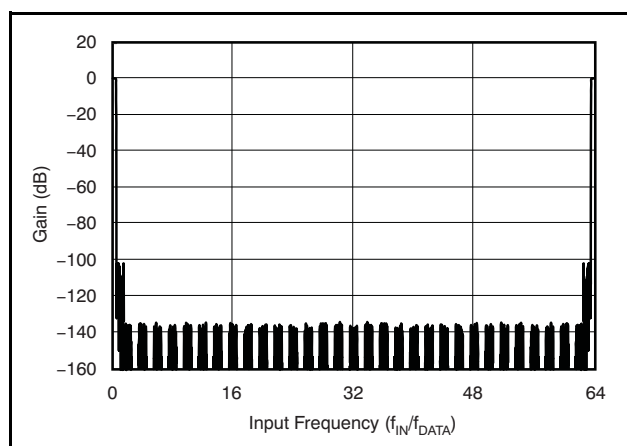**Figure 4. Transition Band Response**



**Figure 5. Frequency Response Out to f$_{MOD}$**

These image frequencies, if present in the signal and not externally filtered, fold back (or alias) into the passband, causing errors. Table 2 lists the degree of image rejection versus external antialiasing filter order. The stop band of the ADS1174/78 provides 100dB attenuation of frequencies that begin just beyond the passband and continue out to f$_{MOD}$. Placing an antialiasing, low-pass filter in front of the ADS1174/78 inputs is recommended to limit possible high-amplitude, out-of-band signals and noise.

**Table 2. Antialiasing Filter Order Image Rejection**

| ANTIALIASING FILTER ORDER | IMAGE REJECTION (dB) (f$_{-3dB}$ at f$_{DATA}$) |
|---|---|
| 1 | 39 |
| 2 | 75 |
| 3 | 111 |

## PHASE RESPONSE

The ADS1174/78 incorporates a multiple stage, linear phase digital filter. Linear phase filters exhibit constant delay time versus input frequency (constant group delay), which means the time delay from any instant of the input signal to the same instant of the output data is constant, and is independent of input signal frequency. This behavior results in essentially zero phase errors when analyzing multi-tone signals.

## SETTLING TIME

As with frequency and phase response, the digital filter also determines settling time. Figure 6 shows the output settling behavior after a step change on the analog inputs normalized to conversion periods. The X-axis is given in units of conversion. Note that after the step change on the input occurs, the output data change very little prior to 30 conversion periods. The output data are fully settled after 76 conversion periods.
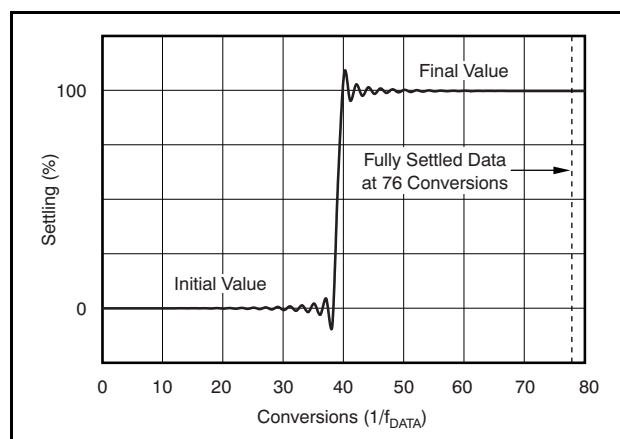


**Figure 6. Step Response**

## ANALOG INPUTS (AINP, AINN)

The ADS1174/78 measures each differential input signal $V_{IN}$ = (AINP − AINN) against the common differential reference $V_{REF}$ = (VREFP − VREFN). The most positive measurable differential input is +$V_{REF}$, which produces the most positive digital output code of 7FFFh. Likewise, the most negative measurable differential input is −$V_{REF}$, which produces the most negative digital output code of 8000h.

For optimal performance, drive the ADS1174/78 inputs differentially. For single-ended input applications, one of the inputs (AINP or AINN) can be driven while the other input is fixed (typically, to AGND or +2.5V); fixing the input to +2.5V permits bipolar operation, thereby using the full range of the converter.

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While the ADS1174/78 measures the differential input signal, the absolute input voltage is also important. This is the voltage on either input (AINP or AINN) with respect to AGND. The range for this voltage is:

−0.1V < (AINN or AINP) < AVDD + 0.1V

If either input is taken below −0.4V or above (AVDD + 0.4), ESD protection diodes on the inputs may turn on.

If these conditions are possible, external Schottky clamp diodes or series resistors may be required to limit the input current to safe levels (see Absolute Maximum Ratings table).

The ADS1174/78 is a high-performance ADC. For optimum performance, it is critical that the appropriate circuitry be used to drive the ADS1174/78 inputs. See the Applications Information section for the recommended circuits.

The ADS1174/78 uses switched-capacitor circuitry to measure the input voltage. Internal capacitors are charged by the inputs and then discharged. Figure 7 shows a conceptual diagram of these circuits. Switch $S_2$ represents the net effect of the modulator circuitry in discharging the sampling capacitor; the actual implementation is different. The timing for switches $S_1$ and $S_2$ is shown in Figure 8. The sampling time ($t_{SAMPLE}$) is the inverse of modulator sampling frequency ($f_{MOD}$) and is a function of the mode, the CLKDIV input, and frequency of CLK, as shown in Table 3.

The average load presented by the switched capacitor input can be modeled with an effective differential impedance, as shown in Figure 9. Note that the effective impedance is a function of $f_{MOD}$.
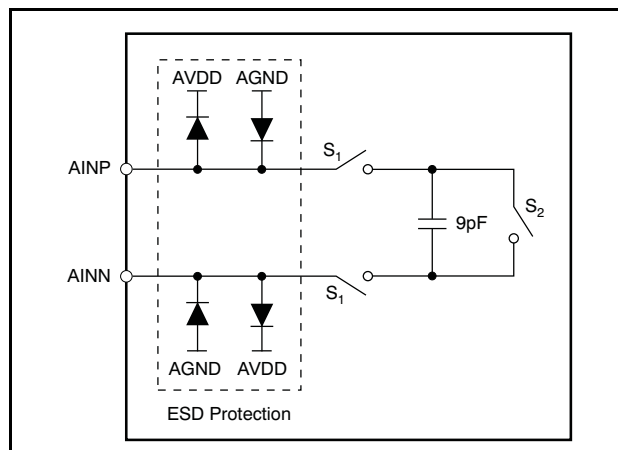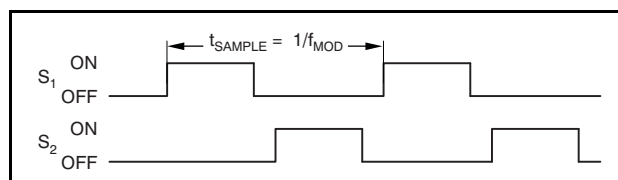


**Figure 7. Equivalent Analog Input Circuitry**



**Figure 8. $S_1$ and $S_2$ Switch Timing for Figure 7**

**Table 3. Modulator Frequency ($f_{MOD}$) versus Mode Selection**

| MODE SELECTION | CLKDIV | $f_{MOD}$ |
|---|---|---|
| High-Speed | 1 | $f_{CLK}/8$ |
| | 0 | $f_{CLK}/4$ |
| Low-Power | 1 | $f_{CLK}/40$ |
| | 0 | $f_{CLK}/8$ |



**Figure 9. Effective Input Impedances**

Product Folder Link(s): ADS1174 ADS1178

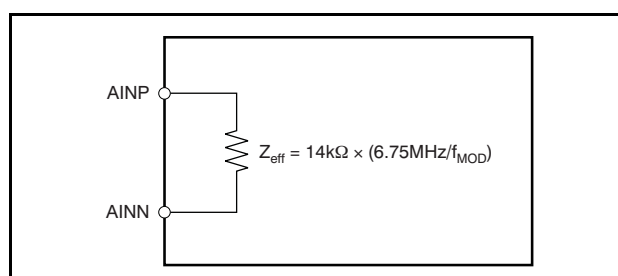## VOLTAGE REFERENCE INPUTS (VREFP, VREFN)

The voltage reference for the ADS1174/78 ADC is the differential voltage between VREFP and VREFN: $V_{REF}$ = (VREFP − VREFN). The voltage reference is common to all channels. The reference inputs use a structure similar to that of the analog inputs with the equivalent circuitry on the reference inputs shown in Figure 10. As with the analog inputs, the load presented by the switched capacitor can be modeled with an effective impedance, as shown in Figure 11. However, the reference input impedance depends on the number of active (enabled) channels in addition to $f_{MOD}$. As a result of the change of reference input impedance caused by enabling and disabling channels, the regulation and settling time of the external reference should be noted, so as not to affect the readings of other channels.
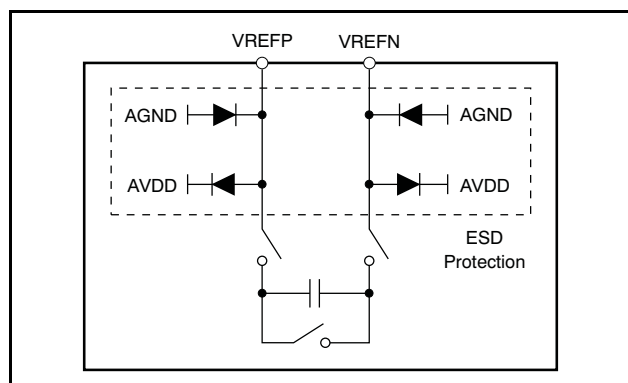


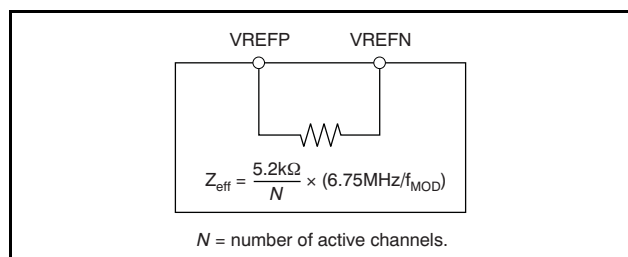**Figure 10. Equivalent Reference Input Circuitry**



$$Z_{eff} = \frac{5.2k\Omega}{N} \times (6.75MHz/f_{MOD})$$

$N$ = number of active channels.

**Figure 11. Effective Reference Impedance**

ESD diodes protect the reference inputs. To keep these diodes from turning on, make sure the voltages on the reference pins do not go below AGND by more than 0.4V, and likewise do not exceed AVDD by 0.4V.

If these conditions are possible, external Schottky clamp diodes or series resistors may be required to limit the input current to safe levels (see Absolute Maximum Ratings table).

Note that the valid operating range of the reference inputs is limited to the following:

−0.1V ≤ VREFN ≤ 0.1V

VREFN + 0.5V ≤ VREFP ≤ VREFN + 3.1V

A high-quality reference voltage with the appropriate drive strength is essential for achieving the best performance from the ADS1174/78. Noise and drift on the reference degrade overall system performance. See the *Application Information* section for example reference circuits.

## CLOCK INPUT (CLK)

The ADS1174/78 requires a clock input for operation. Each ADS1174/78 converter operates from the same clock input. At the maximum data rate, the clock input can be either 27MHz or 13.5MHz (5.4MHz, low-power mode), determined by the setting of the CLKDIV input. The selection of the external clock frequency ($f_{CLK}$) does not affect the resolution (the oversampling ratio, OSR, remains fixed) or power dissipation of the ADS1174/78. However, a slower $f_{CLK}$ can reduce the power consumption of an external clock driver. The output data rate scales with clock frequency, down to a minimum clock frequency of $f_{CLK}$ = 100kHz. Table 4 summarizes the ratio of clock input frequency ($f_{CLK}$) to data rate ($f_{DATA}$), maximum data rate and corresponding maximum clock input for the two operating modes.

**Table 4. Clock Input Options**

| MODE SELECTION | $f_{CLK}$ (MHz) | CLKDIV | $f_{CLK}/f_{DATA}$ | DATA RATE (SPS) |
|---|---|---|---|---|
| High-Speed | 27 | 1 | 512 | 52,734 |
| | 13.5 | 0 | 256 | |
| Low-Power | 27 | 1 | 2,560 | 10,547 |
| | 5.4 | 0 | 512 | |

As with any high-speed data converter, a high-quality, low-jitter clock is essential for optimum performance. Crystal clock oscillators are the recommended clock source. Make sure to avoid excess ringing on the clock input; keeping the clock trace as short as possible using a 50Ω series resistor, placed close to the source end, often helps.

## MODE SELECTION (MODE)

The ADS1174/78 supports two modes of operation: High-Speed and Low-Power. These modes offer optimization of speed and power. The mode selection is determined by the status of the digital input MODE pins, as shown in Table 5. The ADS1174/78 constantly monitors the status of the MODE pin during operation.

**Table 5. Mode Selection**

| MODE | MODE SELECTION | MAX $f_{DATA}$[(1)] |
|---|---|---|
| 0 | High-Speed | 52,734 |
| 1 | Low-Power | 10,547 |

(1) $f_{CLK}$ = 27MHz (CLKDIV = 1).

When using the SPI protocol, $\overline{DRDY}$ is held high after a mode change occurs until settled (or valid) data are ready, as shown in Figure 12 and Table 6.

In Frame-Sync protocol, the DOUT pins are held low after a mode change occurs until settled data are ready, as shown in Figure 12 and Table 6. Data can be read from the device to detect when DOUT changes to logic 1, indicating valid data.

## SYNCHRONIZATION ($\overline{SYNC}$)

The ADS1174/78 can be synchronized by pulsing the $\overline{SYNC}$ pin low and then returning the pin high. When the pin goes low, the conversion process stops, and the internal counters used by the digital filter are reset. When the $\overline{SYNC}$ pin returns high, the conversion process restarts. Synchronization allows the conversion to be aligned with an external event, such as a reference timing pulse.

Since the converters of the ADS1174/78 operate in parallel from the same master clock and use the same $\overline{SYNC}$ input control, they are, by default, in synchronization with each other. However, the synchronization of multiple ADS1174/78s is somewhat different. At device power-on, variations in internal reset thresholds from device to device may result in uncertainty in conversion timing.

The $\overline{SYNC}$ pin can be used to synchronize multiple ADS1174/78s to within the same CLK cycle. Figure 13 illustrates the timing requirement of $\overline{SYNC}$ and CLK in SPI format.

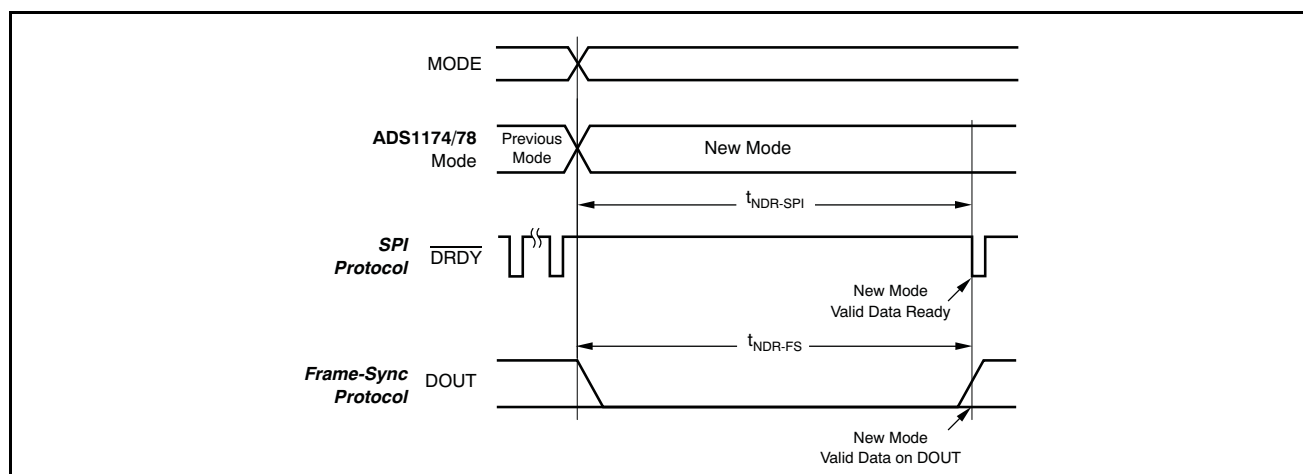See Figure 14 for the Frame-Sync format timing requirement.



**Figure 12. Mode Change Timing**

**Table 6. Mode Change**

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{NDR-SPI}$ | Time for new data to be ready (SPI) | | | 129 | Conversions (1/$f_{DATA}$) |
| $t_{NDR-FS}$ | Time for new data to be ready (Frame-Sync) | 127 | | 128 | Conversions (1/$f_{DATA}$) |

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After synchronization, indication of valid data depends on the whether SPI or Frame-Sync format is used.

In the SPI format, $\overline{DRDY}$ goes high as soon as $\overline{SYNC}$ is taken low; see Figure 13. After $\overline{SYNC}$ is returned high, $\overline{DRDY}$ stays high while the digital filter is settling. Once valid data are ready for retrieval, $\overline{DRDY}$ goes low.

In the Frame-Sync format, DOUT goes low as soon as $\overline{SYNC}$ is taken low; see Figure 14. After $\overline{SYNC}$ is returned high, DOUT stays low while the digital filter is settling. Once valid data are ready for retrieval, DOUT begins to output valid data. For proper synchronization, FSYNC, $\overline{SCLK}$, and CLK must be established before taking $\overline{SYNC}$ high, and must then remain running.
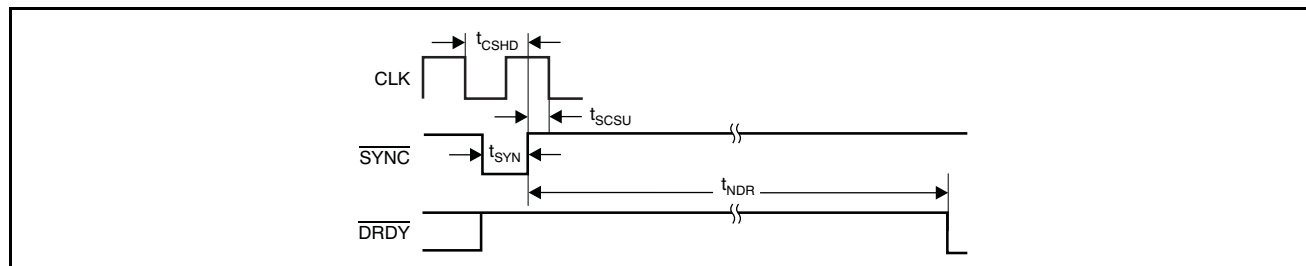


**Figure 13. Synchronization Timing for SPI Protocol**

**Table 7. SPI Protocol**

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CSHD}$ | CLK to $\overline{SYNC}$ hold time (to not latch on CLK edge) | 10 | | | ns |
| $t_{SCSU}$ | $\overline{SYNC}$ to CLK setup time (to latch on CLK edge) | 5 | | | ns |
| $t_{SYN}$ | Synchronize pulse width | 1 | | | CLK periods |
| $t_{NDR}$ | Time for new data to be ready | | | 129 | Conversions (1/$f_{DATA}$) |



**Figure 14. Synchronization Timing for Frame-Sync Protocol**

**Table 8. Frame-Sync Protocol**

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CSHD}$ | CLK to $\overline{SYNC}$ hold time (to not latch on CLK edge) | 10 | | | ns |
| $t_{SCSU}$ | $\overline{SYNC}$ to CLK setup time (to latch on CLK edge) | 5 | | | ns |
| $t_{SYN}$ | Synchronize pulse width | 1 | | | CLK periods |
| $t_{NDR}$ | Time for new data to be ready | 127 | | 128 | Conversions (1/$f_{DATA}$) |

## POWER-DOWN ($\overline{\text{PWDN}}$)

The ADS1174/78 measurement channels can be independently powered down by use of the $\overline{\text{PWDN}}$ inputs. To enter the power-down mode, hold the respective $\overline{\text{PWDN}}$ pin low for at least two $f_{CLK}$ cycles. To exit power-down, return the corresponding PWDN pin high. Note that when all channels are powered down, the ADS1174/78 enters a microwatt (μW) power state where all internal biasing is powered down. In this event, the TEST[1:0] input pins must be driven; all other input pins can float (the ADS1174/78 outputs remain driven).

As shown in Figure 15 and Table 9, a maximum of 130 conversion cycles (SPI interface) or 129 conversion cycles (Frame-Sync interface) must elapse before reading data after exiting power-down. Data from channels already running are not affected. The user software can perform the required delay time in the following ways:

1. Count the number of data conversions after taking the $\overline{\text{PWDN}}$ pin high.

2. Wait for 130/$f_{DATA}$ (SPI) or 129/$f_{DATA}$ (Frame-Sync) after taking the $\overline{\text{PWDN}}$ pins high.

3. Detect for non-zero data in the powered-up channel.

After powering up one or more channels, the channels are synchronized to each other. It is not necessary to use the $\overline{\text{SYNC}}$ pin to synchronize them.

When a channel is powered down in TDM data format, the data for the powered-down channel are either forced to zero (fixed-position TDM data mode) or replaced by shifting the data from the next channel into the vacated data position (dynamic-position TDM data mode).

In discrete data format, the data are always forced to zero. When powering-up a channel in dynamic-position TDM data format mode, the channel data remain packed until the data are ready, at which time the data frame is expanded to include the just-powered channel data. See the Data Format section for details.
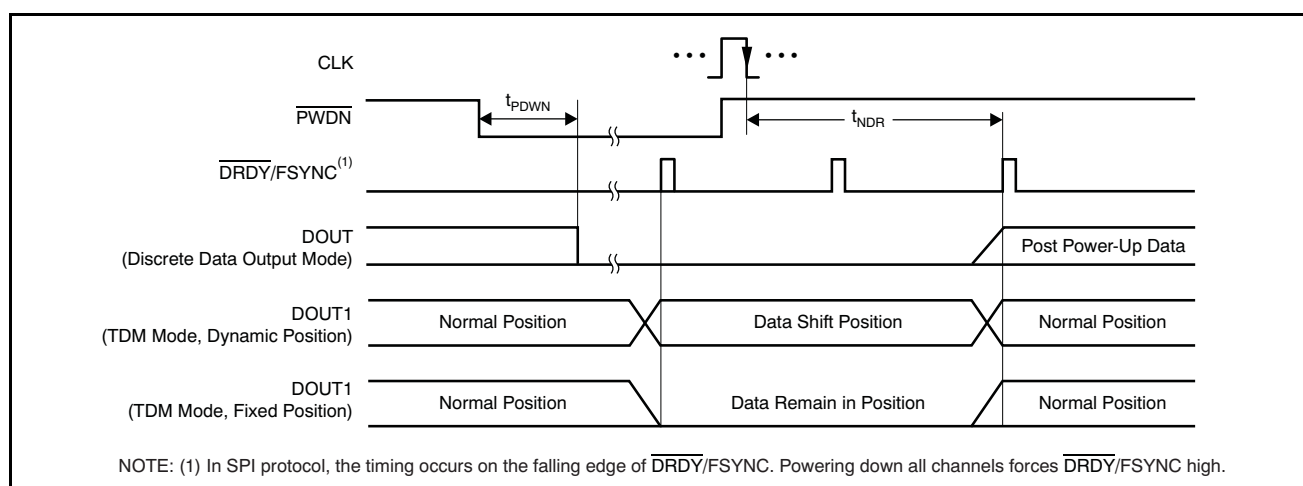


Figure 15. Power-Down Timing

Table 9. Power-Down Timing

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{PDWN}$ | $\overline{\text{PDWN}}$ pulse width to enter Power-Down mode | 2 | | | CLK periods |
| $t_{NDR}$ | Time for new data to be ready (SPI) | 129 | | 130 | Conversions (1/$f_{DATA}$) |
| | Time for new data to be ready (Frame-Sync) | 128 | | 129 | Conversions (1/$f_{DATA}$) |

Product Folder Link(s): ADS1174 ADS1178

**ADS1174**
**ADS1178**

## FORMAT[2:0]

Data can be read from the ADS1174/78 with two serial interface protocols (SPI or Frame-Sync) and several options of data formats (TDM/Discrete and Fixed/Dynamic data positions). The FORMAT[2:0] inputs are used to select among the options. Table 10 lists the available options. See the DOUT Modes section for details of the DOUT modes and data positions.

**Table 10. Data Output Format**

| FORMAT[2:0] | INTERFACE PROTOCOL | DOUT MODE | DATA POSITION |
|---|---|---|---|
| 000 | SPI | TDM | Dynamic |
| 001 | SPI | TDM | Fixed |
| 010 | SPI | Discrete | — |
| 011 | Frame-Sync | TDM | Dynamic |
| 100 | Frame-Sync | TDM | Fixed |
| 101 | Frame-Sync | Discrete | — |

## DATA FORMAT

The ADS1174/78 outputs 16 bits of data in two's complement format.

A positive full-scale input produces an ideal output code of 7FFFh, and the negative full-scale input produces an ideal output code of 8000h. The output clips at these codes for signals exceeding full-scale. Table 11 summarizes the ideal output codes for different input signals.

**Table 11. Ideal Output Code versus Input Signal**

| INPUT SIGNAL $V_{IN}$ (AINP − AINN) | IDEAL OUTPUT CODE[1] |
|---|---|
| $\geq +V_{REF}$ | 7FFFh |
| $\dfrac{+ V_{REF}}{2^{15} - 1}$ | 0001h |
| 0 | 0000h |
| $\dfrac{- V_{REF}}{2^{15} - 1}$ | FFFFh |
| $\leq -V_{REF}\left(\dfrac{2^{15}}{2^{15} - 1}\right)$ | 8000h |

(1) Excludes effects of noise, INL, offset, and gain errors.

## SERIAL INTERFACE PROTOCOLS

Data are retrieved from the ADS1174/78 using the serial interface. Two protocols are available: SPI and Frame-Sync. The same pins are used for both interfaces: SCLK, DRDY/FSYNC, DOUT[4:1] (or DOUT[8:1] for the ADS1178), and DIN. The FORMAT[2:0] pins select the desired interface protocol.

## SPI SERIAL INTERFACE

The SPI-compatible format is a simple read-only interface. Data ready for retrieval are indicated by the falling DRDY output and are shifted out on the falling edge of SCLK, MSB first. The interface can be daisy-chained using the DIN input when using multiple ADS1174/78s. See the Daisy-Chaining section for more information.

## SCLK

The serial clock (SCLK) features a Schmitt-triggered input and shifts out data on DOUT on the falling edge. It also shifts in data on the falling edge on DIN when this pin is being used for daisy-chaining. The device shifts data out on the falling edge and the user typically shifts this data in on the rising edge. Even though the SCLK input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. SCLK may be run as fast as the CLK frequency. SCLK may be either in free-running or stop-clock operation between conversions. For best performance, use $f_{SCLK}/f_{CLK}$ ratios of 1, 1/2, 1/4, 1/8, etc. **NOTE:** One CLK period is required after DRDY falls, to start shifting data (see Timing Requirements: SPI Format ).

## DRDY/FSYNC (SPI Format)

In the SPI format, this pin functions as the DRDY output. It goes low when data are ready for retrieval and then returns high on the falling edge of the first subsequent SCLK. If data are not retrieved (that is, SCLK is held low), DRDY pulses high just before the next conversion data are ready, as shown in Figure 16. The new data are loaded within one CLK cycle before DRDY goes low. All data must be shifted out before this time to avoid being overwritten.



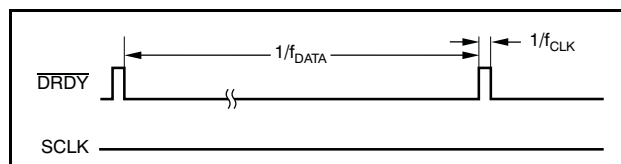**Figure 16. DRDY Timing with No Readback**

Product Folder Link(s): ADS1174 ADS1178

**ADS1174**
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TEXAS
INSTRUMENTS

### DOUT

In Discrete Data Output mode, the conversion data are output on the individual DOUT pins (DOUT1, DOUT2, etc.), whereas in TDM mode, data are output only on DOUT1. The MSB data are valid on DOUT[4:1]/[8:1] when DRDY goes low. The subsequent bits are shifted out with each falling edge of SCLK. If daisy-chaining (TDM mode), the data shifted in using DIN appear on DOUT1 after all channel data have been shifted out.

### DIN

This input is used when multiple ADS1174/78s are to be daisy-chained together. The DOUT1 pin of the first device connects to the DIN pin of the next, etc. It can be used with either the SPI or Frame-Sync formats. Data are shifted in on the falling edge of SCLK. When using only one ADS1174/78, tie DIN low. See the *Daisy-Chaining* section for more information.

### FRAME-SYNC SERIAL INTERFACE

Frame-Sync format is similar to the interface often used on audio ADCs. It operates in slave fashion—the user must supply framing signal FSYNC (similar to the *left/right clock* on stereo audio ADCs) and the serial clock SCLK (similar to the *bit clock* on audio ADCs). The data is output MSB first or *left-justified*. When using Frame-Sync format, the FSYNC and SCLK inputs must be continuously running with the required relationships shown in the *Frame-Sync Timing Requirements*.

### SCLK

The serial clock (SCLK) features a Schmitt-triggered input and shifts out data on DOUT on the falling edge. It also shifts in data on the falling edge on DIN when this pin is being used for daisy-chaining. Even though SCLK has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. When using Frame-Sync format, SCLK must run continuously; if SCLK is disabled or interrupted, the data readback

will be corrupted. The number of SCLKs within a frame period (FSYNC clock) can be any power of two ratio of clock cycles (1, 1/2, 1/4, etc.), as long as the number of cycles is sufficient to shift the data output from all channels within one data frame.

### DRDY/FSYNC (Frame-Sync Format)

In Frame-Sync format, this pin is used as the FSYNC input. The frame-sync input (FSYNC) sets the frame period which must be same as the data rate. The required number of $f_{CLK}$ cycles to each FSYNC period depends on the mode selection and the CLKDIN input. Table 4 indicates the number of CLK cycles to each frame ($f_{CLK}/f_{DATA}$). If the FSYNC period is not the proper value, data readback is corrupted.

### DOUT

In Discrete Data Output mode, the conversion data are shifted out on the individual DOUT pins (DOUT1, DOUT2, etc.), whereas in TDM mode, data are output only on DOUT1. The MSB data become valid on DOUT[4:1]/[8:1] on the SCLK rising edge prior to FSYNC going high. The subsequent bits are shifted out with each falling edge of SCLK. If daisy-chaining (TDM mode), the data shifted in using DIN appear on DOUT1 after all channel data have been shifted out (that is, 4 channels × 16 bits per channel = 64 bits for the ADS1174, and 8 channels × 16 bits per channel = 128 bits for the ADS1178).

### DIN

This input is used when multiple ADS1174/78s are to be daisy-chained together. It can be used with either SPI or Frame-Sync formats. Data are shifted in on the falling edge of SCLK. When using only one ADS1174/78, tie DIN low. See the *Daisy-Chaining* section for more information.

## DOUT MODES

For both SPI and Frame-Sync interface protocols, either the data are shifted out through individual channel DOUT pins in a parallel data format (Discrete mode), or the data for all channels are shifted out in series through common pin DOUT1 (TDM mode).

### TDM Mode

In time division multiplexed (TDM) data output mode, the data for all channels are shifted out, in series, on a single pin (DOUT1). As shown in Figure 17, the data from channel 1 are shifted out first, followed by channel 2 data, etc. After the data from the last channel are shifted out (channel 4 for the ADS1174 or channel 8 for the ADS1178), the data from the DIN input follow. DIN is used to daisy-chain the data

output from another ADS1174, ADS1178, or other compatible device. Note that when all channels of the ADS1174/78 are powered down, the interface is powered down, rendering the DIN input powered down as well. When one or more channels of the device are powered down, the data format of the TDM mode can be fixed or dynamic.

### TDM Mode, Fixed-Position Data

In this TDM data output mode, the data position of the channels remains fixed, regardless of whether channels are disabled. If a channel is powered down, data are forced to zero, but occupy the same position within the data stream. Figure 18 shows the data stream with channel 1 and channel 3 powered down.
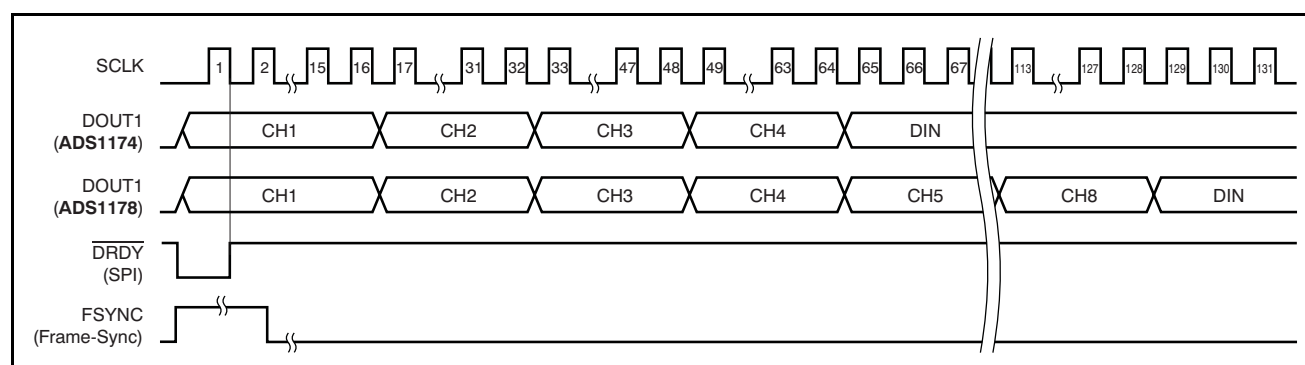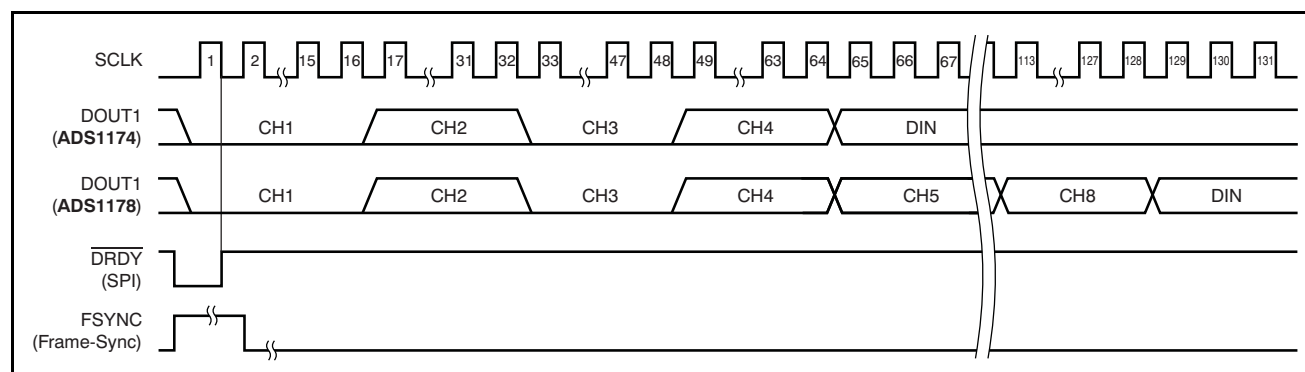


**Figure 17. TDM Mode (All Channels Enabled)**



**Figure 18. TDM Mode, Fixed-Position Data (Channels 1 and 3 Shown Powered Down)**

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**TDM Mode, Dynamic Position Data**

In this TDM data output mode, when a channel is powered down, the data from higher channels shift one position in the data stream to fill the vacated data slot. Figure 19 shows the data stream with channel 1 and channel 3 powered down.

**Discrete Data Output Mode**

In Discrete data output mode, the channel data are shifted out in parallel using individual channel data output pins DOUT[4:1] for the ADS1174, or DOUT[8:1] for the ADS1178. After the 16th SCLK, the channel data are forced to zero. The data are also forced to zero for powered-down channels. Figure 20 depicts the data format.
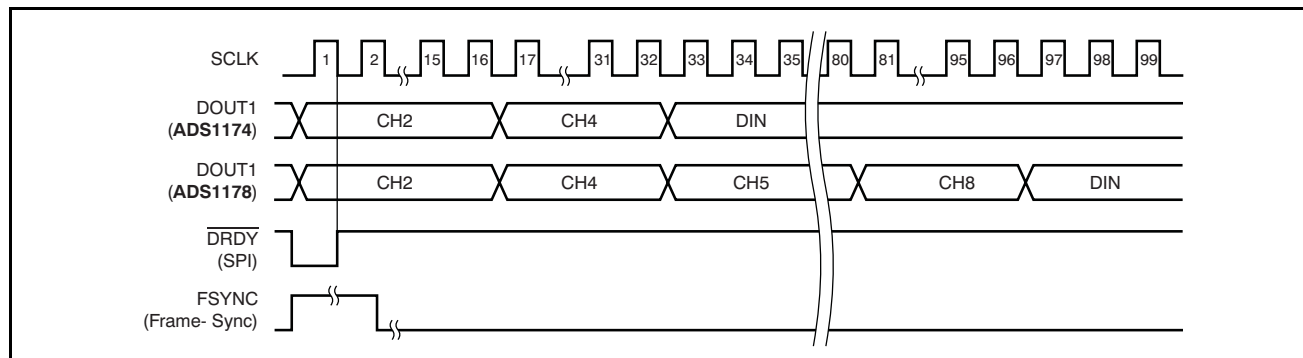


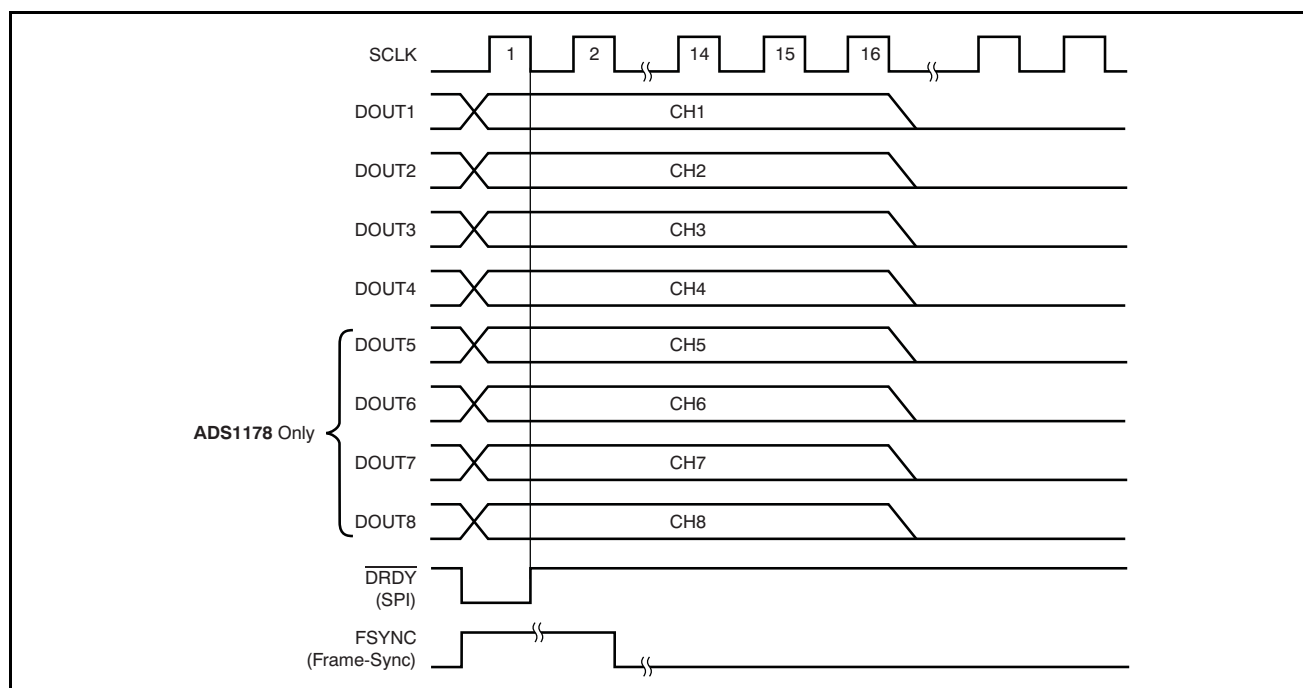**Figure 19. TDM Mode, Dynamic Position Data (Channels 1 and 3 Shown powered Down)**



**Figure 20. Discrete Data Output Mode**

## DAISY-CHAINING

Multiple ADS1174/78s can be daisy-chained together to simplify the serial interface connections. The DOUT1 data output pin of one ADS1174/78 is connected to the DIN input of the next ADS1174/78. As Figure 21 illustrates, the DOUT1 pin of device 1 provides the output data to a controller, and the DIN input of device 2 is grounded. Figure 22 describes the data format when reading data back in a daisy-chain configuration.

The maximum number of channels that may be daisy-chained in this way is limited by the frequency of $f_{SCLK}$, the mode selection, and the CLKDIV input. The frequency of $f_{SCLK}$ must be high enough to completely shift the data out from all channels within one $f_{DATA}$ period. Table 12 lists the maximum number of daisy-chained channels when $f_{SCLK} = f_{CLK}$.
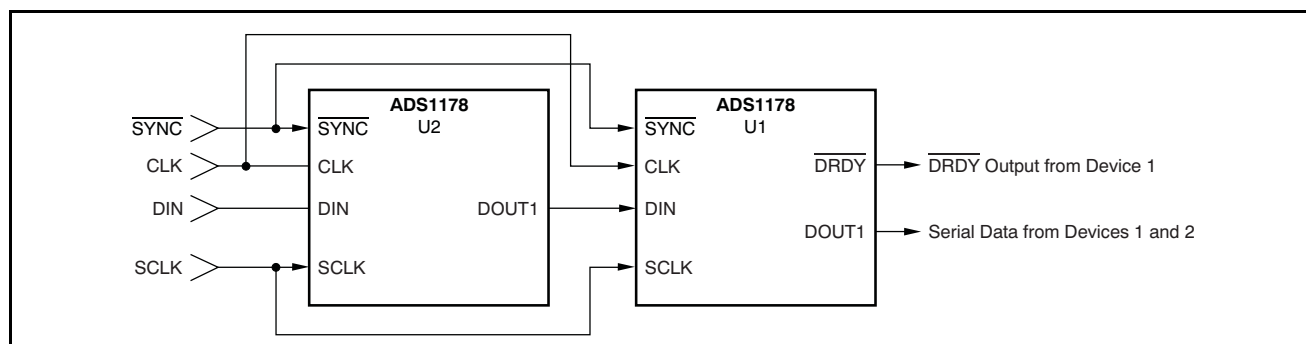


**Figure 21. Daisy-Chaining of Two ADS1178s, SPI Protocol (FORMAT[2:0] = 000 or 001)**
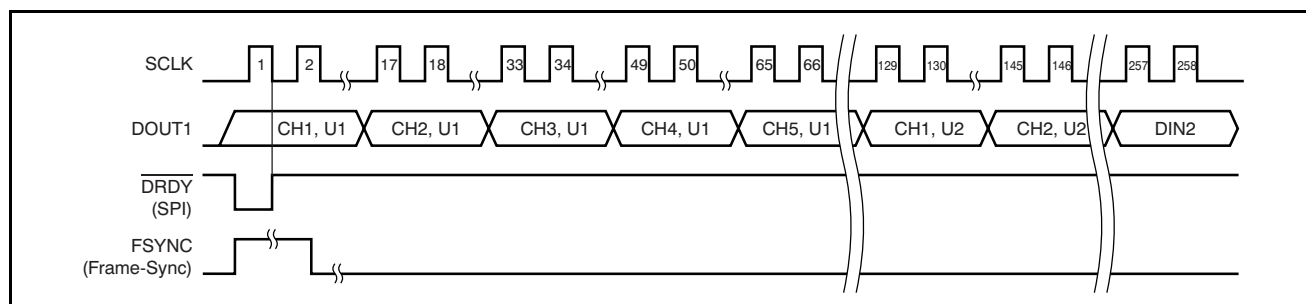


**Figure 22. Daisy-Chain Data Format of Figure 21**

**Table 12. Maximum Channels in a Daisy-Chain ($f_{SCLK} = f_{CLK}$)**

| MODE SELECTION | CLKDIV | MAXIMUM NUMBER OF CHANNELS |
|---|---|---|
| High-Speed | 1 | 32 |
| | 0 | 16 |
| Low-Power | 1 | 160 |
| | 0 | 32 |

To increase the number of data channels possible in a chain, a segmented DOUT scheme may be used, producing two data streams. Figure 23 illustrates four ADS1178s, with a pair of ADS1178s daisy-chained together. The channel data of each daisy-chained pair are shifted out in parallel and are received by the processor through independent data channels.

Whether the interface protocol is SPI or Frame-Sync, it is recommended to synchronize all devices by tying the $\overline{\text{SYNC}}$ inputs together. When synchronized in SPI protocol, it is only necessary to monitor the $\overline{\text{DRDY}}$ output of one ADS1178.

In Frame-Sync interface protocol, the data from all devices are ready on the rising edge of FSYNC.

Since DOUT1 and DIN are both shifted on the falling edge of SCLK, the propagation delay on DOUT1 creates a setup time for DIN. Minimize the skew in SCLK to avoid timing violations.
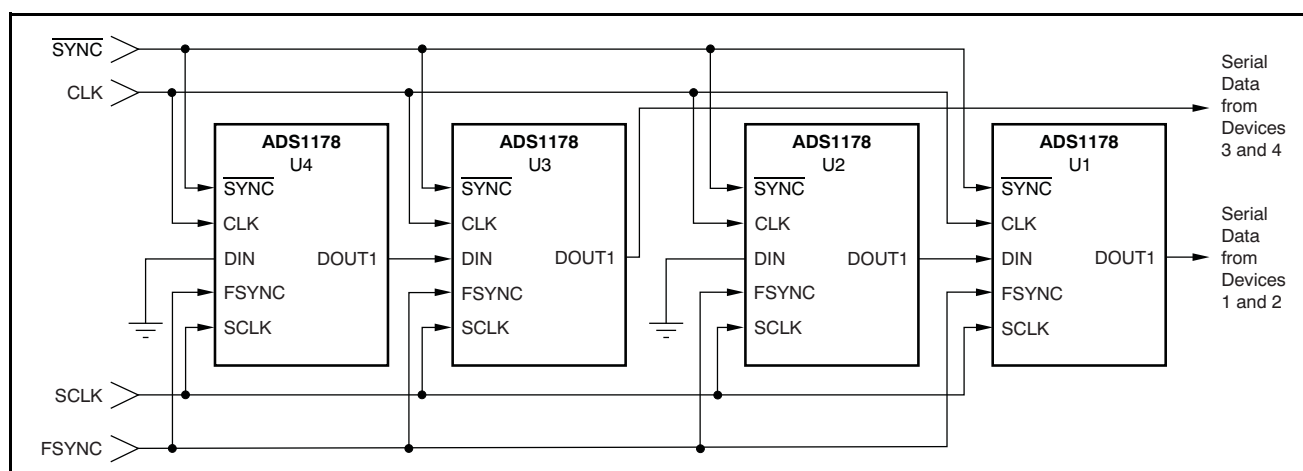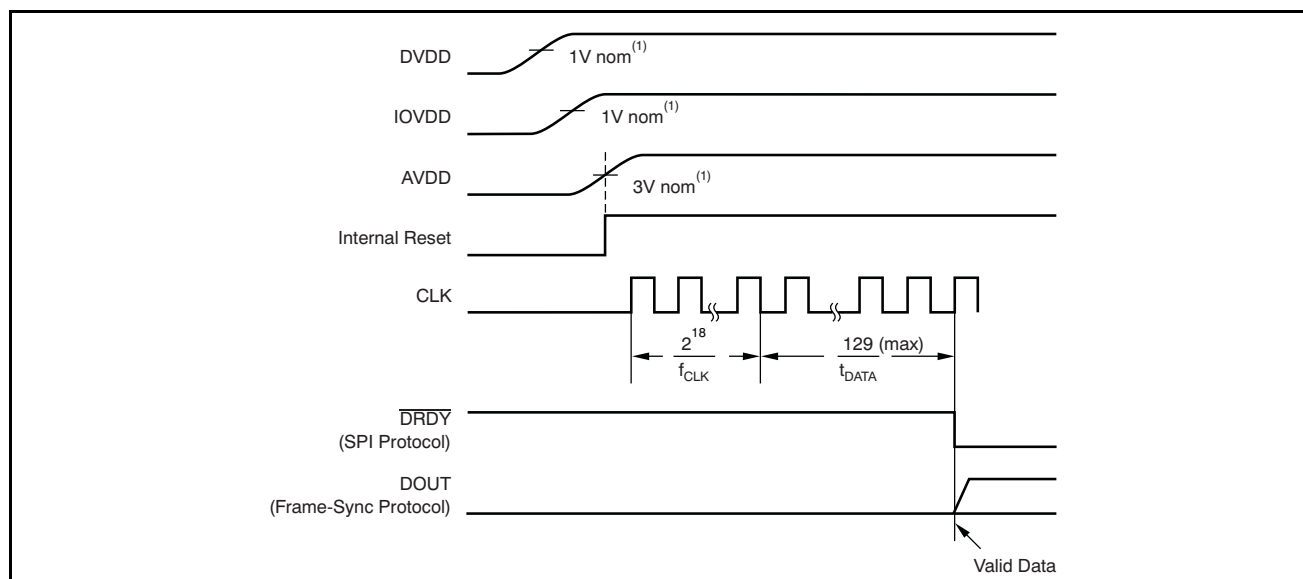


**Figure 23. Segmented DOUT Daisy-Chain, Frame-Sync Protocol (FORMAT[2:0] = 011 or 100)**

## POWER SUPPLIES

The ADS1174/78 has three power supplies: AVDD, DVDD, and IOVDD. AVDD is the analog supply that powers the modulator, DVDD is the digital supply that powers the digital core, and IOVDD is the digital I/O power supply. The IOVDD and DVDD power supplies can be tied together if desired (+1.8V). To achieve rated performance, it is critical that the power supplies are bypassed with 0.1µF and 10µF capacitors placed as close as possible to the supply pins. A single 10µF ceramic capacitor may be substituted in place of the two capacitors.

Figure 24 shows the start-up sequence of the ADS1174/78. At power-on, bring up the DVDD supply first, followed by IOVDD and then AVDD. Check the power-supply sequence for proper order, including the ramp rate of each supply. DVDD and IOVDD may

be sequenced at the same time if the supplies are tied together. Each supply has an internal reset circuit whose outputs are summed together to generate a global power-on reset. After the supplies have exceeded the reset thresholds, $2^{18}$ $f_{CLK}$ cycles are counted before the converter initiates the conversion process. Following the CLK cycles, the data for 129 conversions are suppressed by the ADS1174/78 to allow output of fully-settled data. In SPI protocol, $\overline{DRDY}$ is held high during this interval. In frame-sync protocol, DOUT is forced to zero. The power supplies should be applied before any analog or digital pin is driven. For consistent performance, assert $\overline{SYNC}$ after device power-on when data first appear.



(1) The power-supply reset thresholds are approximate.

**Figure 24. Start-Up Sequence**

**ADS1174**
**ADS1178**

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## PIN TEST USING TEST[1:0] INPUTS

Test mode allows continuity testing of the digital I/O pins. In this mode, the normal functions of the digital pins are disabled and routed to each other as pairs through internal logic, as shown in Table 13. Note that some of the digital input pins become outputs; this configuration should be taken into account when using test mode.

**Table 13. Test Mode Pin Map (TEST[1:0] = 11)**

| TEST MODE PIN MAP[1] | |
|---|---|
| INPUT PINS | OUTPUT PINS |
| $\overline{PWDN1}$ | DOUT1 |
| $\overline{PWDN2}$ | DOUT2 |
| $\overline{PWDN3}$ | DOUT3 |
| $\overline{PWDN4}$ | DOUT4 |
| $\overline{PWDN5}$ [2] | DOUT5[2] |
| $\overline{PWDN6}$ [2] | DOUT6[2] |
| $\overline{PWDN7}$ [2] | DOUT7[2] |
| $\overline{PWDN8}$ [2] | DOUT8[2] |
| MODE | DIN |
| FORMAT0 | CLKDIV |
| FORMAT1 | $\overline{DRDY}$/FSYNC |
| FORMAT2 | SCLK |

(1) The CLK input does not have a test output; $\overline{SYNC}$ = 1 and is an output.
(2) ADS1178 only.

The analog input, power supply, and ground pins remain connected as normal. The test mode is engaged by the setting the pins TEST[1:0] = 11. For normal converter operation, set TEST[1:0] = 00.

## VCOM OUTPUT

The VCOM pin is an analog output of approximately AVDD/2. This voltage may be used to set the common-mode voltage of the input buffers. The drive capability of this output is limited; most cases require an external buffer to minimize loading. A 0.1μF capacitor to AGND is recommended to reduce noise pick-up.
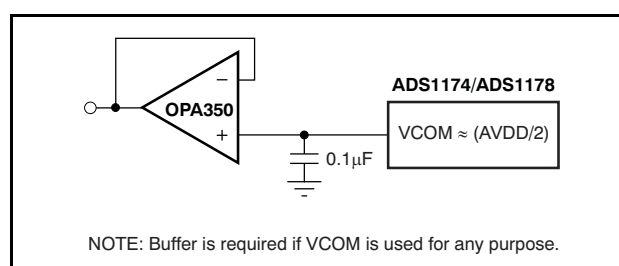


NOTE: Buffer is required if VCOM is used for any purpose.

**Figure 25. VCOM Output**

**TEXAS INSTRUMENTS**
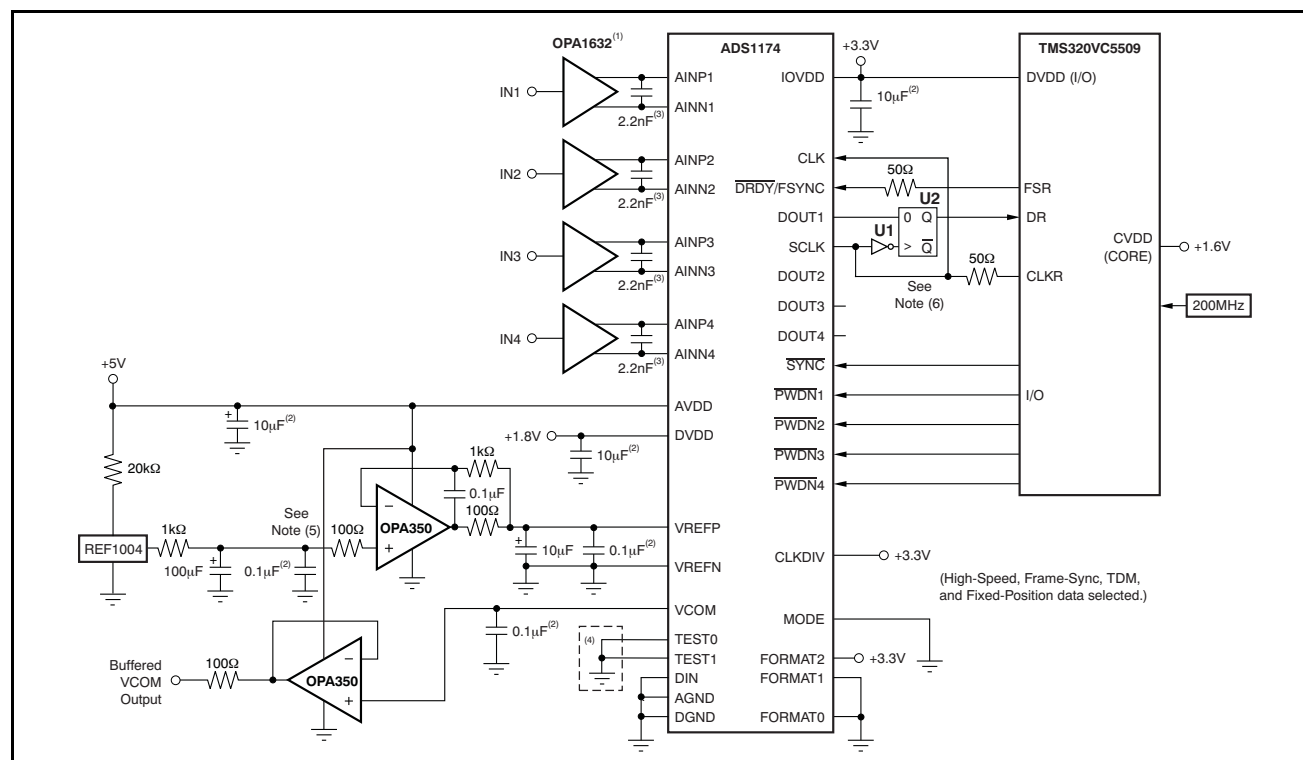
**ADS1174**
**ADS1178**

# APPLICATION INFORMATION

To obtain the specified performance from the ADS1174/78, the following layout and component guidelines should be considered.

1. **Power Supplies:** The device requires three power supplies for operation: DVDD, IOVDD, and AVDD. The range for DVDD is 1.65V to 1.95V; the range of IOVDD is 1.65V to 3.6V; and AVDD is restricted to 4.75V to 5.25V. For all supplies, use a 10μF tantalum capacitor, bypassed with a 0.1μF ceramic capacitor, placed close to the device pins. Alternatively, a single 10μF ceramic capacitor can be used. The supplies should be relatively free of noise and should not be shared with devices that produce voltage spikes (such as relays, LED display drivers, etc.). If a switching power-supply source is used, the voltage ripple should be low (< 2mV) and the switching frequency outside the passband of the converter.

2. **Ground Plane:** A single ground plane connecting both AGND and DGND pins can be used. If separate digital and analog grounds are used, connect the grounds together at the converter, or at the power entry point of the printed circuit board (PCB).

3. **Digital Inputs:** It is recommended to source-terminate the digital inputs to the device with 50Ω series resistors. The resistors should be placed close to the driving end of the digital source (oscillator, logic gates, DSP, etc.) This placement helps to reduce ringing on the digital lines, which may lead to degraded ADC performance.

4. **Analog/Digital Circuits:** Place analog circuitry (input buffer, reference) and associated tracks together, keeping them away from digital circuitry (DSP, microcontroller, logic). Avoid crossing digital tracks across analog tracks to reduce noise coupling and crosstalk.

5. **Reference Inputs:** It is recommended to use either a minimum 10μF tantalum with a 0.1μF ceramic capacitor, or a single 1μF ceramic capacitor, directly across the reference inputs, VREFP and VREFN. The reference input should be driven by a low-impedance source. For best performance, the reference should be low-noise.

6. **Analog Inputs:** The analog input pins must be driven differentially to achieve specified performance. A true differential driver or transformer (for ac applications) can be used for this purpose. Route the analog inputs tracks (AINP, AINN) as a pair from the buffer to the converter using short, direct tracks and away from digital tracks.

   A 1nF to 10nF capacitor should be used directly across the analog input pins, AINP and AINN. A low-k dielectric (such as COG or film type) should be used to maintain low THD. Capacitors from each analog input to ground can be used. They should be no larger than 1/10 the size of the difference capacitor (typically 100pF) to preserve the AC common-mode performance.

7. **Component Placement:** Place the power supply, analog input, and reference input bypass capacitors as close as possible to the device pins. This layout is particularly important for the small-value ceramic capacitors. Surface-mount components are recommended to avoid the higher inductance of leaded components.

Figure 26 to Figure 28 illustrate basic connections and interfaces that can be used with the ADS1174/78.

Product Folder Link(s): *ADS1174 ADS1178*

(1) External Schottky clamp diodes or series resistors may be needed to prevent overvoltage on the inputs. See the *Analog Inputs* section.

(2) Indicates ceramic capacitors.

(3) Indicates COG ceramic capacitors.

(4) For pin test mode, set to logic high.

(5) The op amp and input RC components filter the REF1004 noise.

(6) U1: SN74LVC1G04. U2: SN74LVC2G74. These components re-clock the ADS1174 data output to interface to the TMS320VC5509.

**Figure 26. ADS1174 Basic Connection Circuit**

Distributor of Texas Instruments: Excellent Integrated System Limited
Datasheet of ADS1174IPAPT - IC ADC 16BIT QUAD 64-HTQFP
Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com
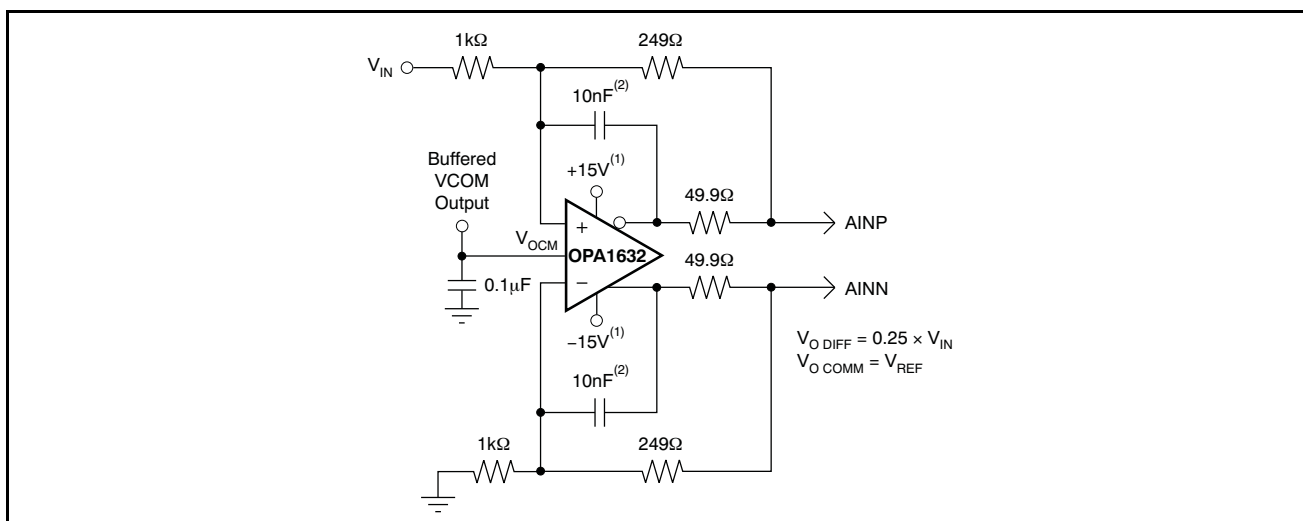
ADS1174
ADS1178

(1) Bypass with 10μF and 0.1μF capacitors.

(2) 15nF for Low-Speed mode.

**Figure 27. Basic Differential Input Signal Interface**



(1) Bypass with 10μF and 0.1μF capacitors.

(2) 56nF for Low-Speed mode.

**Figure 28. Basic Single-Ended Input Signal Interface**

**ADS1174**
**ADS1178**

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## PowerPAD THERMALLY-ENHANCED PACKAGING

The PowerPAD concept is implemented in standard epoxy resin package material. The integrated circuit is attached to the leadframe die pad using thermally conductive epoxy. The package is molded so that the leadframe die pad is exposed at a surface of the package. This exposure provides an extremely low thermal resistance to the path between the IC junction and the exterior case. The external surface of the leadframe die pad is located on the PCB side of the package, allowing the die pad to be attached to the PCB using standard flow soldering techniques. This soldering allows efficient attachment to the PCB and permits the board structure to be used as a heat-sink for the package. Using a thermal pad identical in size to the die pad and vias connected to the PCB ground plane, the board designer can now implement power packaging without additional thermal hardware (for example, external heat sinks) or the need for specialized assembly instructions.

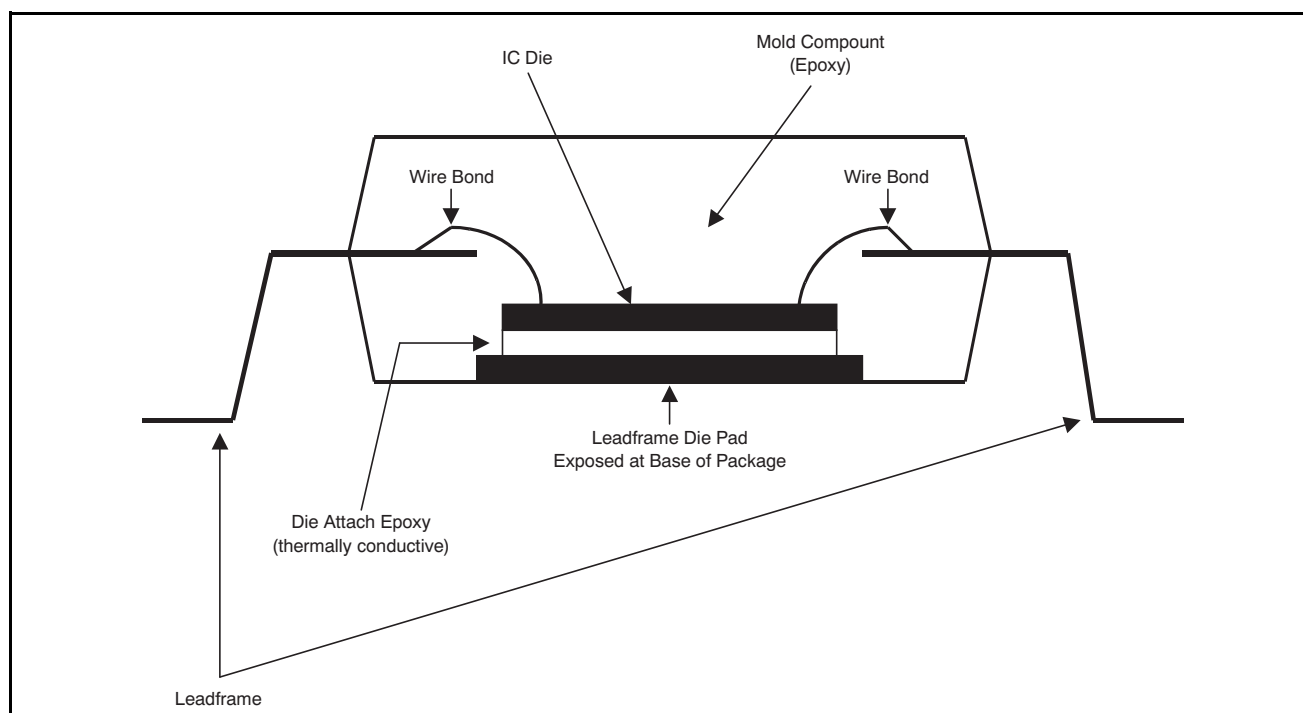Figure 29 illustrates a cross-section view of a PowerPAD package.



**Figure 29. Cross-Section View of a PowerPAD Thermally-Enhanced Package**

**PowerPAD PCB Layout Considerations for the ADS1174/78**

Figure 30 shows the recommended layer structure for thermal management when using a PowerPad package on a 4-layer PCB design. Note that the thermal pad is placed on both the top and bottom sides of the board. The ground plane is used as the heat-sink, while the power plane is thermally isolated from the thermal vias.

Figure 31 shows the required thermal pad etch pattern for the 64-lead HTQFP package used for the ADS1174/78. Nine 13mil (0.33mm) thermal vias plated with one ounce of copper are placed within the thermal pad area for the purpose of connecting the pad to the ground plane layer. The ground plane is used as a heatsink in this application. It is very important that the thermal via diameter be no larger than 13mils in order to avoid solder wicking during the reflow process. Solder wicking results in thermal voids that reduce heat dissipation efficiency and hamper heat flow away from the IC die.

The via connections to the thermal pad and internal ground plane should be plated completely around the hole, as opposed to the typical web or spoke thermal relief connection. Plating entirely around the thermal via provides the most efficient thermal connection to the ground plane.

**Additional PowerPAD Package Information**

Texas Instruments publishes the PowerPAD Thermally-Enhanced Package Application Report (TI literature number SLMA002), available for download at www.ti.com, which provides a more detailed discussion of PowerPAD design and layout considerations. Before attempting a board layout with the ADS1174/78, it is recommended that the hardware engineer and/or layout designer be familiar with the information contained in this document.



**Figure 30. Recommended PCB Structure for a 4-Layer Board**

**ADS1174**
**ADS1178**

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SBAS373B−OCTOBER 2007−REVISED SEPTEMBER 2008

**www.ti.com**
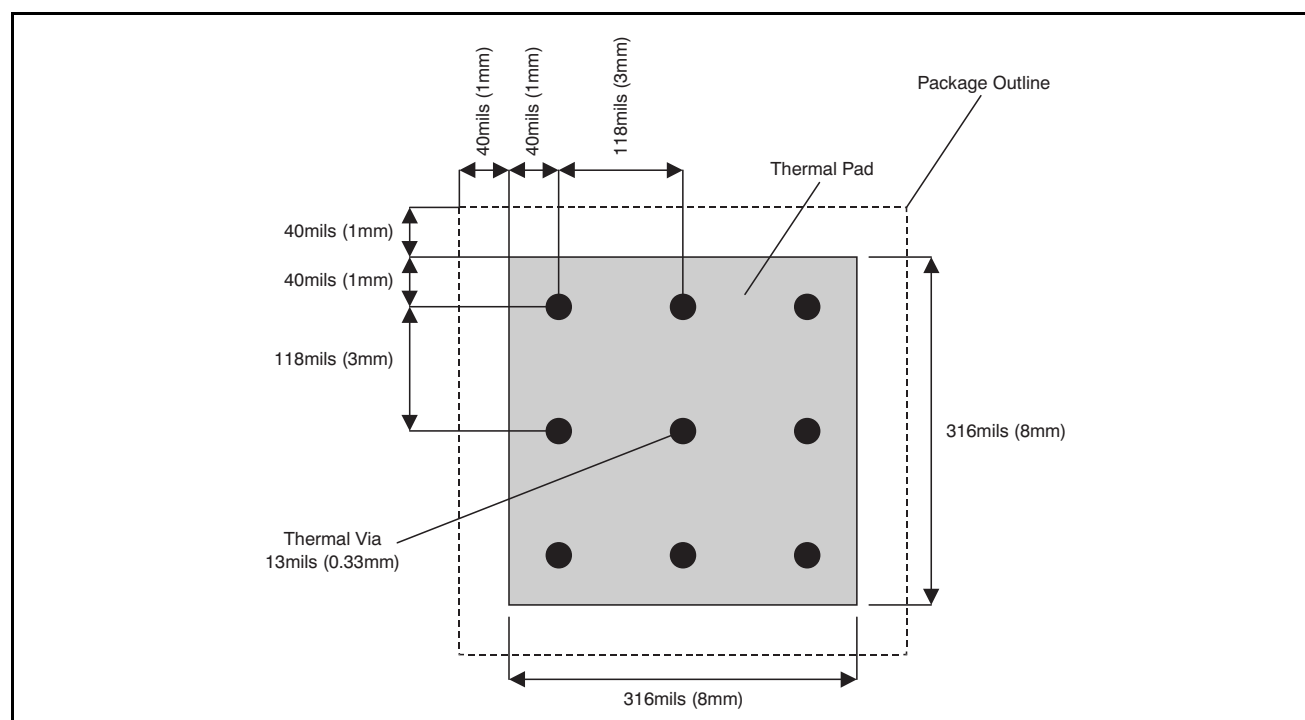


**Figure 31. Thermal Pad Etch and Via Pattern for the 64-Lead HTQFP Package**

# Revision History

**Changes from Revision A (December 2007) to Revision B**                                                **Page**

**PACKAGE OPTION ADDENDUM**

www.ti.com

10-Jun-2014

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS1174IPAPR | ACTIVE | HTQFP | PAP | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS1174 | Samples |
| ADS1174IPAPRG4 | ACTIVE | HTQFP | PAP | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS1174 | Samples |
| ADS1174IPAPT | ACTIVE | HTQFP | PAP | 64 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS1174 | Samples |
| ADS1174IPAPTG4 | ACTIVE | HTQFP | PAP | 64 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS1174 | Samples |
| ADS1178IPAPR | ACTIVE | HTQFP | PAP | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS1178 | Samples |
| ADS1178IPAPT | ACTIVE | HTQFP | PAP | 64 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS1178 | Samples |
| ADS1178IPAPTG4 | ACTIVE | HTQFP | PAP | 64 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS1178 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**PACKAGE OPTION ADDENDUM**

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10-Jun-2014

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(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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# PACKAGE MATERIALS INFORMATION

www.ti.com                                                                                           2-Sep-2015

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

Reel Diameter

Reel Width (W1)

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

Sprocket Holes

| Q1 | Q2 |
|---|---|
| Q3 | Q4 |

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS1174IPAPR | HTQFP | PAP | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 1.5 | 16.0 | 24.0 | Q2 |
| ADS1174IPAPT | HTQFP | PAP | 64 | 250 | 180.0 | 24.4 | 13.0 | 13.0 | 1.5 | 16.0 | 24.0 | Q2 |
| ADS1178IPAPR | HTQFP | PAP | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 1.5 | 16.0 | 24.0 | Q2 |
| ADS1178IPAPT | HTQFP | PAP | 64 | 250 | 180.0 | 24.4 | 13.0 | 13.0 | 1.5 | 16.0 | 24.0 | Q2 |

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# PACKAGE MATERIALS INFORMATION

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2-Sep-2015

## TAPE AND REEL BOX  DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS1174IPAPR | HTQFP | PAP | 64 | 1000 | 367.0 | 367.0 | 45.0 |
| ADS1174IPAPT | HTQFP | PAP | 64 | 250 | 213.0 | 191.0 | 55.0 |
| ADS1178IPAPR | HTQFP | PAP | 64 | 1000 | 367.0 | 367.0 | 45.0 |
| ADS1178IPAPT | HTQFP | PAP | 64 | 250 | 213.0 | 191.0 | 55.0 |

**MECHANICAL DATA**

PAP (S−PQFP−G64)          PowerPAD™  PLASTIC QUAD FLATPACK



Thermal Pad
(See Note D)

0,50

0,27
0,17     ⊕ 0,08 Ⓜ

48            33

49            32

64            17

1            16

7,50 TYP

10,20
9,80     SQ

12,20
11,80     SQ

1,05
0,95

1,20 MAX

Seating Plane

⌒ 0,08

0,13 NOM

Gage Plane

0,25

0,15
0,05

0,75
0,45

0°−7°

4147702/C 08/03

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion
         D.   This package is designed to be soldered to a thermal pad on the board.   Refer to Technical Brief, PowerPad
              Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
              recommended board layout.   This document is available at www.ti.com <http://www.ti.com>.
         E.   Falls within JEDEC MS−026

PowerPAD is a trademark of Texas Instruments.

# THERMAL PAD MECHANICAL DATA
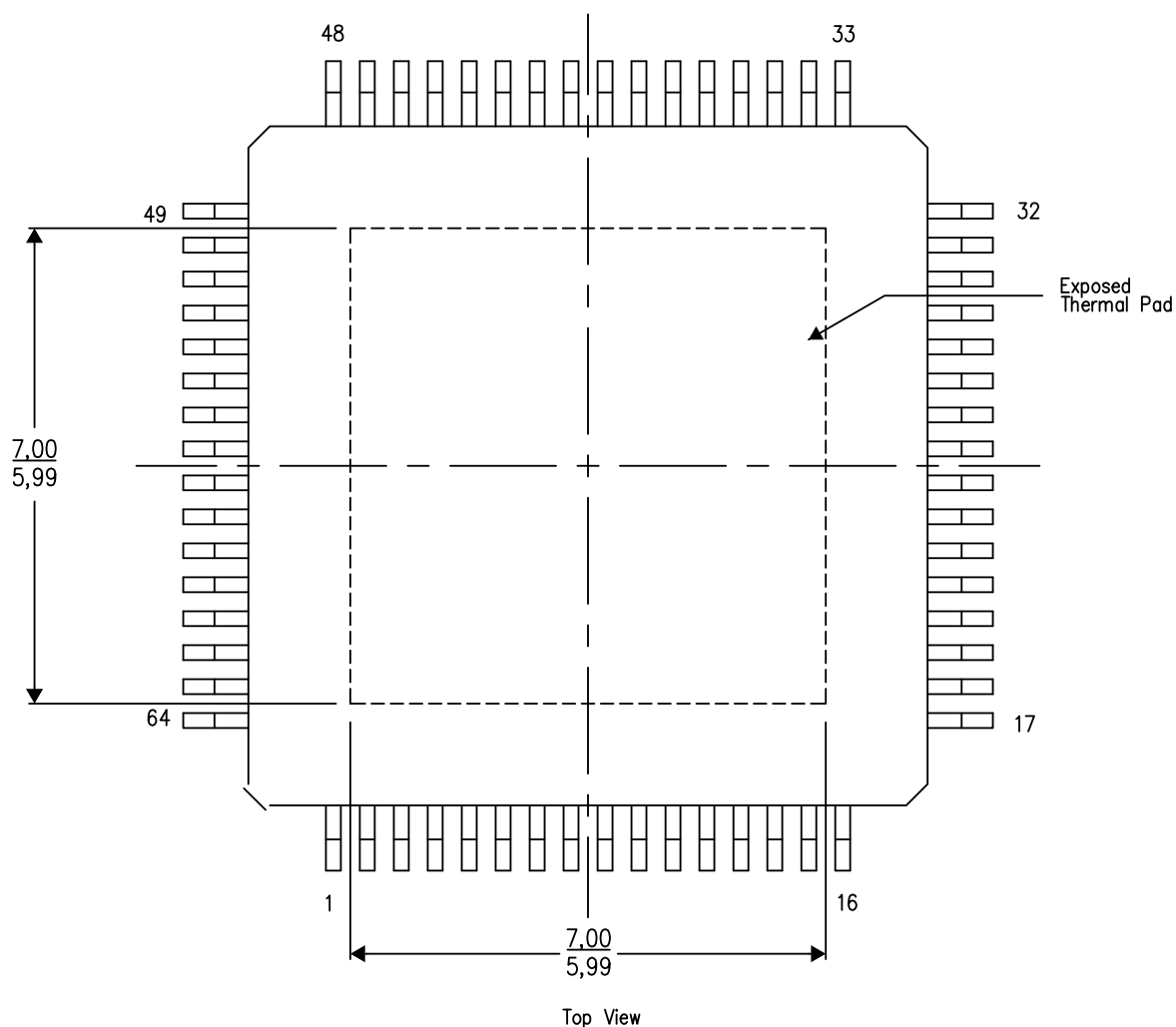
PAP (S–PQFP–G64)                    PowerPAD™ PLASTIC QUAD FLATPACK

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
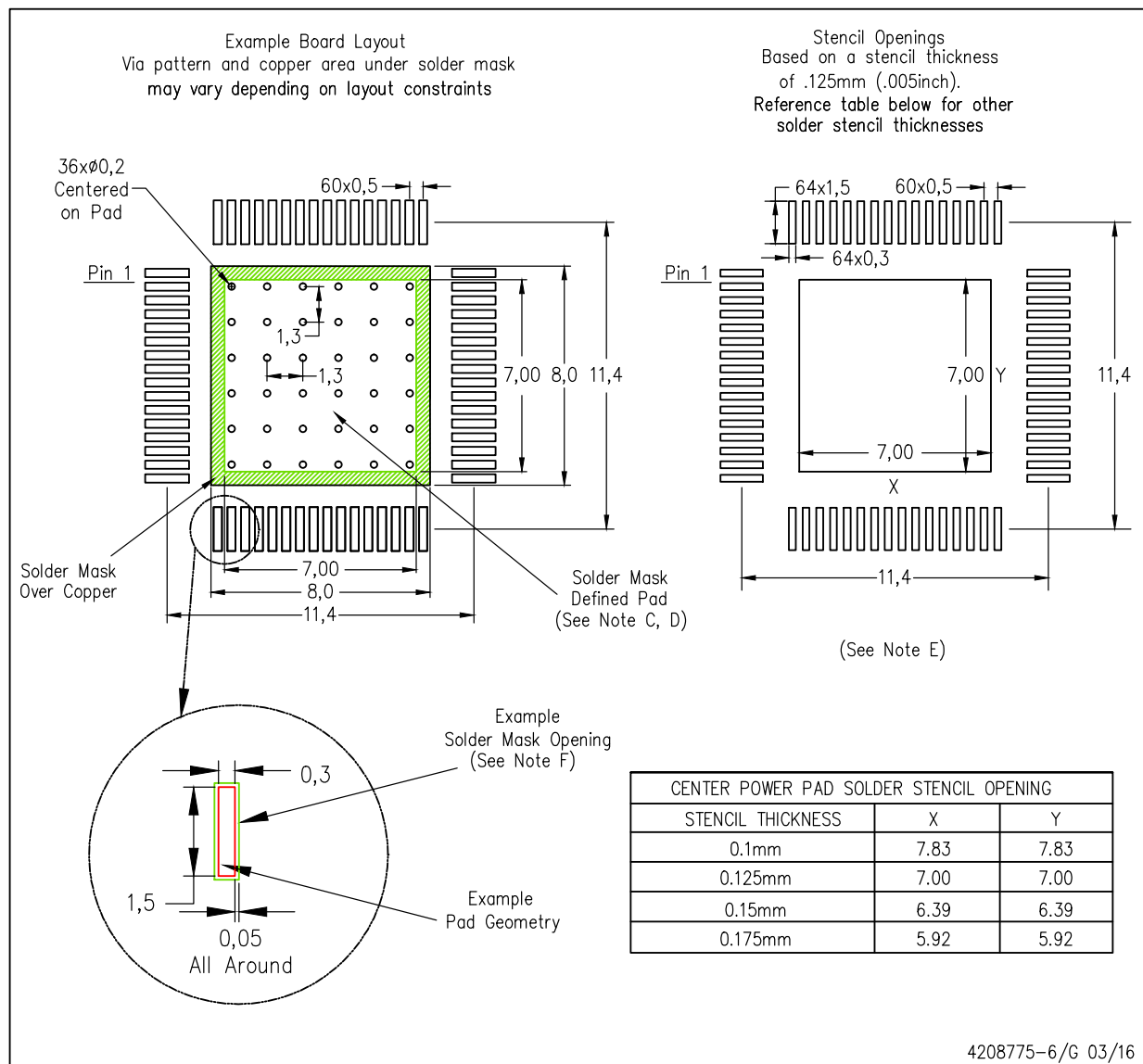


Top View

Exposed Thermal Pad Dimensions

4206326–5/P    05/14

NOTES:   A. All linear dimensions are in millimeters
PowerPAD is a trademark of Texas Instruments

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**LAND PATTERN DATA**

PAP (S−PQFP−G64)  PowerPAD™ PLASTIC QUAD FLATPACK

Example Board Layout
Via pattern and copper area under solder mask
may vary depending on layout constraints

Stencil Openings
Based on a stencil thickness
of .125mm (.005inch).
Reference table below for other
solder stencil thicknesses

36x⌀0,2
Centered
on Pad

60x0,5

Pin 1

1,3

1,3

7,00 8,0 11,4

Solder Mask
Over Copper

7,00
8,0
11,4

Solder Mask
Defined Pad
(See Note C, D)

64x1,5  60x0,5
64x0,3

Pin 1

7,00 Y  11,4

7,00
X

11,4

(See Note E)

Example
Solder Mask Opening
(See Note F)

0,3

1,5

0,05
All Around

Example
Pad Geometry

| CENTER POWER PAD SOLDER STENCIL OPENING | | |
|---|---|---|
| STENCIL THICKNESS | X | Y |
| 0.1mm | 7.83 | 7.83 |
| 0.125mm | 7.00 | 7.00 |
| 0.15mm | 6.39 | 6.39 |
| 0.175mm | 5.92 | 5.92 |

4208775−6/G 03/16

**PowerPAD is a trademark of Texas Instruments**

NOTES:  A.  All linear dimensions are in millimeters.
B.  This drawing is subject to change without notice.
C.  Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D.  This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC−7351 is recommended for alternate designs.
E.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC−7525 for other stencil recommendations.
F.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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