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Diodes Incorporated
DLP03LC-7

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sales@integrated-circuit.com

NOT RECOMMENDED FOR NEW DESIGNS

DLP03LC

Lead-free Green

LOW CAPACITANCE UNIDIRECTIONAL TVS

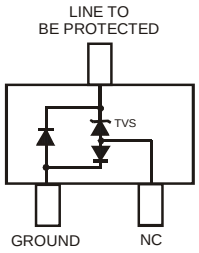
Features

- 350 Watts Peak Pulse Power (tp = 8x20μs)
- Transient Protection for data, signal, and V_{CC} bus to IEC61000-4-2 level 4 (ESD)
- Low Capacitance, typ. = 4pF
- Unidirectional Configuration
- **Lead Free/RoHS Compliant (Note 4)**
- **"Green" Device (Note 5)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: SOT-23
- Case Material: Molded Plastic, "Green" Molding Compound, Note 4. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Matte Tin Finish annealed over Alloy 42 leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208
- Marking Information: See Page 3
- Ordering Information: See Page 3
- Weight: 0.0083 grams (approximate)

Top View



Device Schematic

Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Peak Pulse Power (tp = 8x20μs)	P_{pk}	350	W

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	460	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics @T_A = 25°C unless otherwise specified

Reverse Standoff Voltage	Breakdown Voltage V_{BR} @ I_T		Test Current	Max. Reverse Leakage @ V_{RWM}	Max. Clamping Voltage @ I_p = 1A (Note 3)	Max. Clamping Voltage V_C @ I_{pp}	Max. Peak Pulse Current (Note 2)	Typical Total Capacitance (Note 1)
V_{RWM} (V)	Min (V)	Max (V)	I_T (mA)	I_R (μA)	V_C (V)	(V)	(A)	(pF)
3.3	4.0	—	1.0	110	8	18	20	4

Notes:
1. V_R = 0V, f = 1MHz.
2. tp = 8x20μs.
3. Clamping voltage value is based on an 8x20 μs peak pulse current (I_{pp}) waveform.
4. No purposefully added lead.
5. Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com/products/lead_free/index.php.
6. Device mounted on FR-4 PCB with pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

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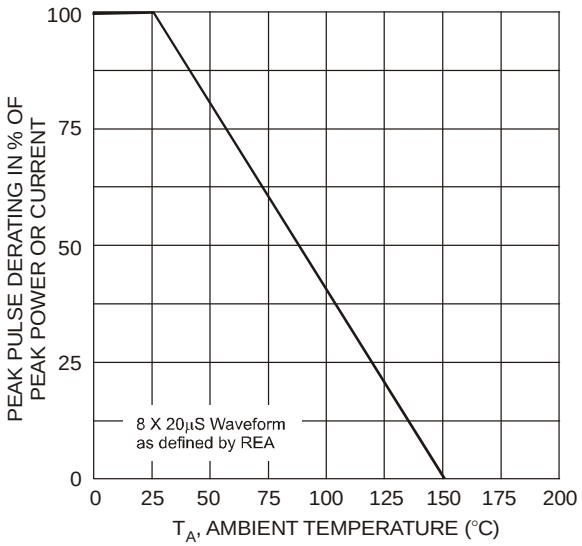


Fig. 1 Pulse Derating Curve

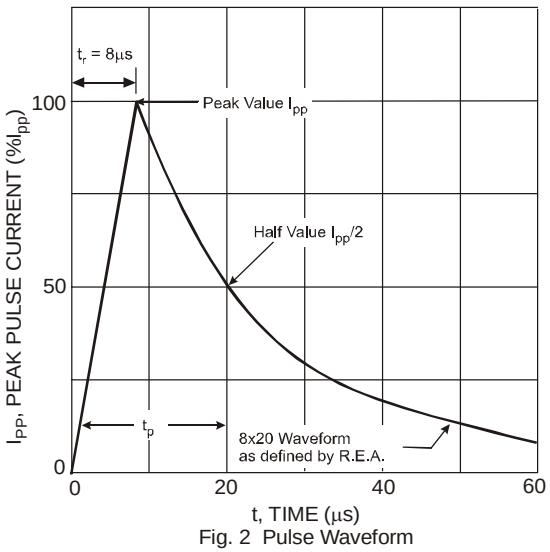


Fig. 2 Pulse Waveform

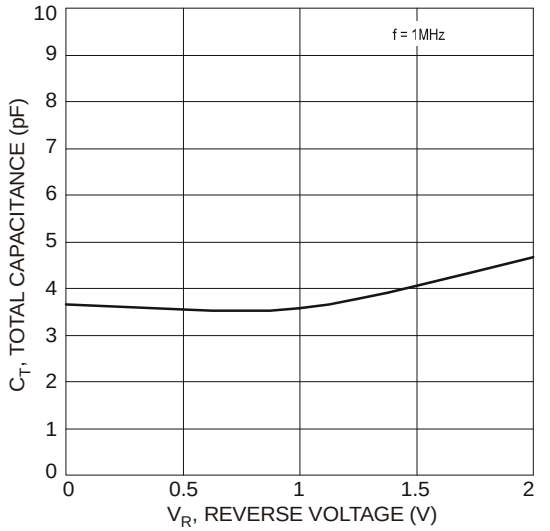


Fig. 3 Typical Total Capacitance vs. Reverse Voltage

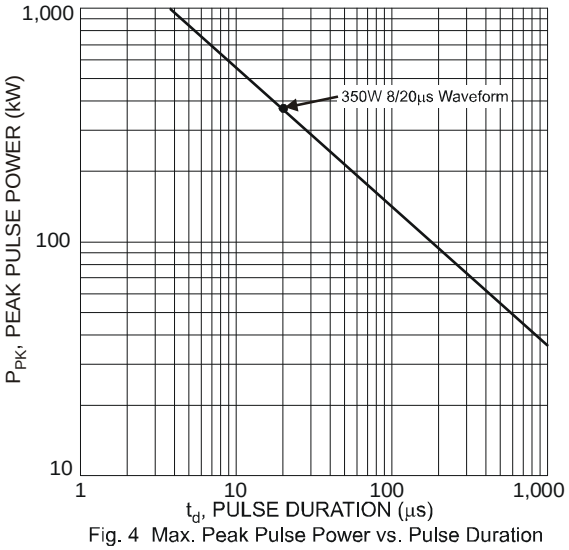


Fig. 4 Max. Peak Pulse Power vs. Pulse Duration

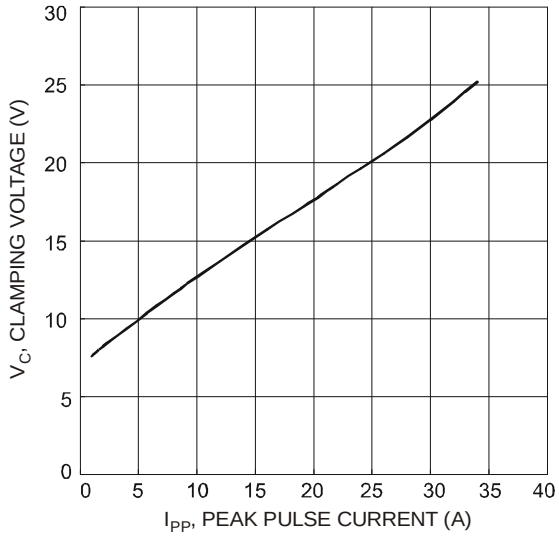


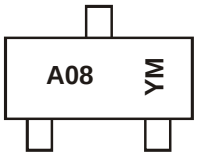
Fig. 5 Typical Clamping Voltage vs. Peak Pulse Current (Note 2)

Ordering Information (Note 7)

Part Number	Case	Packaging
DLP03LC-7	SOT-23	3000/Tape & Reel

Notes: 7. For packaging details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.

Marking Information



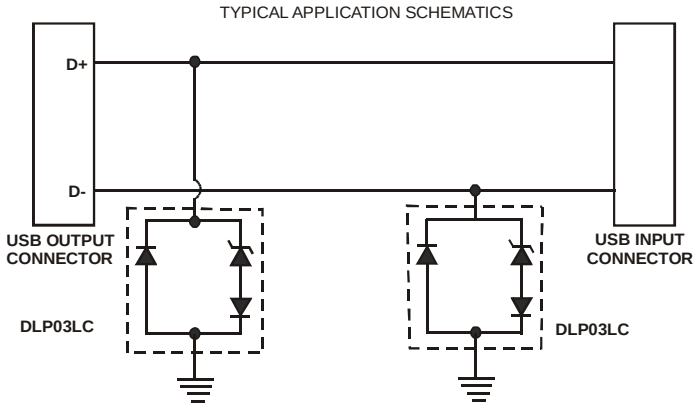
A08 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: U = 2007)
M = Month (ex: 9 = September)

Date Code Key

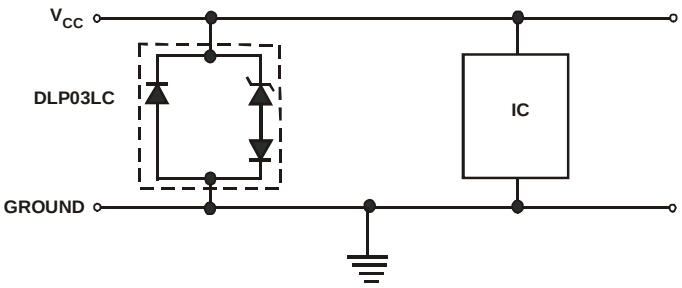
Year	2007	2008	2009	2010	2011	2012	2013	2014	2015
Code	U	V	W	X	Y	Z	A	B	C

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Typical Application Schematics



TYPICAL USB DATA LINE APPLICATION



TYPICAL V_{CC} POWER LINE PROTECTION

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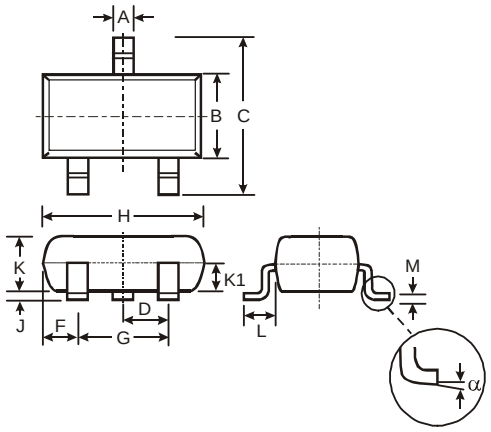
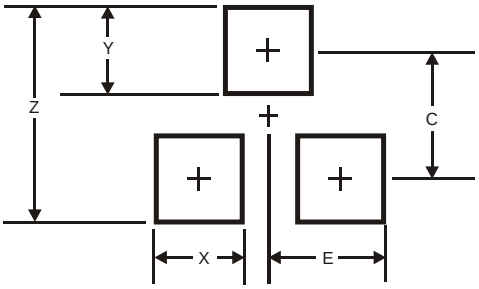
Package Outline Dimensions



SOT-23			
Dim	**Min**	**Max**	**Typ**
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.903	1.10	1.00
K1	-	-	0.400
L	0.45	0.61	0.55
M	0.085	0.18	0.11
α	0°	8°	-
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
Z	2.9
X	0.8
Y	0.9
C	2.0
E	1.35

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