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TLV3492AMDREP

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TLV3491A-EP, TLV3492A-EP, TLV3494A-EP

SGDS035−DECEMBER 2007

1.8 V, NANOPOWER, PUSH/PULL OUTPUT COMPARATORS

FEATURES

- **Very Low Supply Current: 0.8 μA (Typical)**
- **Input Common Mode Range 200 mV Beyond Supply Rails**
- **Supply Voltage: 1.8 V to 5.5 V**
- **High Speed: 6 μs**
- **Push/Pull CMOS Output Stage**
- **Controlled Baseline**
    - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree**

Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

APPLICATIONS

- **Portable Medical Equipment**
- **Wireless Security Systems**
- **Remote Control Systems**
- **Handheld Instruments**
- **Ultra-Low Power Systems**

DESCRIPTION/ORDERING INFORMATION

The TLV349x family of push/pull output comparators features a fast 6μs response time and <1.2 μA (max) nanopower capability, allowing operation from 1.8 V to 5.5 V. Input common-mode range beyond supply rails make the TLV349x an ideal choice for low-voltage applications.

The TLV349x is excellent for power-sensitive, low-voltage (2-cell) applications.

TLV349x RELATED PRODUCTS

PRODUCT	FEATURES
TLV370x	550 nA, 2.5 V to 16 V, Push-Pull CMOS Output Stage Comparator
TLV340x	550 nA, 2.5 V to 16 V, Open-Drain Output Stage Comparator

ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[2]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERABLE PART NUMBER	TRANSPORT MEDIA, QUANTITY
TLV3491	SO-8	D	–55°C to 125°C	3491EP	TLV3491AMDREP[3]	Tape and Reel, 2500
TLV3492	SO-8	D	–55°C to 125°C	3492EP	TLV3492AMDREP	Tape and Reel, 2500
TLV3494	SO-14	D	–55°C to 125°C	3494EP	TLV3494AMDREP[3]	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Prouct Preview. Contact your Texas Instruments Sales Representative for availability.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
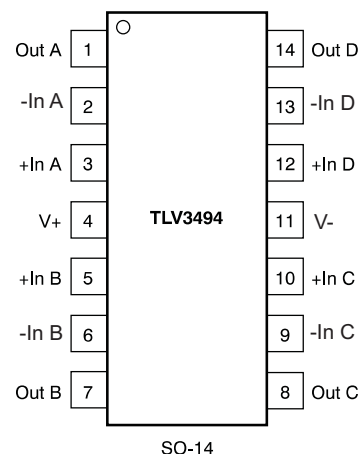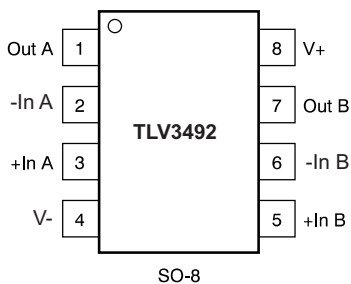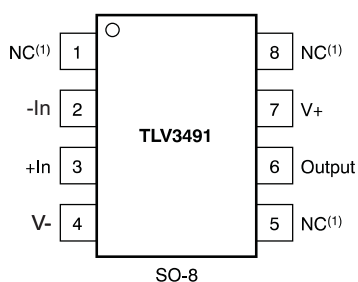
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ABSOLUTE MAXIMUM RATINGS[1]

		VALUE	UNIT
Supply Voltage		5.5	V
Signal Input Terminals	Voltage[2]	$(V-) - 0.5$ to $(V+) + 0.5$	V
	Current[2]	±10	mA
Output Short-Circuit[3]		Continuous	
Operating Temperature		−55 to 125	°C
Storage Temperature		−65 to 150	°C
Junction Temperature		150	°C
Lead Temperature (soldering, 10s)		300	°C
ESD Rating (Human Body Model)		3000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

PIN CONFIGURATIONS

Top View

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Product Folder Link(s): *TLV3491A-EP TLV3492A-EP TLV3494A-EP*

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ELECTRICAL CHARACTERISTICS

At T_A = 25°C, and V_S = 1.8 V to 5.5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		T_A[1]	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE								
Input Offset Voltage	V_{OS}	V_{CM} = 0V, I_O = 0mA		25°C		±3	±15	mV
				Full Range			±25	
vs Temperature	dV_{OS}/dT	T_A = −55°C to 125°C				±12		µV/°C
vs Power Supply	PSRR	V_S = 1.8 V to 5.5 V		25°C		350	1000	µV/V
				Full Range			1600	
INPUT BIAS CURRENT								
Input Bias Current	I_B	V_{CM} = V_{CC}/2		25°C		±1	±50	pA
				Full Range			±1600	
Input Offset Current	I_{OS}	V_{CM} = V_{CC}/2		25°C		±1	±50	pA
				Full Range			±200	
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range	V_{CM}				(V−) − 0.2		(V+) + 0.2	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −0.2 V to (V+) − 1.5 V		25°C	60	74		dB
				Full Range	55			
		V_{CM} = −0.2 V to (V+) + 0.2 V		25°C	54	62		
				Full Range	50			
INPUT CAPACITANCE								
Common-Mode						2		pF
Differential						4		pF
SWITCHING CHARACTERISTICS								
Propagation Delay Time, Low-to-High	$t_{(PLH)}$	f = 10 kHz, V_{STEP} = 1 V	Input Overdrive = 10 mV			12		µs
			Input Overdrive = 100 mV			6		µs
Propagation Delay Time, High-to-Low	$t_{(PHL)}$	f = 10 kHz, V_{STEP} = 1 V	Input Overdrive = 10 mV			13.5		µs
			Input Overdrive = 100 mV			6.5		µs
Rise Time	t_R	C_L = 10 pF				100		ns
Fall Time	t_F	C_L = 10 pF				100		ns
OUTPUT								
Voltage Output High from Rail	V_{OH}	V_S = 5 V, I_{OUT} = -5 mA		Full Range		90	300	mV
Voltage Output Low from Rail	V_{OL}	V_S = 5 V, I_{OUT} = 5 mA		Full Range		160	300	mV
Short-Circuit Current	I_{SC}			See Typical Characteristics				
POWER SUPPLY								
Specified Voltage Range	V_S				1.8		5.5	V
Quiescent Current[2]	I_Q	V_s = 5.5 V, V_O = High		25°C		0.85	1.2	µA
				Full Range			2.1	
TEMPERATURE RANGE								
Specified Range	T_A				−55		125	°C
Storage Range					−65		150	°C
Thermal Resistance, θ_{JA}								
SO-8						165		°C/W
SO-14						133		°C/W

(1) Full Range is -55°C to 125°C.
(2) I_Q per channel.

Product Folder Link(s): *TLV3491A-EP TLV3492A-EP TLV3494A-EP*

TLV3491A-EP, TLV3492A-EP, TLV3494A-EP

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TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = 1.8 V to 5.5 V, and Input Overdrive = 100 mV, unless otherwise noted.
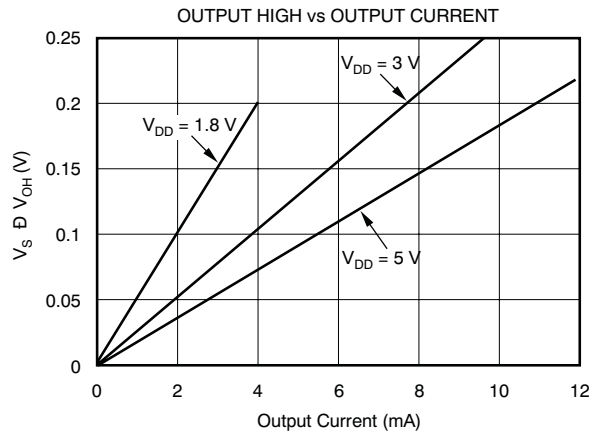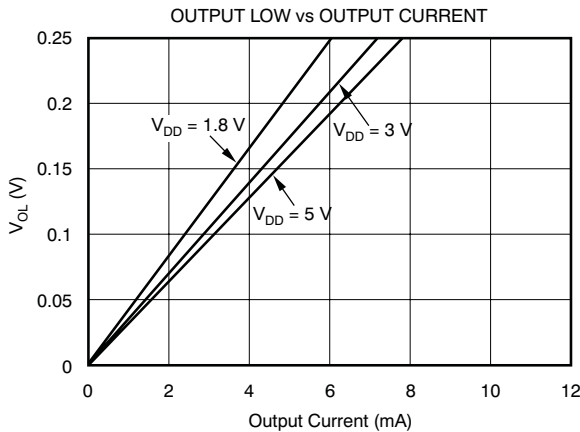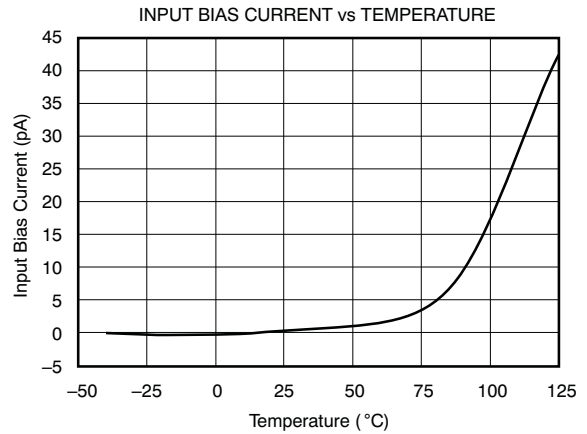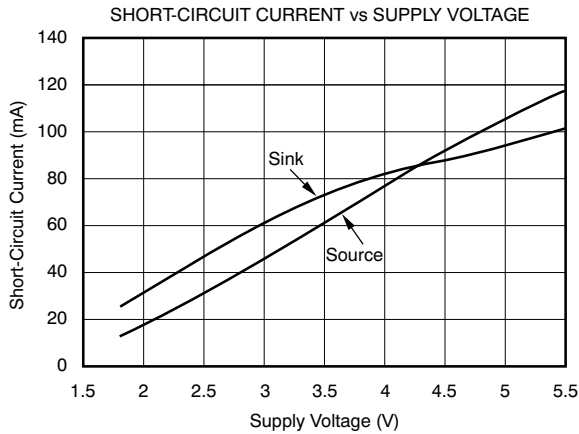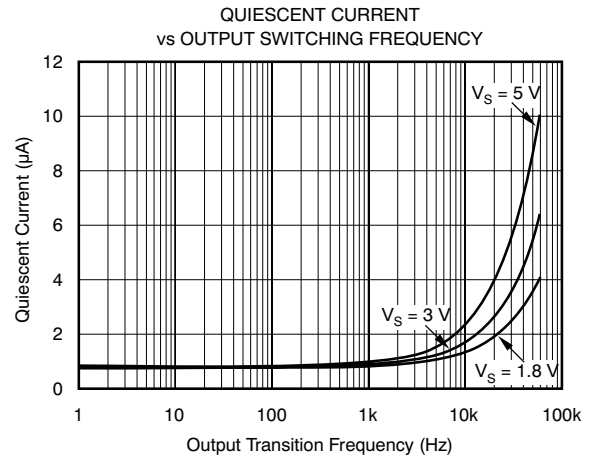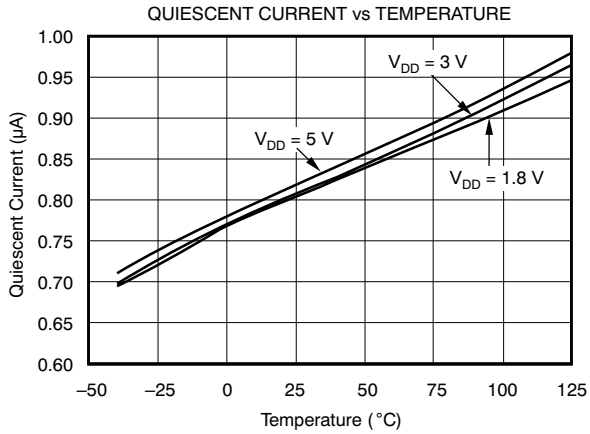
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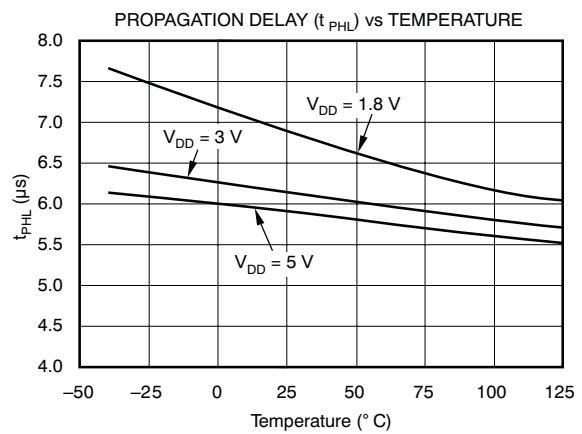www.ti.com

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TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = 1.8 V to 5.5 V, and Input Overdrive = 100 mV, unless otherwise noted.
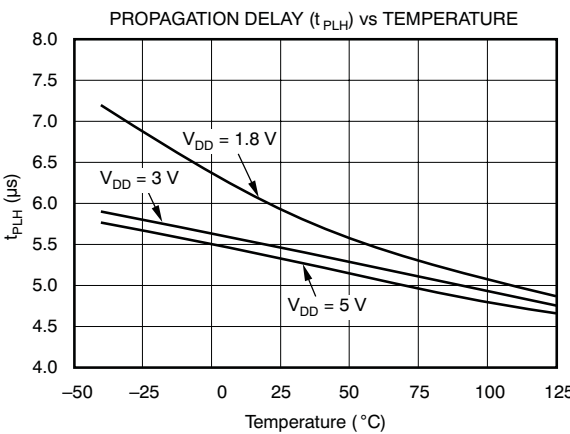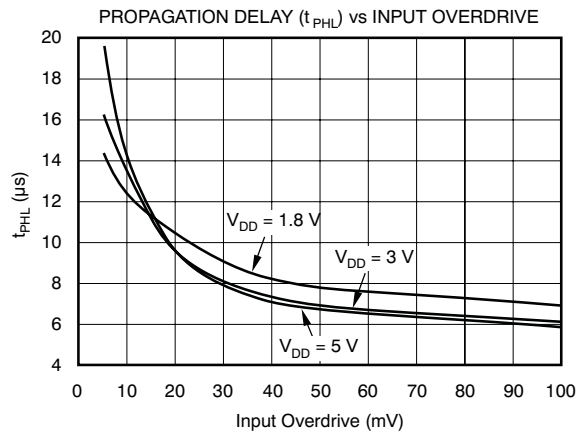
TLV3491A-EP, TLV3492A-EP, TLV3494A-EP

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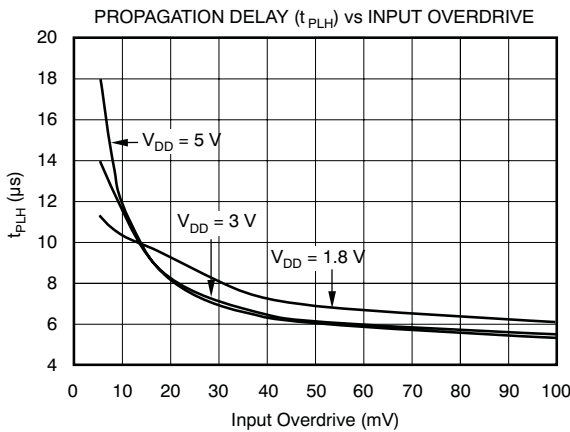## TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = 1.8 V to 5.5 V, and Input Overdrive = 100 mV, unless otherwise noted.

PROPAGATION DELAY (t_{PLH})

V_{DD} = ±2.5 V

V_{IN-}
V_{IN+}
500 mV/div

V_{OUT}
2V/div

2 µs/div

PROPAGATION DELAY (t_{PHL})

V_{DD} = ±2.5 V

V_{IN+}
V_{IN-}
500 mV/div

V_{OUT}
2V/div

2 µs/div

PROPAGATION DELAY (t_{PLH})

V_{DD} = ±0.9 V

V_{IN-}
V_{IN+}
500 mV/div

V_{OUT}
2V/div

2 µs/div

PROPAGATION DELAY (t_{PHL})

V_{DD} = ±0.9 V

V_{IN+}
V_{IN-}
500 mV/div

V_{OUT}
2V/div

2 µs/div

Product Folder Link(s): *TLV3491A-EP TLV3492A-EP TLV3494A-EP*

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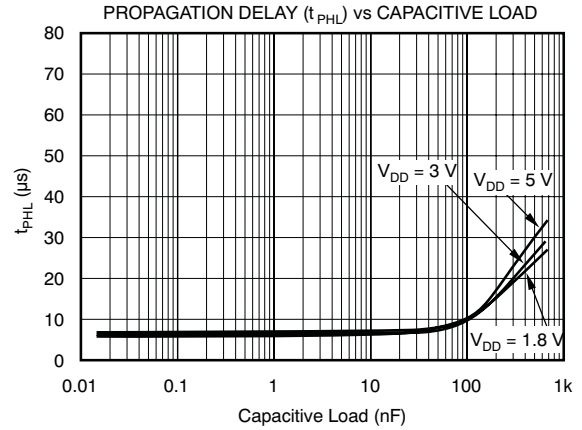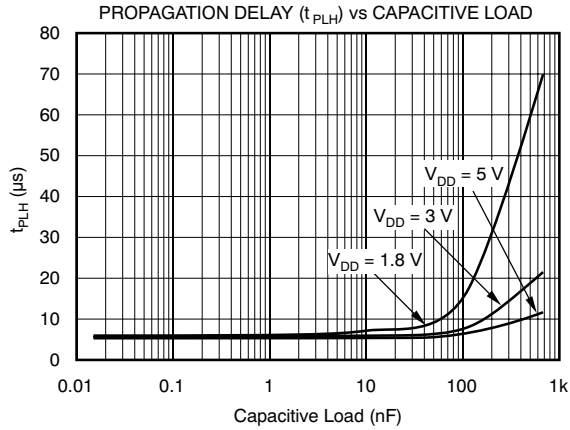
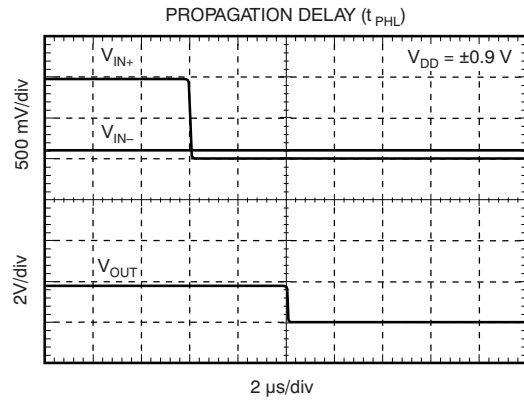### TLV3491A-EP, TLV3492A-EP, TLV3494A-EP

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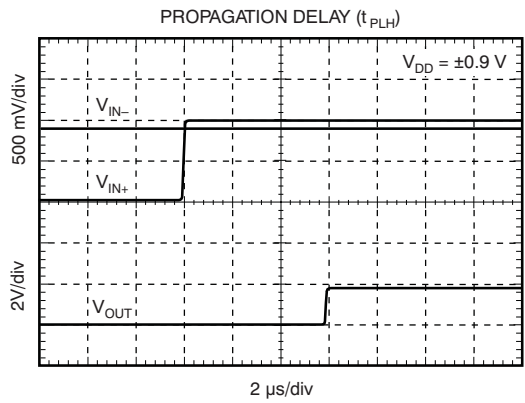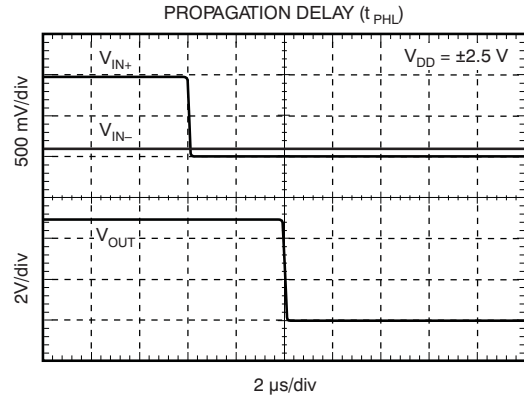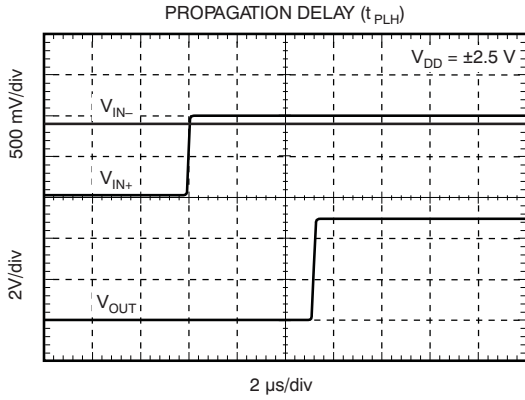
APPLICATION INFORMATION

The TLV349x family of comparators features rail-to-rail input and output on supply voltages as low as 1.8 V. The push/pull output stage is optimal for reduced power budget applications and features no shoot-through current. Low supply voltages, common-mode input range beyond supply rails, and a typical supply current of 0.8 µA make the TLV349x family an excellent candidate for battery-powered applications with single-cell operation.

BOARD LAYOUT

Figure 1 shows the typical connections for the TLV349x. To minimize supply noise, power supplies should be capacitively decoupled by a 0.01 µF ceramic capacitor in parallel with a 10 µF electrolytic capacitor. Comparators are very sensitive to input noise. Proper grounding (use of ground plane) will help maintain specified performance of the TLV349x family.
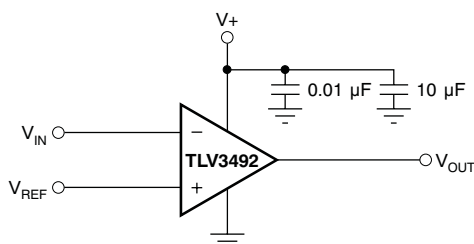

Figure 1. Basic Connections of the TLV3492

SETTING REFERENCE VOLTAGE

It is important to use a stable reference when setting the transition point for the TLV349x. The REF1004 provides a 1.25-V reference voltage with low drift and only 8 µA of quiescent current.

EXTERNAL HYSTERESIS

Comparator inputs have no noise immunity within the range of specified offset voltage (±15 mV). For noisy input signals, the comparator output may display multiple switching as input signals move through the switching threshold. The typical comparator threshold of the TLV349x is ±15 mV. To prevent multiple switching within the comparator threshold of the TLV349x, external hysteresis may be added by connecting a small amount of feedback to the positive input. Figure 2 shows a typical topology used to introduce hysteresis, described by the equation:

$$V_{HYST} = \frac{V^+ \times R1}{R_1 + R_2}$$

V_{HYST} will set the value of the transition voltage required to switch the comparator output by increasing the threshold region, thereby reducing sensitivity to noise.
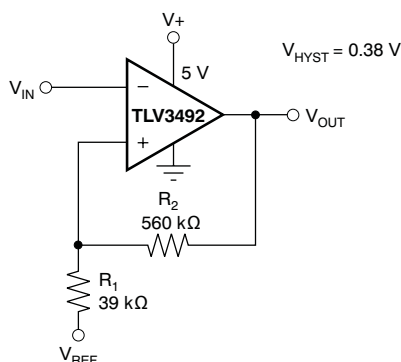

Figure 2. Adding Hysteresis to the TLV3492

TLV3491A-EP, TLV3492A-EP, TLV3494A-EP

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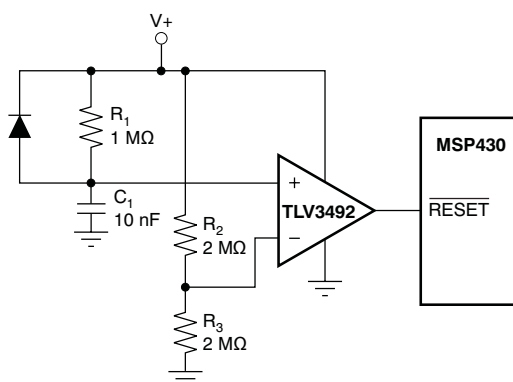SGDS035–DECEMBER 2007

RELAXATION OSCILLATOR

The TLV3492 can be configured as a relaxation oscillator to provide a simple and inexpensive clock output (see Figure 3). The capacitor is charged at a rate of 0.69 RC. It also discharges at a rate of 0.69 RC. Therefore, the period is 1.38 RC. R_1 may be a different value than R_2.
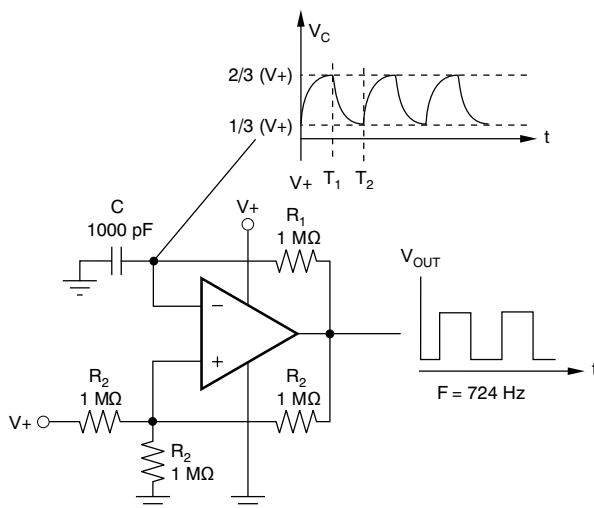
Figure 3. TLV3492 Configured as a Relaxation Oscillator

POWER-ON RESET

The reset circuit shown in Figure 4 provides a time delayed release of reset to the MSP430 microcontroller. Operation of the circuit is based on a stabilization time constant of the supply voltage, rather than on a predetermined voltage value. The negative input is a reference voltage created by a simple resistor divider. These resistor values should be relatively high to reduce the current consumption of the circuit. The positive input is an RC circuit that provides a power-up delay. When power is applied, the output of the comparator is low, holding the processor in the reset condition. Only after allowing time for the supply voltage to stabilize does the positive input of the comparator become higher than the negative input, resulting in a high output state and releasing the processor for operation. The stabilization time required for the supply voltage is adjustable by the selection of the RC component values. Use of a lower-valued resistor in this portion of the circuit will not increase current consumption because no current flows through the RC circuit after the supply has stabilized. The reset delay time needed depends on the power-up characteristics of the system power supply. R_1 and C_1 are selected to allow enough time for the power supply to stabilize. D1 provides rapid reset if power is lost. In this example, the $R_1 \bullet C_1$ time constant is 10 ms.

Figure 4. The TLV349x Configured as a Reset Circuit for the MSP430.

Product Folder Link(s): *TLV3491A-EP TLV3492A-EP TLV3494A-EP*

PACKAGE OPTION ADDENDUM

www.ti.com   31-May-2014

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3492AMDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	3492EP	Samples
V62/07635-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	3492EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM
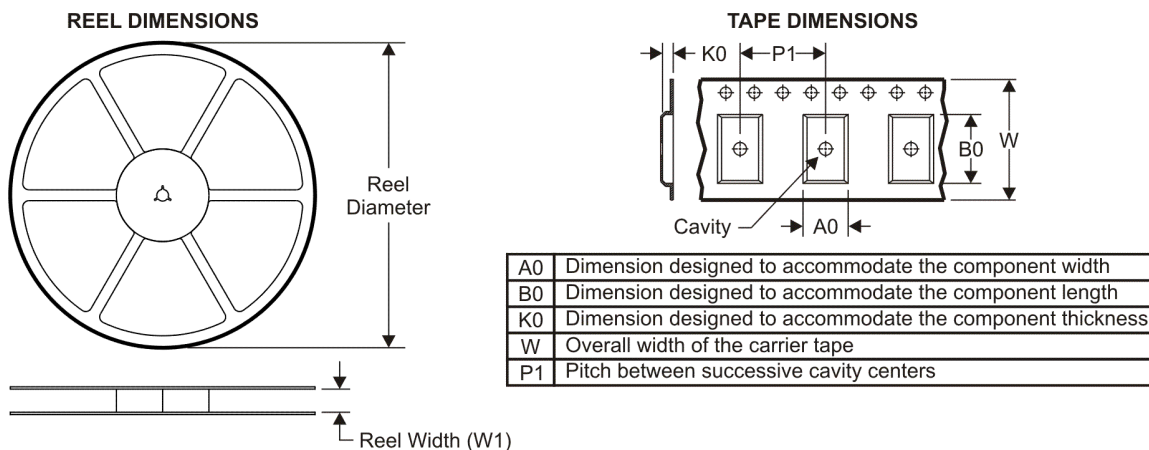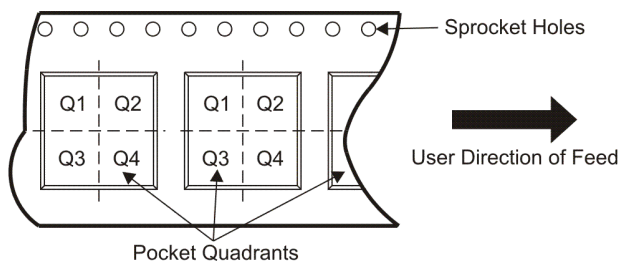
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31-May-2014

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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PACKAGE MATERIALS INFORMATION

22-Aug-2008

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

| A0 | Dimension designed to accommodate the component width |
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3492AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

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PACKAGE MATERIALS INFORMATION

22-Aug-2008

TAPE AND REEL BOX DIMENSIONS
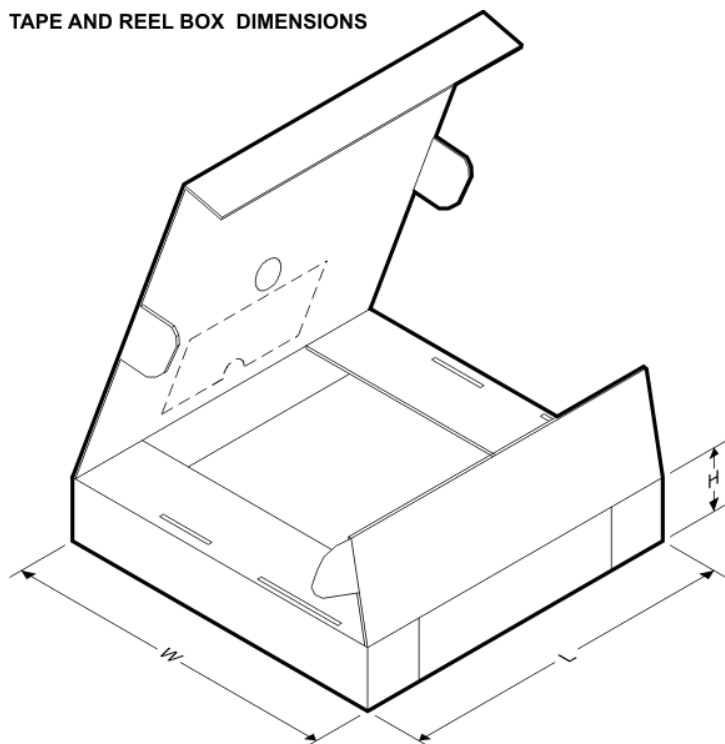
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3492AMDREP	SOIC	D	8	2500	340.5	338.1	20.6

MECHANICAL DATA

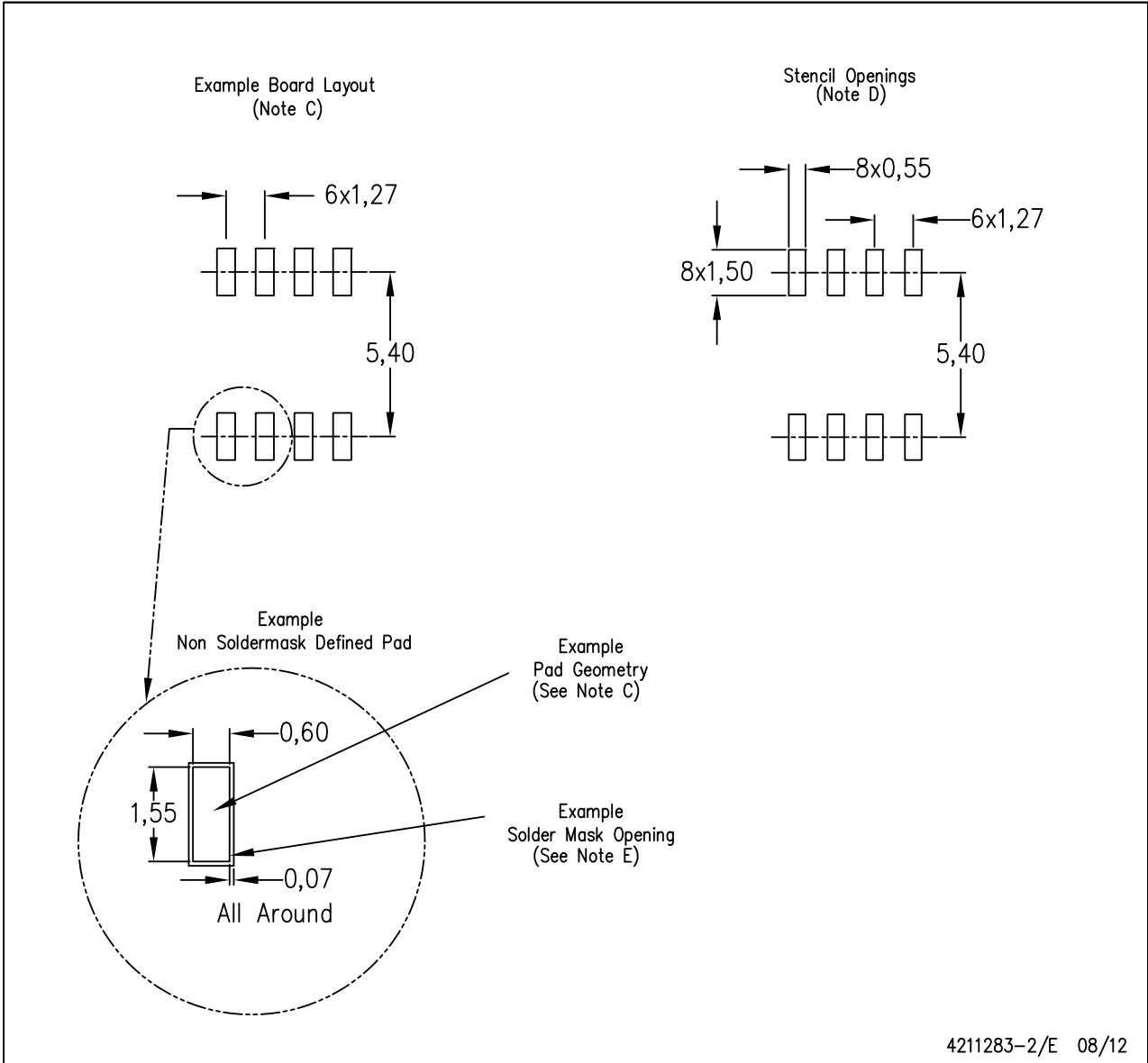D (R−PDSO−G8)   PLASTIC SMALL OUTLINE
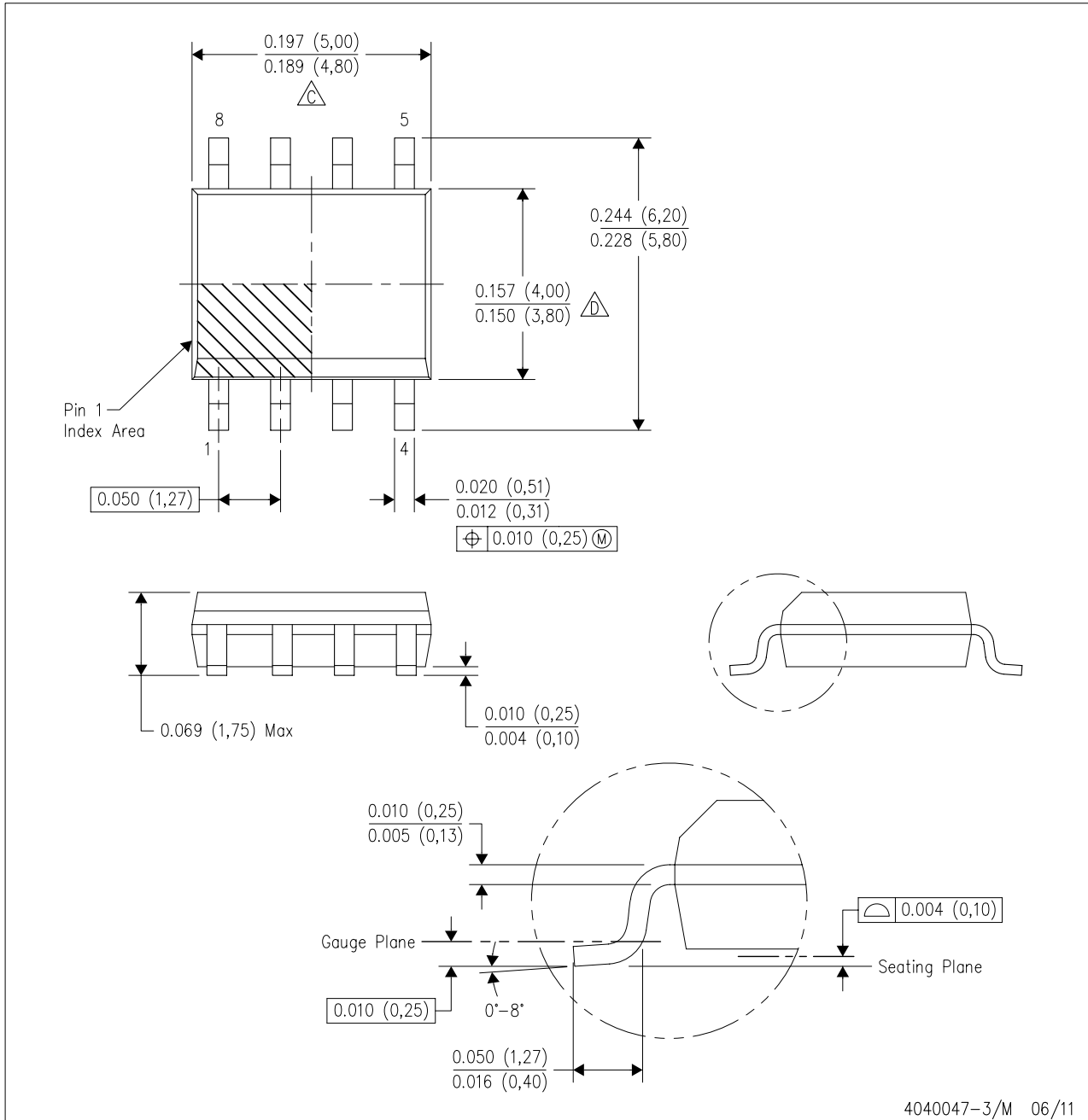
4040047−3/M 06/11

NOTES: A. All linear dimensions are in inches (millimeters).
             B. This drawing is subject to change without notice.
          C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
          D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
             E. Reference JEDEC MS−012 variation AA.

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LAND PATTERN DATA

D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

6x1,27

8x0,55

6x1,27

8x1,50

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

0,60

1,55

0,07

All Around

4211283−2/E 08/12

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate designs.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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