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STG4158BJR

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STG4158

Low-voltage 0.6 Ω typ. single SPDT switch with break-before-make feature and 15 kV ESD protection

Datasheet −**production data**

Features

- Power-off and overvoltage protection
- Wide operating voltage range:
  V_{CC} (opr) = 1.65 to 4.5 V
- Low ON-resistance V_{IN} = 0 V:
  – R_{ON} = 0.85 Ω (max.) at V_{CC} = 4.5 V
- Latch-up performance exceeds 300 mA JESD 17
- ESD performance tested on (D pin)
  – 8 kV IEC-61000-4-2 ESD, contact discharge
  – 15 kV IEC-61000-4-2 ESD, air discharge
- ESD performance test on all other pins
  – 3 kV human body model
  – 200 V machine model (IEC61340-3-2 level M2)
  – 1000 V charge device model (JESD22 C101)

Flip Chip6

Wafer

Description

The STG4158 is a high-speed CMOS low-voltage single analog SPDT (single-pole dual throw) switch or 2:1 multiplexer/demultiplexer switch fabricated in silicon gate C^2MOS technology. Designed to operate from 1.65 to 4.5 V, this device is ideal for portable applications.

It offers low ON-resistance (0.6 Ω) at V_{CC} = 4.5 V (typical T_A = 25 °C). The SEL input threshold is compatible with 1.8 V, and provides control to the switches.
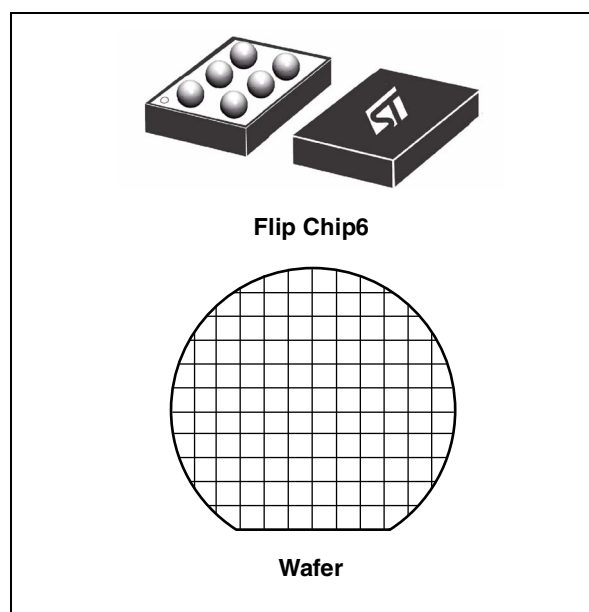
The switch S1 is ON (connected to common port D) when the SEL input is held high and OFF (high-impedance state exists between the two ports) when SEL is held low. The switch S2 is ON (connected to common port D) when the SEL input is held low and OFF (high-impedance state exists between the two ports) when SEL is held high.

The SEL input has an integrated weak pull-down resistor to prevent the SEL signal from floating. For low-power consumption, the SEL input must be grounded.

The STG4158 features power-off and overvoltage protection, enabling the device to be isolated during voltage fault events.

Table 1.   Device summary

Order code	Package	Packing
STG4158BJR	Flip Chip6	Tape and reel
JSTG4158-CD1		Unsawn wafer

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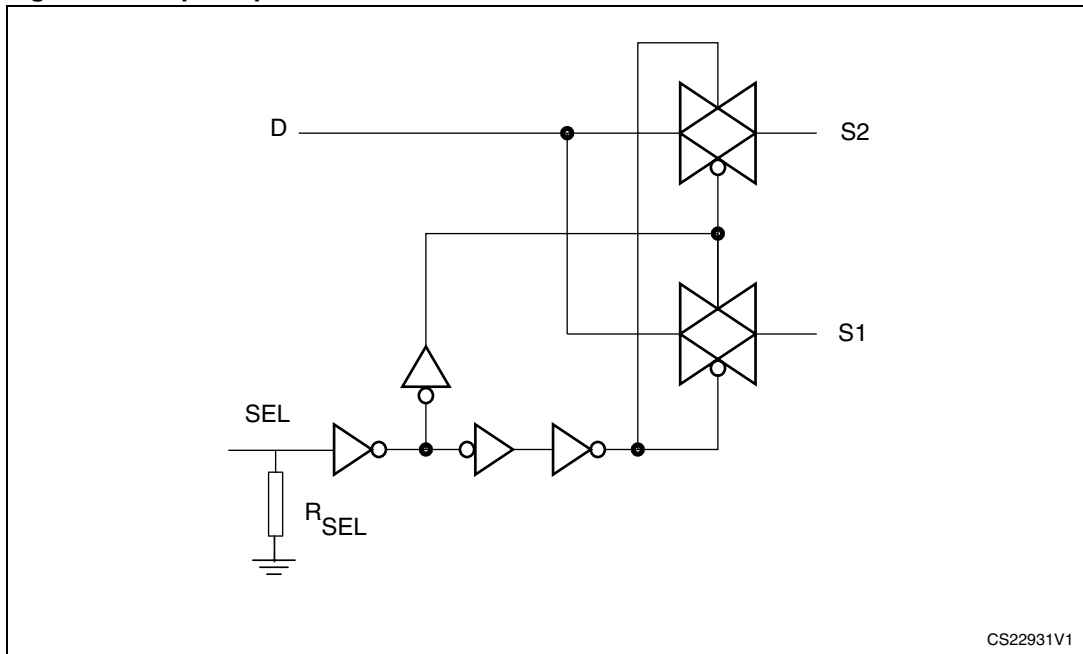
Table 2.   Truth table

SEL	Switch S1	Switch S2
H	ON	OFF[1]
L	OFF[1]	ON

1.   High impedance.

Logic diagram   **STG4158**

Figure 3.   Pin connection (bump side view)

AM00939
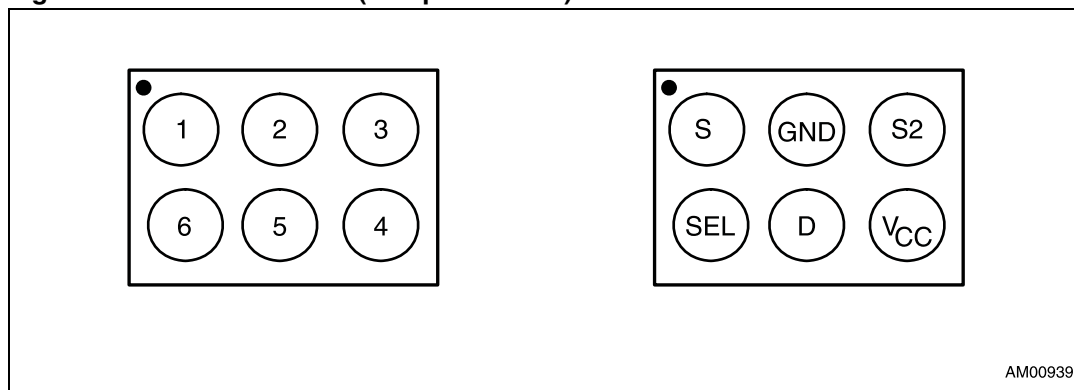
Table 3.   Pin description

Flip Chip	Symbol	Name and function
1, 3	S1, S2	Independent channels
5	D	Common channel
6	SEL	Control
4	V_{CC}	Positive supply voltage
2	GND	Ground (0 V)

2 Maximum rating

Stressing the device above the ratings listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 5: Recommended operating conditions* of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC input diode current on control pin (V_{SEL} < 0 V)	- 50	mA
I_{IK}	DC input diode current (V_{SEL} < 0 V)	± 50	mA
I_{OK}	DC output diode current	± 20	mA
I_O	DC output current	± 300	mA
I_{OP}	DC output current peak (pulse at 1 ms, 10% duty cycle)	± 500	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	± 100	mA
P_D	Power dissipation at T_A = 70 °C[1]	500	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 sec.)	260	°C

1. Derate above 70 °C by 18.5 mW/°C.

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		1.65 to 4.5	V
V_I	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to V_{CC}	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	V_{CC} = 1.65 to 2.7 V	0 to 20	ns/V
		V_{CC} = 3.0 to 4.5 V	0 to 10	

3 Electrical characteristics

Table 6.   DC specifications

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High-level input voltage	1.65 – 1.95		0.9			0.9		V
		2.25 – 2.7		0.9			0.9		
		3.0 – 4.3		1.0			1.0		
		4.5		1.1			1.1		
V_{IL}	Low-level input voltage	1.65 – 1.95				0.6		0.6	V
		2.25 – 2.7				0.6		0.6	
		3.0 – 4.3				0.7		0.7	
		4.5				0.7		0.7	
R_{ON}	ON-resistance	1.65 – 2.20	V_S = 0 V to V_{CC} I_S = 100 mA		2.0			3.0	Ω
		2.25 – 3.6			0.9			1.3	
		3.7 – 4.5			0.6			0.85	
ΔR_{ON}	ON-resistance match between channels	1.65 – 2.20	V_S = 0 V to V_{CC} I_S = 100 mA		40			400	mΩ
		2.25 – 3.6			10			100	
		3.7 – 4.5			10			100	
R_{FLAT}	ON-resistance flatness	1.65 – 2.20	V_S = 0 V to V_{CC} I_S = 100 mA		1.2				Ω
		2.25 – 3.6			0.3			0.6	
		3.7 – 4.5			0.2			0.4	
R_{SEL}	SEL pull-down resistance	1.65 – 4.5			5000				kΩ
I_{OFF}	Sn OFF state leakage current	1.65 – 4.5	V_S = 0, V_D = V_{CC} V_S = V_{CC}, V_D = 0	-30		30	-300	300	nA
I_{ON}	Sn ON state leakage current	1.65 – 4.5	V_S = 0 to V_{CC} V_D = open	-20		20	-200	200	nA

Table 6.   DC specifications (continued)

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
I_D	D ON state leakage current	1.65 – 4.5	V_S = open V_D = 0 to V_{CC}	-30		30	-300	300	nA
		Floating	V_D = 0 - 4.5		10			25	µA
		0 – 0.5	V_D = 0 - 4.5		10			25	µA
		V_{CC} > 0.5	$V_D \geq V_{CC}$ + 0.4		10			25	µA
I_S	S ON state leakage current	1.65 – 4.5	V_S = 0 to V_{CC} V_D = open	-30		30	-300	300	nA
		Floating	V_S = 0 - 4.5		5			15	µA
		0 – 0.5	V_S = 0 - 4.5		5			15	µA
		V_{CC} > 0.5	$V_S \geq V_{CC}$ + 0.4		5			15	µA
I_{CC}	Quiescent supply current	2.5	$V_{SEL} = V_{CC}$		5.6			10	µA
		4.5			9			20	µA
		1.65 – 4.5	V_{SEL} = GND		0.05			0.1	µA
I_{SEL}	SEL leakage current	1.65 – 4.5	V_{SEL} = GND		0.1			1.0	µA
		2.5	$V_{SEL} = V_{CC}$		0.5			1.0	µA
		4.5	$V_{SEL} = V_{CC}$		1.0			2.0	µA
I_{CCLV}	Quiescent supply current low-voltage driving	4.5	V_{SEL} = 1.45 V		8			20	µA

Table 7.   AC electrical characteristics (C$_L$ = 35 pF, R$_L$ = 50 Ω, t$_r$ = t$_f$ $\leq$ 5 ns)

Symbol	Parameter	V$_{CC}$ (V)	Test condition	Value					Unit
				T$_A$ = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t$_{PLH}$, t$_{PHL}$	Propagation delay	1.65 – 1.95			0.13				ns
		2.25 – 2.7			0.15				
		3.0 – 3.6			0.16				
		3.7 – 4.5			0.16				
t$_{ON}$	Turn-on time	1.65 – 1.95	V$_S$ = V$_{CC}$ R$_L$ = 50 Ω C$_L$ = 30 pF		112			160	ns
		2.25 – 2.7			64			86	
		3.0 – 3.6			43			58	
		3.7 – 4.5			28			38	
t$_{OFF}$	Turn-off time	1.65 – 1.95	V$_S$ = V$_{CC}$ R$_L$ = 50 Ω C$_L$ = 30 pF		14			20	ns
		2.25 – 2.7			13			18	
		3.0 – 3.6			13			18	
		3.7 – 4.5			13			18	
t$_D$	Break-before-make time delay	1.65 – 1.95	C$_L$ = 35 pF R$_L$ = 50 Ω V$_S$ = V$_{CC}$/2	10	86				ns
		2.25 – 2.7		10	56				
		3.0 – 3.6		5	31				
		3.7 – 4.5		5	25				
Q	Charge injection	1.65 – 1.95	C$_L$ = 1 nF V$_{GEN}$ = 0 V		70				pC
		2.25 – 2.7			140				
		3.0 – 3.6			190				
		3.7 – -4.5			230				

Table 8.   Analog switch characteristics (C_L = 5 pF, R_L = 50 Ω, T_A = 25 °C)

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
OIRR [1]	OFF-isolation	1.65 – 4.5	V_S = 1 V_{RMS} f = 100 kHz		-76				dB
			V_S = 1 V_{RMS} f = 1 MHz		-55				
			V_S = 1 V_{RMS} f = 5 MHz		-40				
Xtalk	Crosstalk	1.65 – 4.5	V_S = 1 V_{RMS} f = 100 kHz		-81				dB
			V_S = 1 V_{RMS} f = 1 MHz		-61				
			V_S = 1 V_{RMS} f = 5 MHz		-48				
THD	Total harmonic distortion	2.3 – 4.5	R_L = 600 Ω C_L = 50 pF V_S = V_{CC} V_{PP} f = 600 Hz to 20 kHz		0.015				%
BW	-3 dB bandwidth (switch ON)	1.65 – 4.5	R_L = 50 Ω		40				MHz
C_{SEL}	Control pin input capacitance	1.8 – 4.5	V_L = V_{CC}		30				pF
C_{Sn}	Sn port capacitance	1.8 – 4.5	V_L = V_{CC}		80				
C_D	D port capacitance when switch is enabled	1.8 – 4.5	V_L = V_{CC}		190				

1.   OFF-isolation = 20 $\log_{10}$ (V_D/V_S), V_D = output, V_S = input to OFF switch.

4   Application information

Power-off and overvoltage protection

The STG4158 has two operation modes:

1.   Normal operation mode
2.   Isolation mode

In normal operation mode, the switch functions as a normal SPDT, with the SEL pin that selects the switch to be either ON or OFF. Either S1 or S2 is connected to common channel D.

In isolation mode, all the switches are OFF. S1 or S2 are isolated from common channel D. The S1, S2, D ports have a 1 MΩ impedance to ground.

The operation modes are made possible by special detection circuitry that detects the voltage level at D, S1 and S2 supplies. Depending on these voltage levels, the device goes into isolation mode or normal operation mode accordingly.

Isolation mode is a feature of the device that is useful during fault conditions that occur in the application environment.

Table 9.   Voltage conditions

V_{CC}	$V_{D,S}$ (voltage at common port D, S1 or S2)	Voltage condition	Mode
Floating	0 – 4.5 V	All switches OFF - S1, S2 and D are isolated from each other.	Isolation
0 – 0.5 V	0 – 4.5 V	All switches OFF - S1, S2 and D are isolated from each other.	Isolation
$V_{CC} > 0.5$	$V_{D,S} > V_{CC} + 0.4$	All switches OFF - S1, S2 and D are isolated from each other.	Isolation
1.65 – 4.5 V	$0 - V_{CC}$	Either S1 or S2 is connected to D, depending on SEL input.	Normal

Figure 4.   Voltage conditions
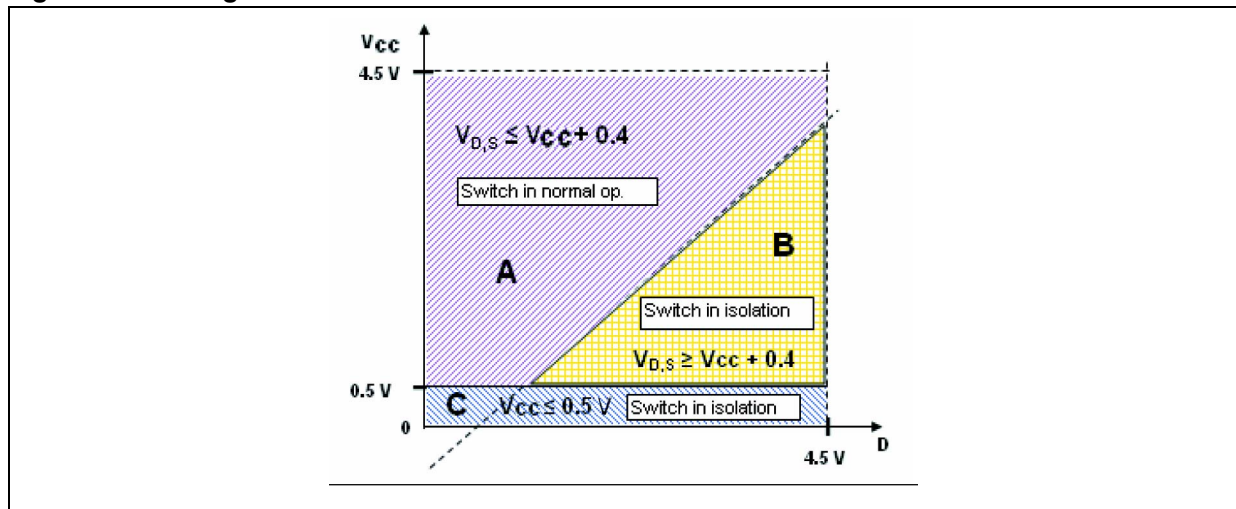
The SEL input has an integrated weak pull-down resistor R_{SEL} to prevent the SEL signal from floating. For lower power consumption, the SEL input must be grounded.

5   Test circuits

Figure 5.   ON-resistance

CS14071V1

Figure 6.   Bandwidth

CS00371V1
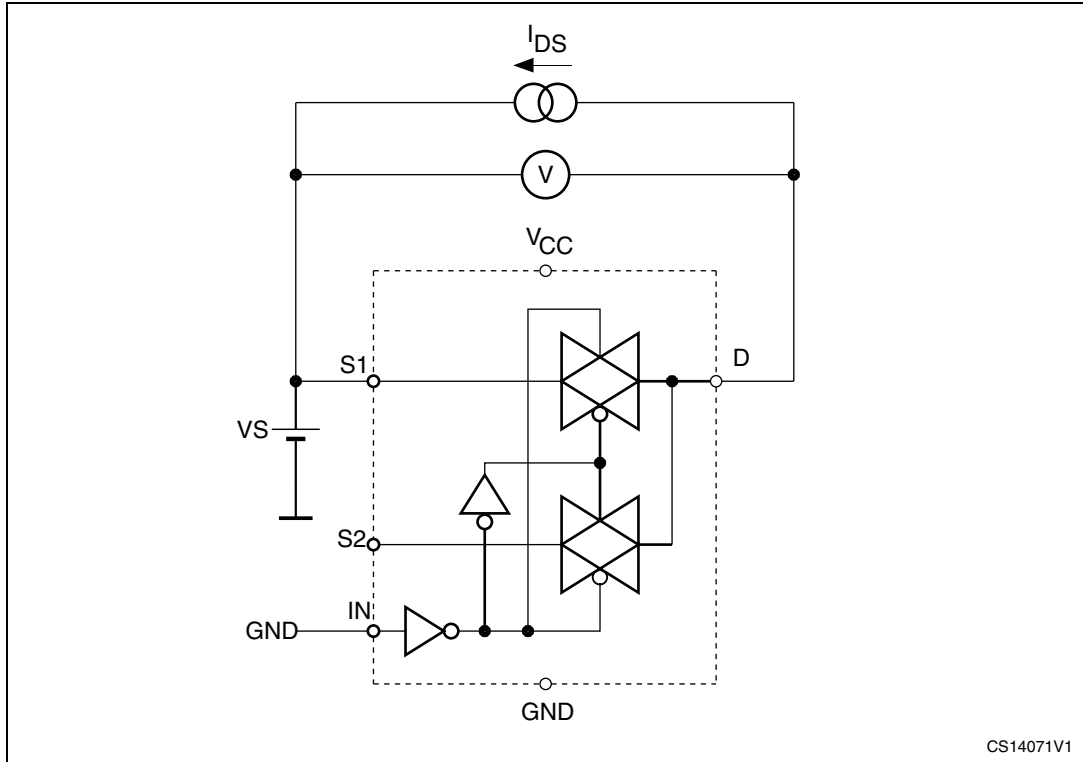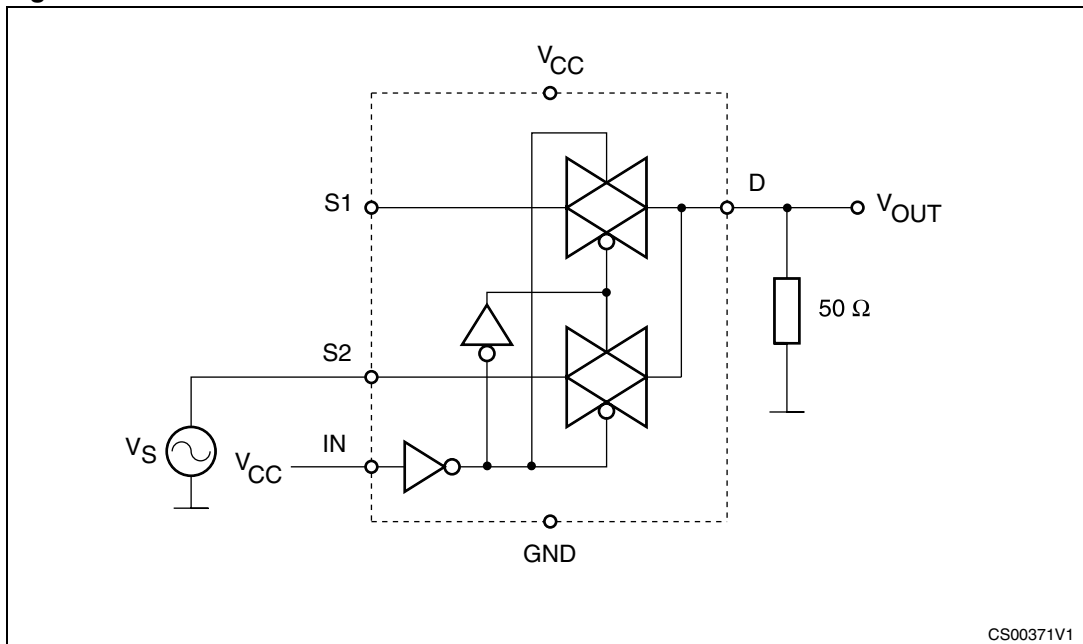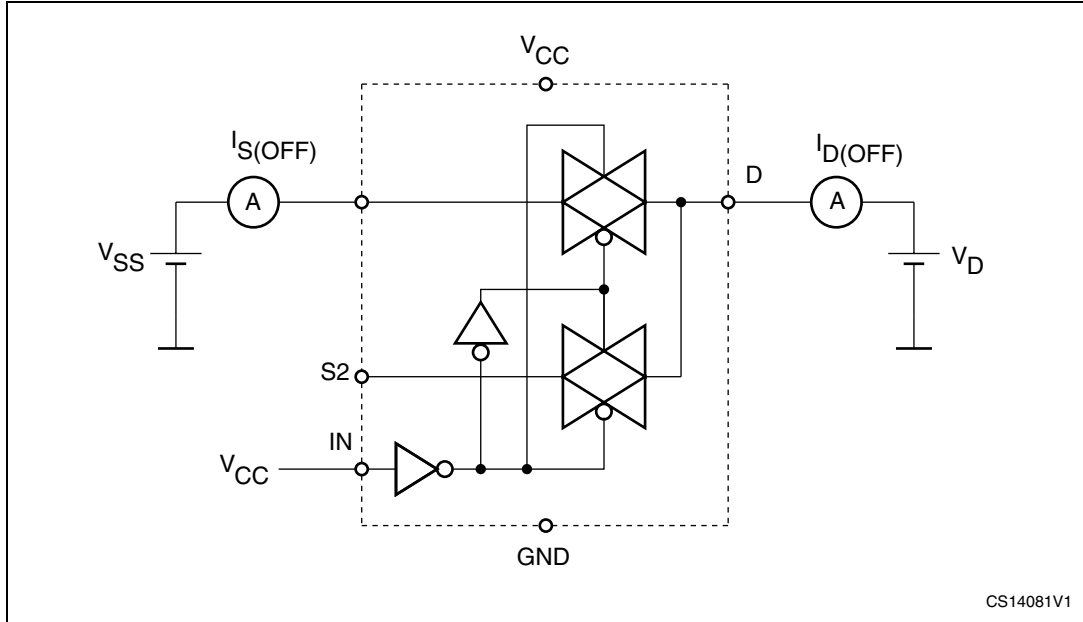
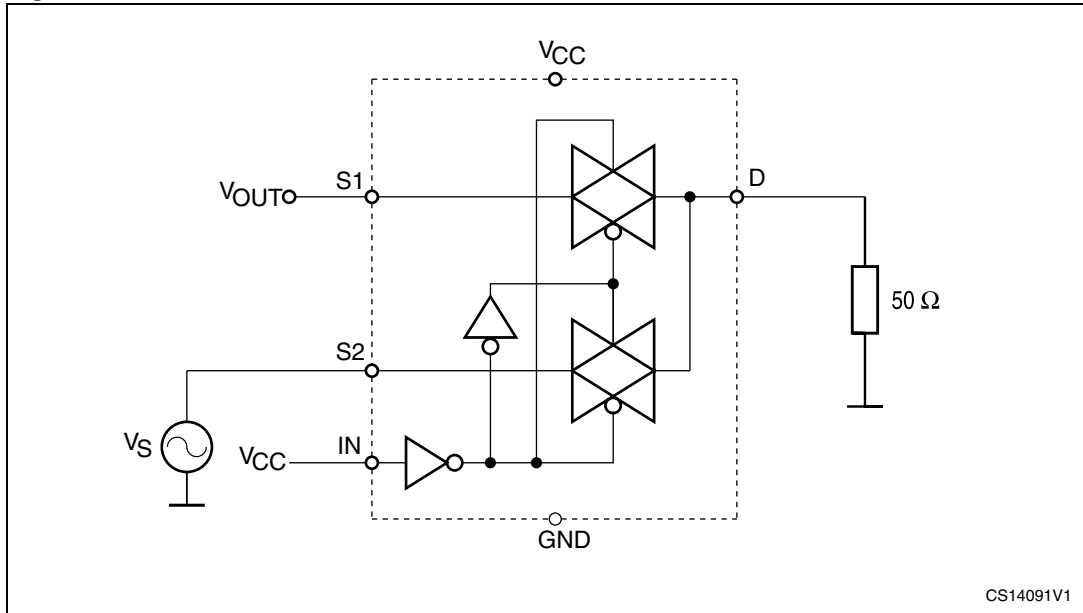**Test circuits**   **STG4158**

Figure 7.   OFF leakage
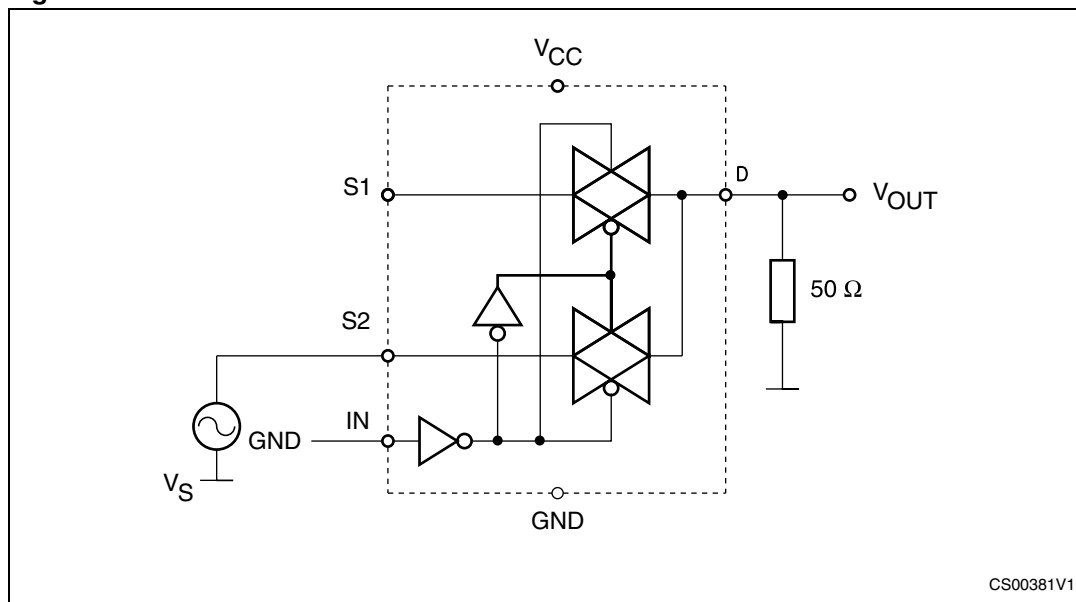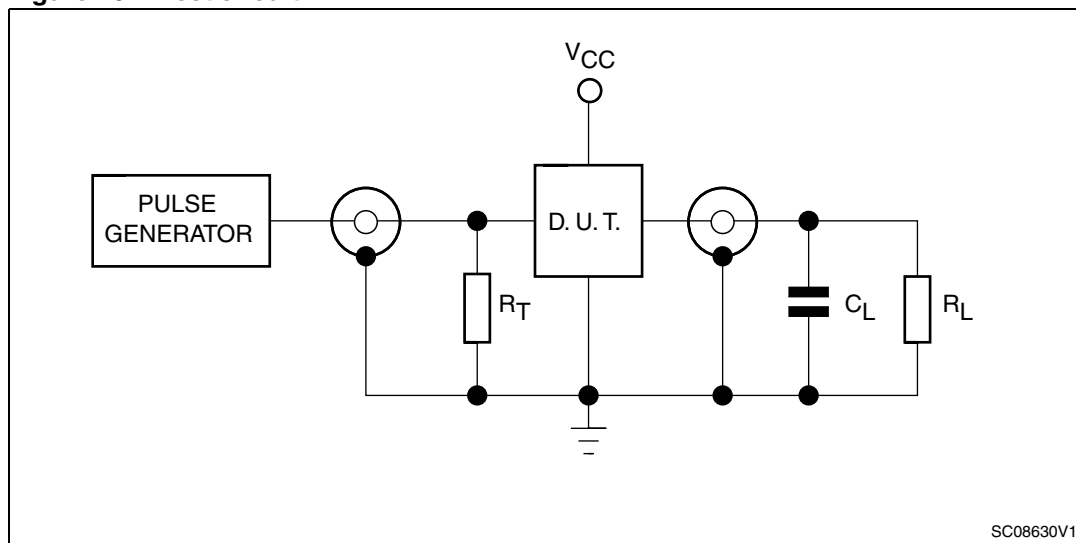

CS14081V1

Figure 8.   Channel-to-channel crosstalk

CS14091V1

Figure 9.   OFF isolation

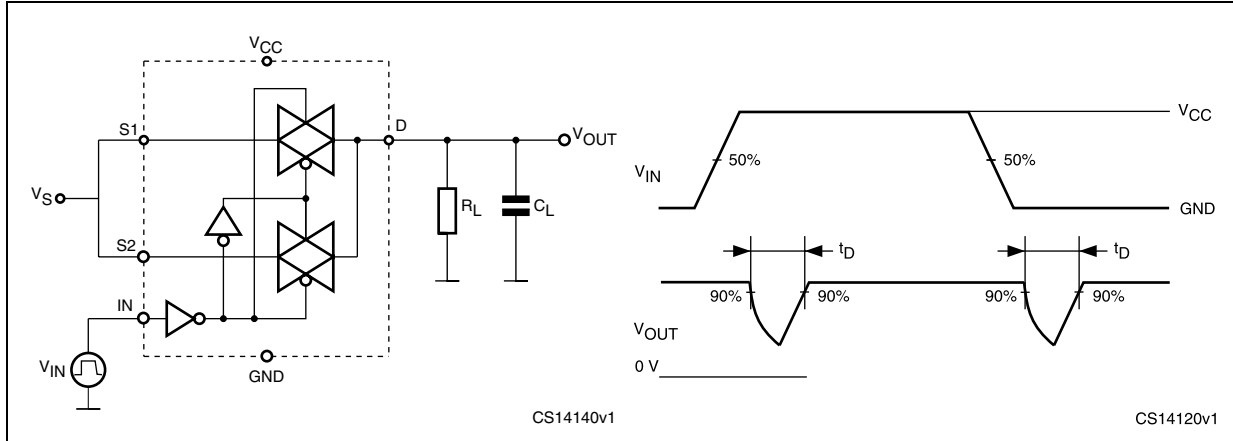CS00381V1

Figure 10.   Test circuit

SC08630V1

1. C_L = 5/35 pF or equivalent: (includes jig capacitance).

2. R_L = 50 Ω or equivalent.

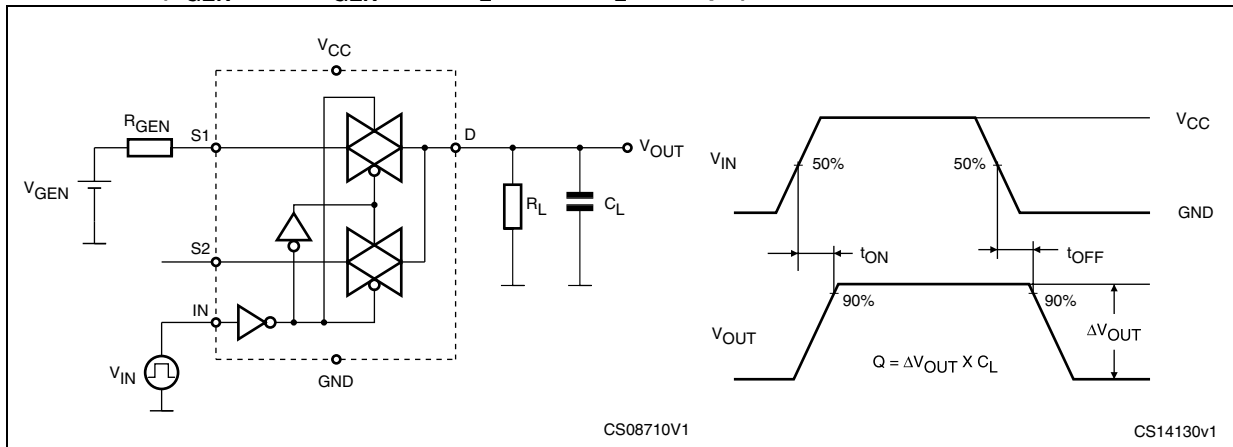3. R_T = Z_{OUT} of pulse generator (typically 50 Ω).

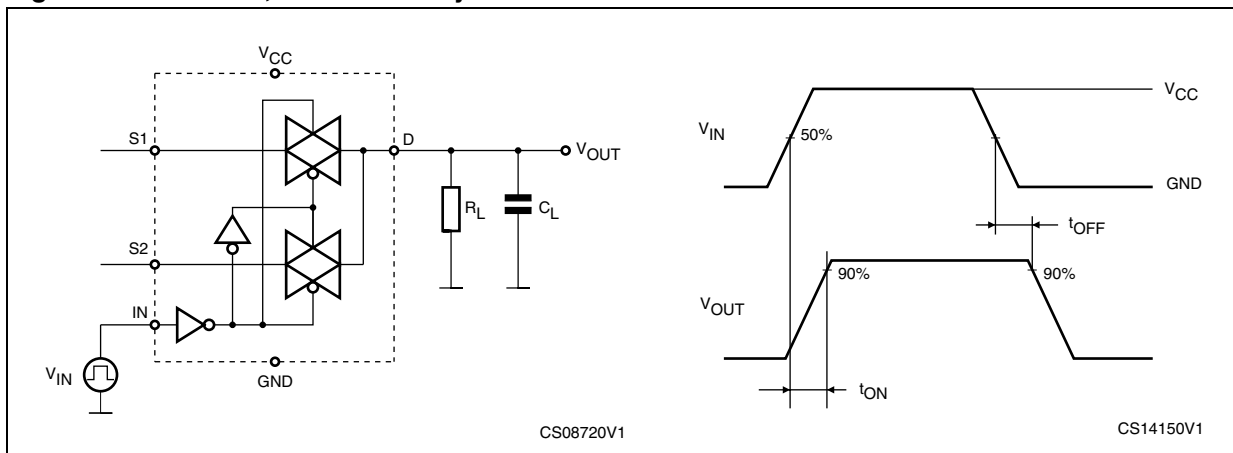### Figure 11. Break-before-make time delay

Figure 12. Switching time and charge injection
### (V_{GEN} = 0 V, R_{GEN} = 0 Ω, R_L = 1 MΩ, C_L = 100 pF)

Figure 13. Turn-ON, turn-OFF delay time

6   Package mechanical data

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Figure 14.   Flip Chip6 package outline

7504896_JV1
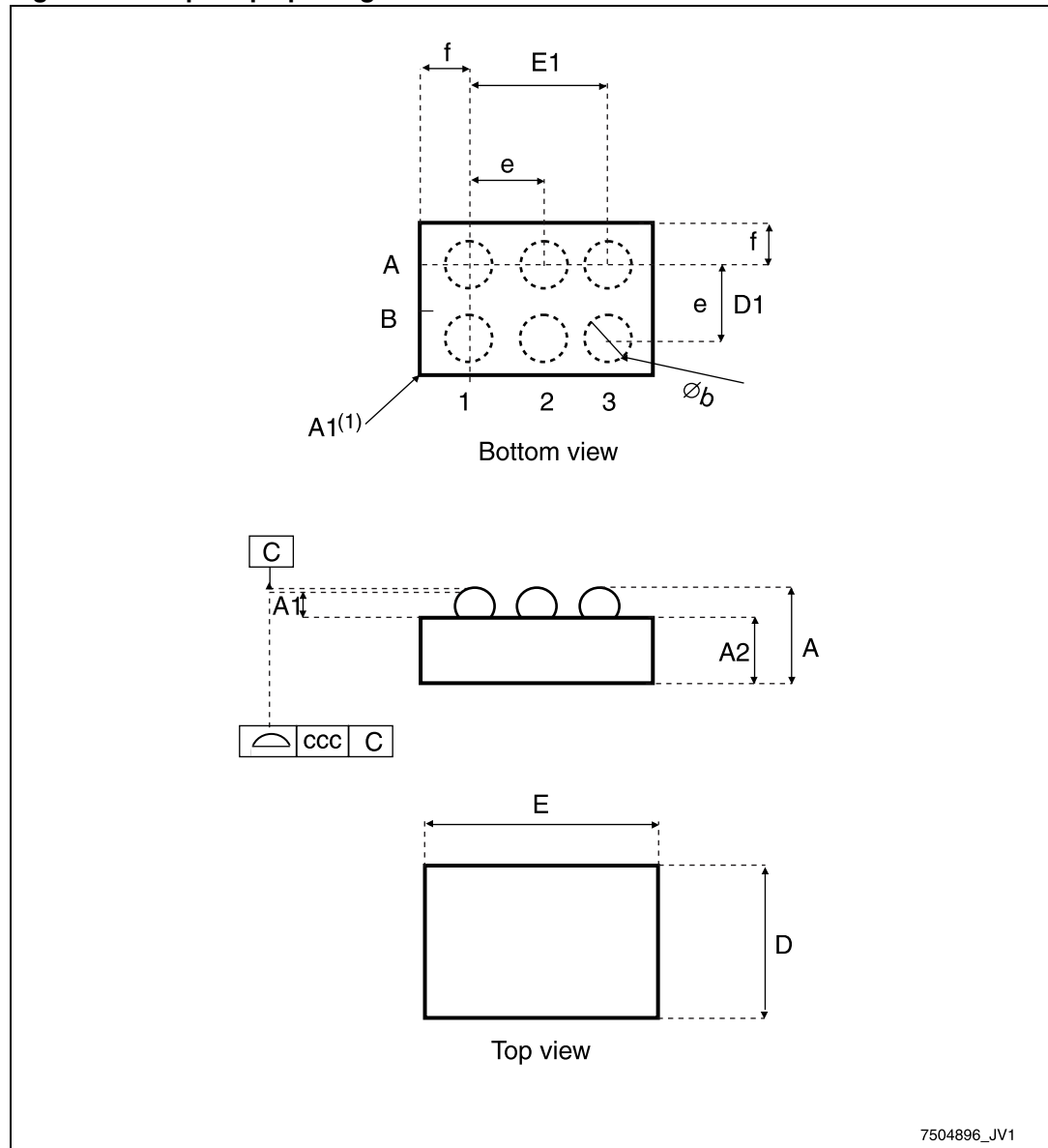
1.   The terminal pin 1 on the bumps side is identified by a distinguishing feature (for instance by a circular "clear area" - typically 0.1 mm diameter). The terminal pin 1 on the backside of the product is identified by a distinguishing feature (for instance by a circular "dot" - typically 0.5 mm diameter).
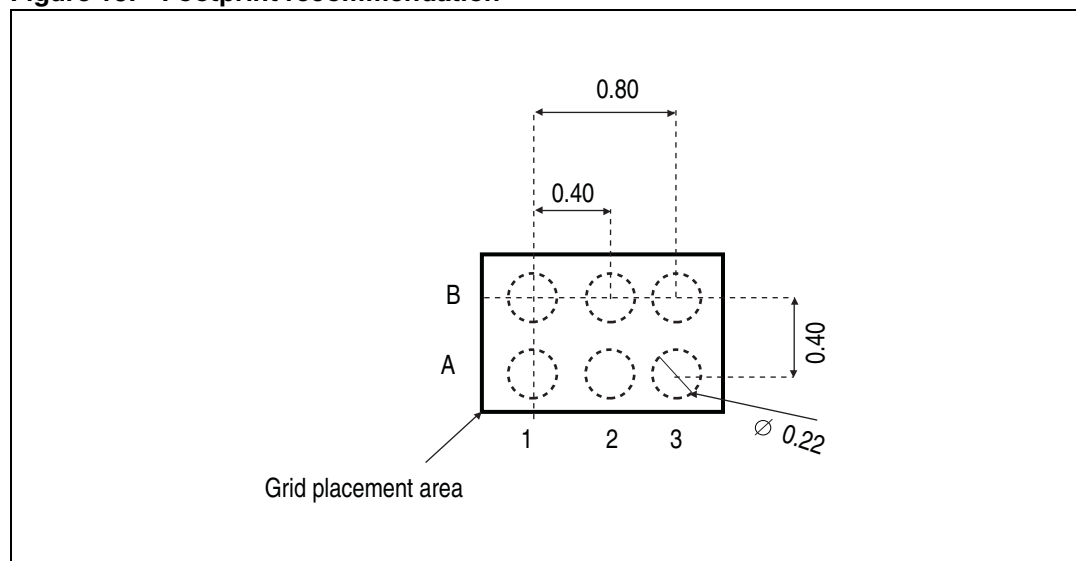
2.   Drawing not to scale.

Package mechanical data   **STG4158**

Table 10.   Flip Chip6 mechanical data

Symbol	Dimensions (mm.)		
	Min.	Typ.	Max.
A	0.545	0.6	0.655
A1	0.17	0.2	0.23
A2	0.375	0.4	0.425
b	0.23	0.255	0.28
D	0.813	0.828	0.843
D1	0.39	0.4	0.41
E	1.213	1.228	1.243
E1	0.79	0.8	0.81
e	0.36	0.4	0.44
f	0.204	0.214	0.224
ccc		0.05	

Figure 15.   Footprint recommendation

Figure 16.   Flip Chip6 marking
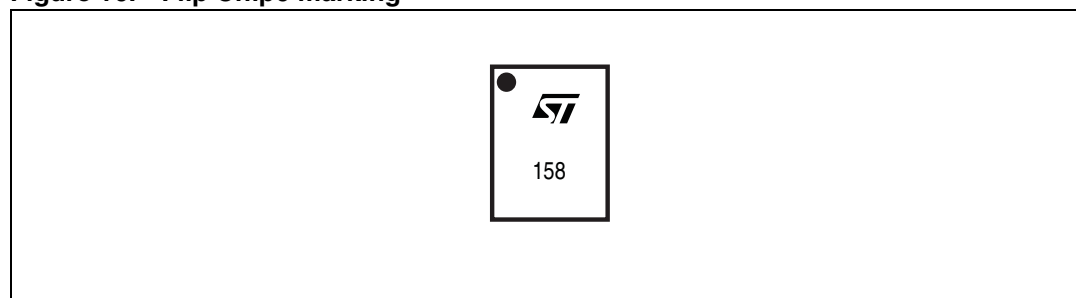
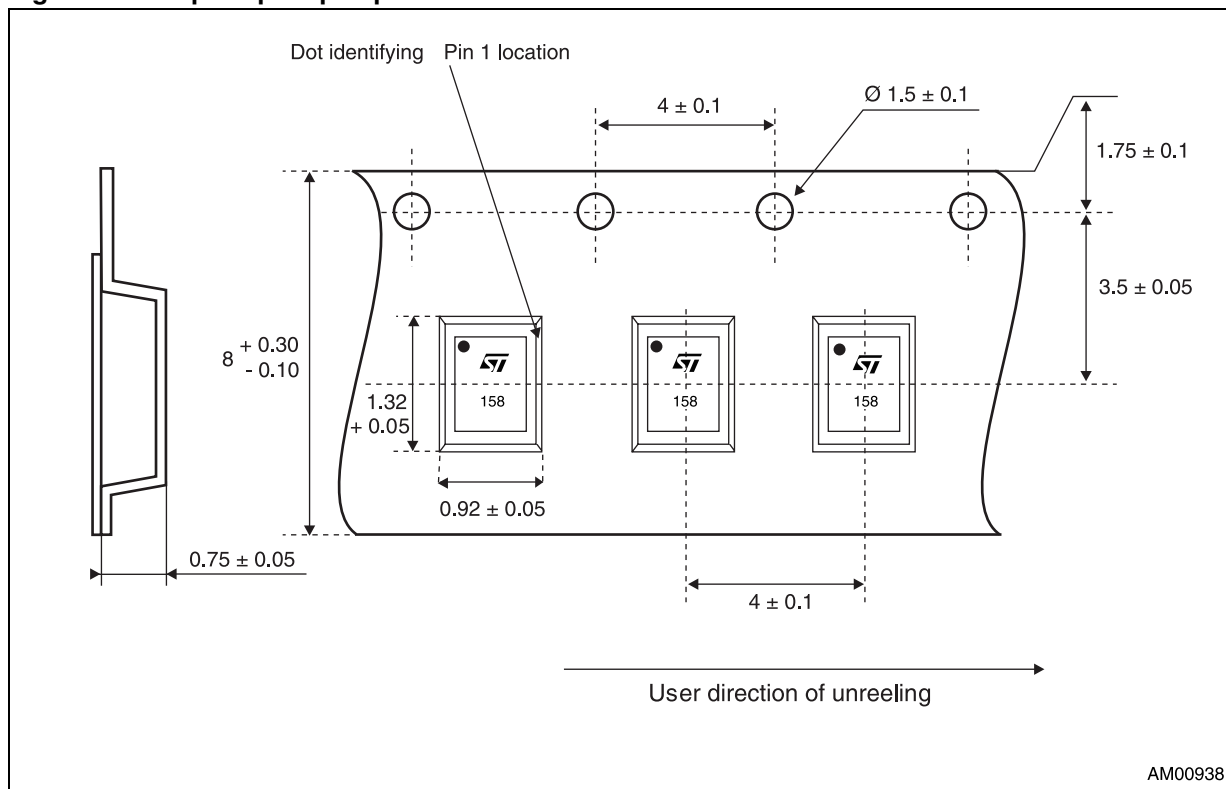**STG4158**   **Package mechanical data**
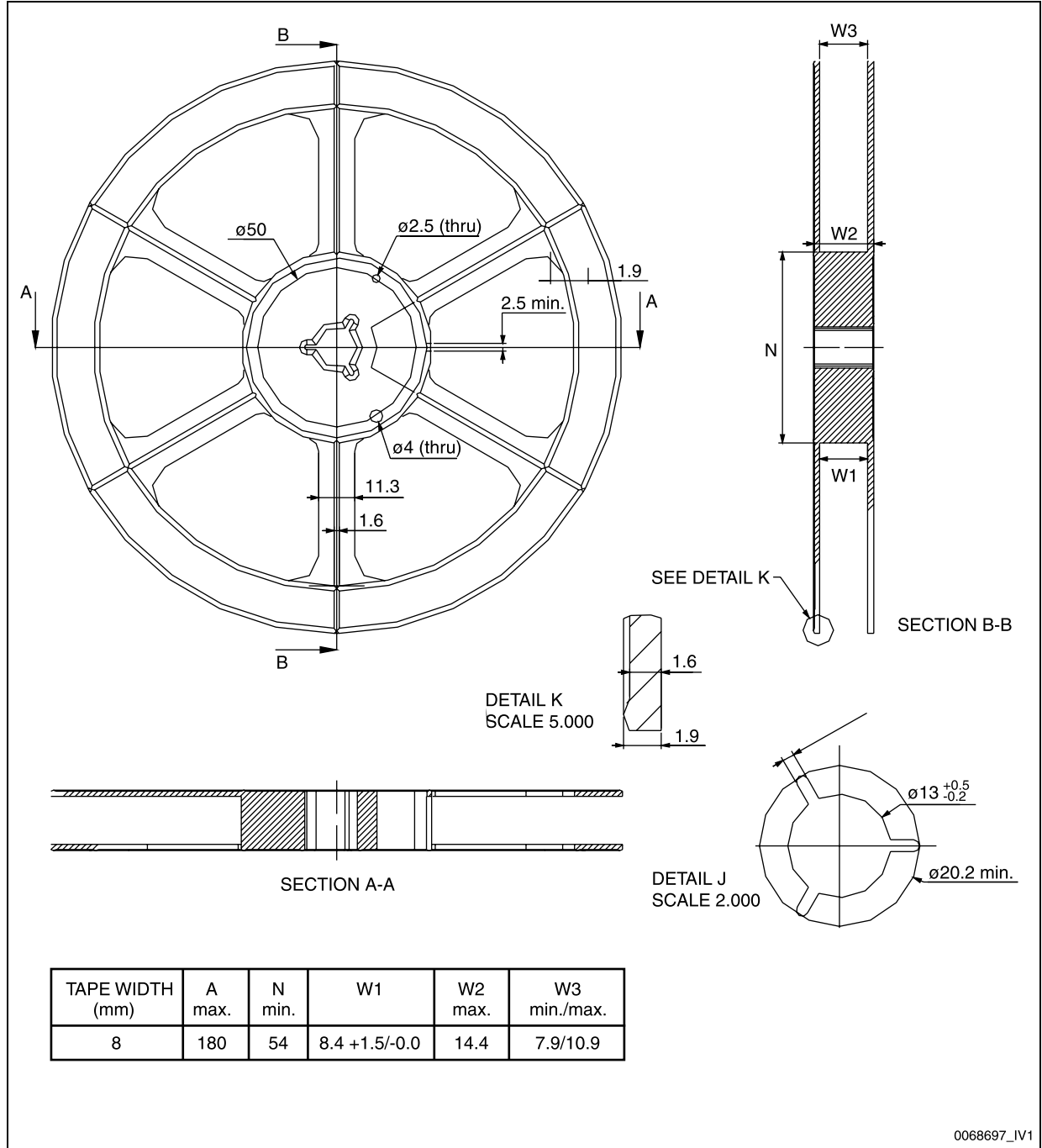
Figure 17.   Flip Chip6 tape specification

1.   All dimensions in mm.

Figure 18.   Flip Chip6 reel information

1.   Material properties:
     1) Antistatic (white or blue).
     2) Conductive (black).

7   Die description

Product JSTG4158-CD1

● Wafer size: 203 mm (8 inches)
● Wafer thickness: 725 µm + 20 µm
● Die identification: UP98A.

Die layout

● Design die size (X x Y): 1128 x 728 µm
● Scribe line: 100 x 100 µm
● Stepping die size: 1228 x 828 µm
● Pad opening: 184 x 184 µm
● DI: die identification (at the position shown in *Figure 19*)
● Pads: pad contact (at the position shown in *Figure 19* and *Table 11*).

Figure 19.   JSTG4158-CD1 die plot
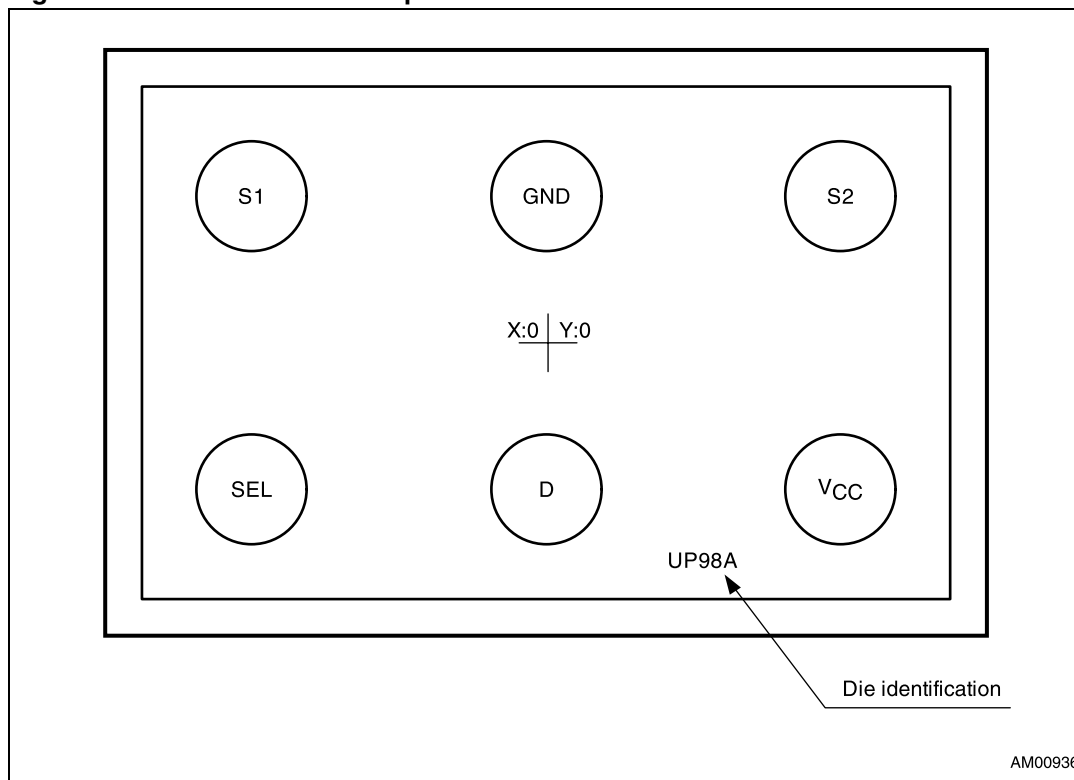
Refer to *Table 11* for the pad locations.

Table 11.   Pad information

Pad function	X (µm)	Y(µm)
S1	-400	200
GND	0	200
S2	400	200
V_{CC}	400	-200
D	0	-200
SEL	-400	-200

Pad locations are measured relative to the die center (where X and Y are the horizontal and vertical axis, respectively, measured in µm). Refer to *Figure 19*.

8   Revision history

Table 12.   Document revision history

Date	Revision	Changes
12-Nov-2007	1	Initial release
24-Apr-2012	2	Added wafer JSTG4158-CD1, *Section 7: Die description*, updated *Table 1*, *Section 2: Maximum rating*, ECOPACK®, *Figure 17*, *Figure 18* and Disclaimer, minor text corrections throughout document.

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