

## Excellent Integrated System Limited

Stocking Distributor

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[Vishay/Siliconix](#)  
[DG441DY-T1-E3](#)

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## Quad SPST CMOS Analog Switches

### DESCRIPTION

The DG441, DG442 monolithic quad analog switches are designed to provide high speed, low error switching of analog and audio signals. The DG441 has a normally closed function. The DG442 has a normally open function. Combining low on-resistance (50 Ω, typ.) with high speed ( $t_{ON}$  150 ns, typ.), the DG441, DG442 are ideally suited for upgrading DG201A/202 sockets. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

To achieve high voltage ratings and superior switching performance, the DG441, DG442 are built on Vishay Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages to the supply levels when off.

### FEATURES

- **Halogen-free according to IEC 61249-2-21 Definition**
- Low on-resistance: 50 Ω
- Low leakage: 80 pA
- Low power consumption: 0.2 mW
- Fast switching action -  $t_{ON}$ : 150 ns
- Low charge injection - Q: - 1 pC
- DG201A/DG202 upgrades
- TTL/CMOS-compatible logic
- Single supply capability
- **Compliant to RoHS Directive 2002/95/EC**



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

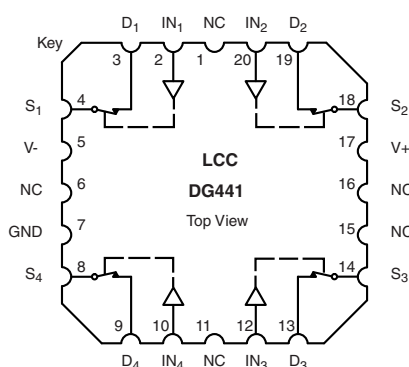
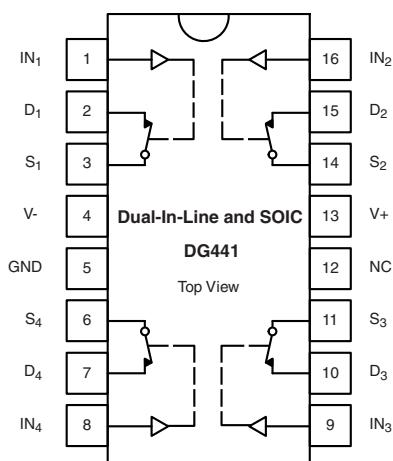
### BENEFITS

- Less signal errors and distortion
- Reduced power supply requirements
- Faster throughput
- Improved reliability
- Reduced pedestal errors
- Simplifies retrofit
- Simple interfacing

### APPLICATIONS

- Audio switching
- Battery powered systems
- Data acquisition
- Hi-Rel systems
- Sample-and-hold circuits
- Communication systems
- Automatic test equipment
- Medical instruments

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



### TRUTH TABLE

Logic	DG441	DG442
0	On	Off
1	Off	On

Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.4 V

# DG441, DG442

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ORDERING INFORMATION		
Temp. Range	Package	Part Number
- 40 °C to 85 °C	16-pin plastic DIP	DG441DJ DG441DJ-E3
		DG442DJ DG442DJ-E3
	16-pin narrow SOIC	DG441DY DG441DY-E3 DG441DY-T1 DG441DY-T1-E3
		DG442DY DG442DY-E3 DG442DY-T1 DG442DY-T1-E3

ABSOLUTE MAXIMUM RATINGS			
Parameter		Limit	Unit
V+ to V-		44	V
GND to V-		25	
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>		(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Continuous Current (any terminal)		30	mA
Current, S or D (pulsed at 1 ms, 10 % duty cycle)		100	
Storage Temperature	(AK suffix)	- 65 to 150	°C
	(DJ, DY suffix)	- 65 to 125	
Power Dissipation (Package) <sup>b</sup>	16-pin plastic DIP <sup>c</sup>	450	mW
	16-pin CerDIP <sup>d</sup>	900	
	16-pin narrow SOIC <sup>d</sup>	900	
	LCC-20 <sup>d</sup>	1200	

Notes:

a. Signals on S<sub>x</sub>, D<sub>x</sub>, or IN<sub>x</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC board.

c. Derate 6 mW/°C above 75 °C.

d. Derate 12 mW/°C above 75 °C.

## SCHEMATIC DIAGRAM Typical Channel

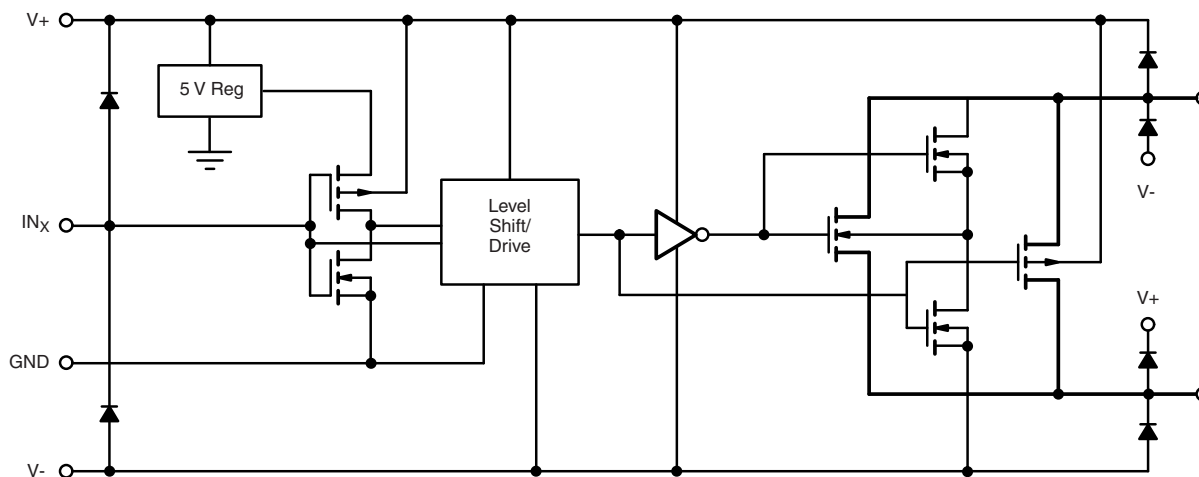


Figure 1.


**DG441, DG442**

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<b>SPECIFICATIONS<sup>a</sup> (Dual Supplies)</b>										
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^f$	Temp. <sup>b</sup>	Typ. <sup>c</sup>	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit	
					Min. <sup>d</sup>	Max. <sup>d</sup>	Min. <sup>d</sup>	Max. <sup>d</sup>		
<b>Analog Switch</b>										
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		- 15	15	- 15	15	V	
Drain-Source On-Resistance	$R_{DS(on)}$	$I_S = -10\text{ mA}$ , $V_D = \pm 8.5\text{ V}$ $V_+ = 13.5\text{ V}$ , $V_- = -13.5\text{ V}$	Room Full	50		85 100		85 100	Ω	
On-Resistance Match Between Channels <sup>e</sup>	$\Delta R_{DS(on)}$	$I_S = -10\text{ mA}$ , $V_D = \pm 10\text{ V}$ $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$	Room Full			4 5		4 5		
Switch Off Leakage Current	$I_{S(off)}$	$V_+ = 16.5\text{ V}$ , $V_- = -16.5\text{ V}$ $V_D = \pm 15.5\text{ V}$ , $V_S = \pm 15.5\text{ V}$	Room Full	$\pm 0.01$	- 0.5 - 20	0.5 20	- 0.5 - 5	0.5 5	nA	
	$I_{D(off)}$		Room Full	$\pm 0.01$	- 0.5 - 20	0.5 20	- 0.5 - 5	0.5 5		
Channel On Leakage Current	$I_{D(on)}$	$V_+ = 16.5\text{ V}$ , $V_- = -16.5\text{ V}$ $V_S = V_D = \pm 15.5\text{ V}$	Room Full	$\pm 0.08$	- 0.5 - 40	0.5 40	- 0.5 - 10	0.5 10		
<b>Digital Control</b>										
Input Current $V_{IN}$ Low	$I_{IL}$	$V_{IN}$ under test = 0.8 V, All Other = 2.4 V	Full	- 0.01	- 500	500	- 500	500	nA	
Input Current $V_{IN}$ High	$I_{IH}$	$V_{IN}$ under test = 2.4 V All Other = 0.8 V	Full	0.01	- 500	500	- 500	500		
<b>Dynamic Characteristics</b>										
Turn-On Time	$t_{ON}$	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$ $V_S = \pm 10\text{ V}$ See Figure 2	Room	150		250		250	ns	
Turn-Off Time			DG441	Room	90		120			120
			DG442	Room	110		210			210
Charge Injection <sup>e</sup>	Q	$C_L = 1\text{ nF}$ , $V_S = 0\text{ V}$ $V_{gen} = 0\text{ V}$ , $R_{gen} = 0\text{ }\Omega$	Room	- 1					pC	
Off Isolation <sup>e</sup>	OIRR	$R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$	Room	60					dB	
Crosstalk (Channel-to-Channel)	$X_{TALK}$		Room	100						
Source Off Capacitance <sup>e</sup>	$C_{S(off)}$	$f = 1\text{ MHz}$	Room	4					pF	
Drain Off Capacitance <sup>e</sup>	$C_{D(off)}$		Room	4						
Channel On Capacitance <sup>e</sup>	$C_{D(on)}$		$V_{ANALOG} = 0\text{ V}$	Room	16					
<b>Power Supplies</b>										
Positive Supply Current	$I_+$	$V_+ = 16.5\text{ V}$ , $V_- = -16.5\text{ V}$ $V_{IN} = 0$ or $5\text{ V}$	Full	15		100		100	μA	
Negative Supply Current	$I_-$		Room	- 0.0001	- 1		- 1			
			Full		- 5		- 5			
Ground Current	$I_{GND}$		Full	- 15	- 100		- 100			

# DG441, DG442

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SPECIFICATIONS <sup>a</sup> (Single Supply)									
Parameter	Symbol	Test Conditions Unless Otherwise Specified V <sub>+</sub> = 12 V, V <sub>-</sub> = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>f</sup>	Temp. <sup>b</sup>	Typ. <sup>c</sup>	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
					Min. <sup>d</sup>	Max. <sup>d</sup>	Min. <sup>d</sup>	Max. <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		0	12	0	12	V
Drain-Source On-Resistance	R <sub>DS(on)</sub>	I <sub>S</sub> = - 10 mA, V <sub>D</sub> = 3 V, 8 V V <sub>+</sub> = 10.8 V	Room Full	100		160 200		160 200	Ω
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF V <sub>S</sub> = 8 V See Figure 2	Room	300		450		450	ns
Turn-Off Time	t <sub>OFF</sub>		Room	60		200		200	
Charge Injection	Q	C <sub>L</sub> = 1nF, V <sub>gen</sub> = 6 V, R <sub>gen</sub> = 0 Ω	Room	2					pC
<b>Power Supplies</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 13.2 V, V <sub>-</sub> = 0 V V <sub>IN</sub> = 0 or 5 V	Full	15		100		100	μA
Negative Supply Current	I <sub>-</sub>		Room	- 0.0001	- 1		- 1		
Ground Current	I <sub>GND</sub>		Full	- 15	- 100		- 100		

Notes:

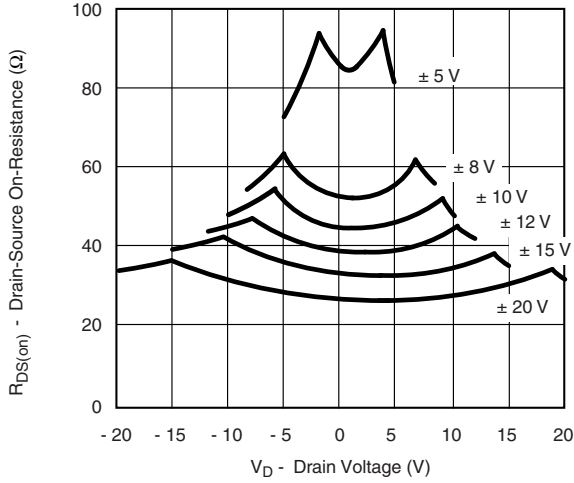
- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- e. Guaranteed by design, not subject to production test.
- f. V<sub>IN</sub> = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

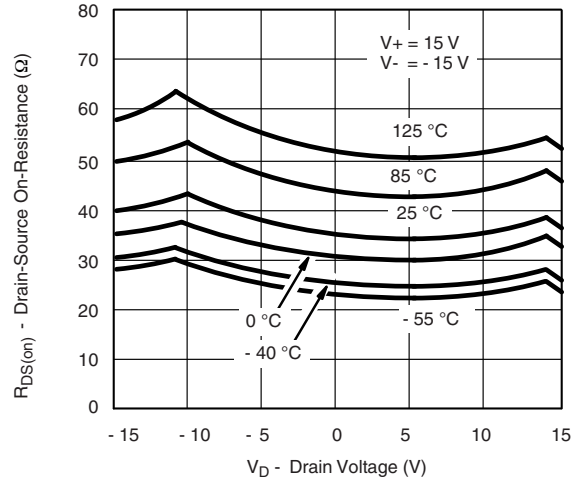


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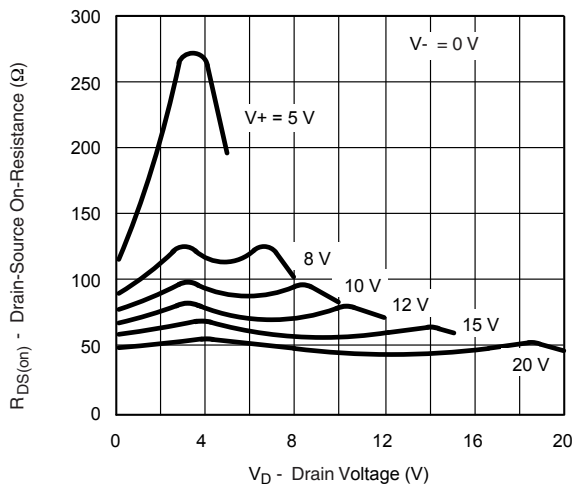
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



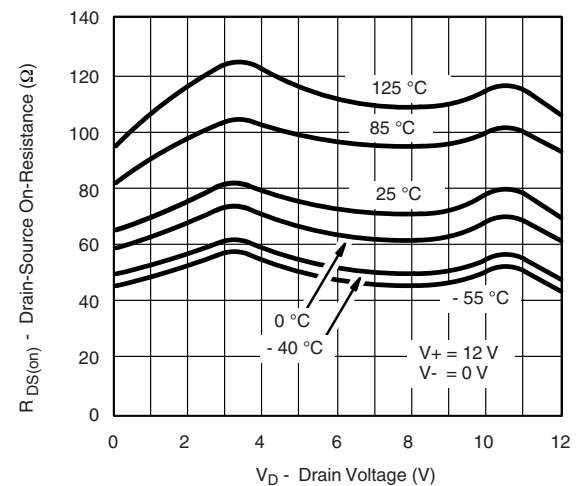
**R<sub>DS(on)</sub> vs. V<sub>D</sub> and Power Supply Voltage**



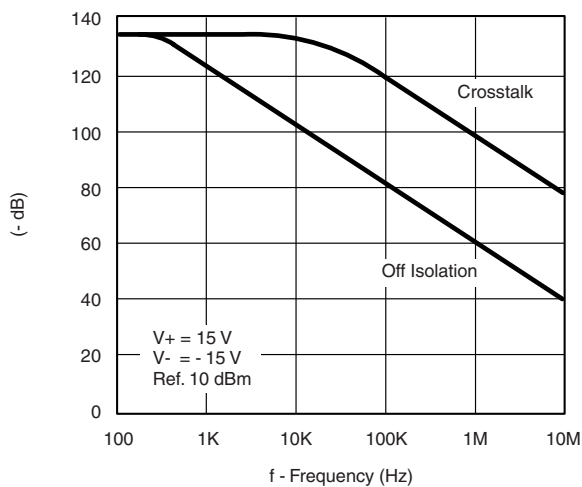
**R<sub>DS(on)</sub> vs. V<sub>D</sub> and Temperature**



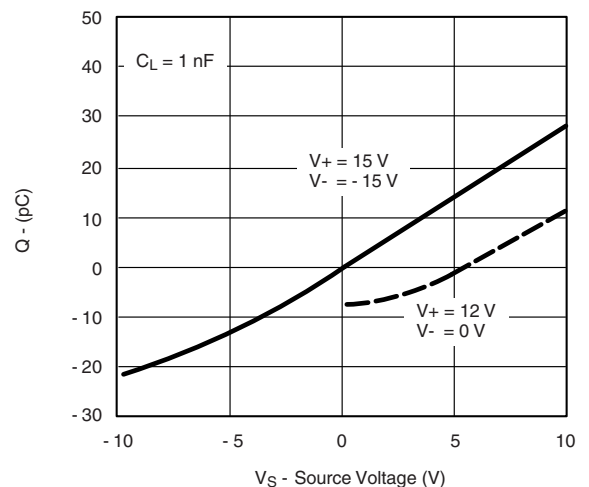
**R<sub>DS(on)</sub> vs. V<sub>D</sub> and Unipolar Power Supply Voltage**



**R<sub>DS(on)</sub> vs. V<sub>D</sub> and Temperature (Single 12-V Supply)**



**Crosstalk and Off Isolation vs. Frequency**



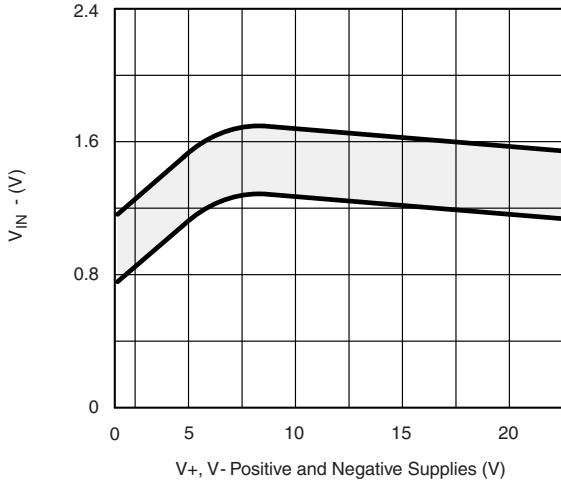
**Charge Injection vs. Source Voltage**

# DG441, DG442

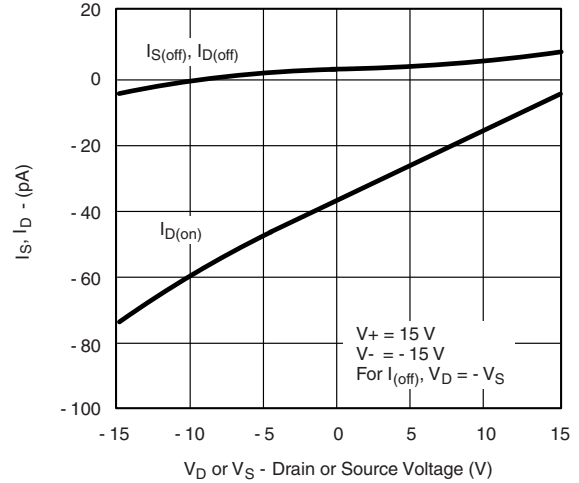
Vishay Siliconix



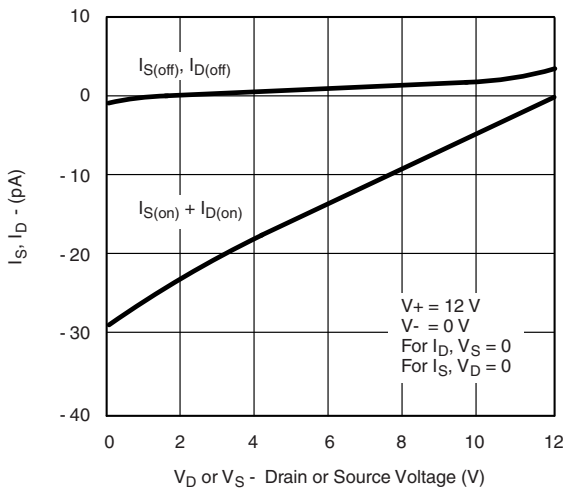
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



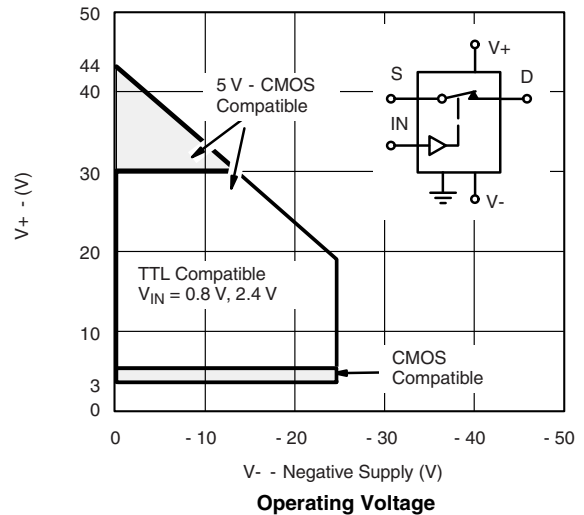
**Switching Threshold vs. Supply Voltage**



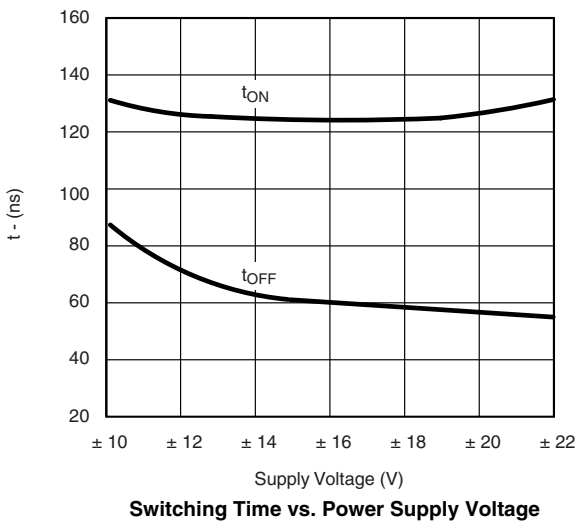
**Source/Drain Leakage Currents**



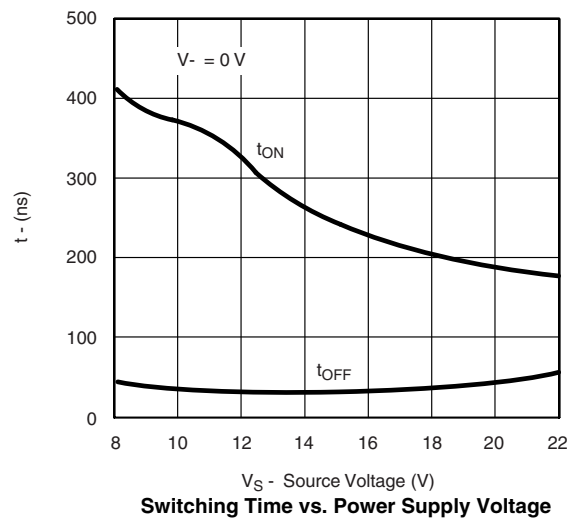
**Source/Drain Leakage Currents (Single 12 V Supply)**



**Operating Voltage**



**Switching Time vs. Power Supply Voltage**

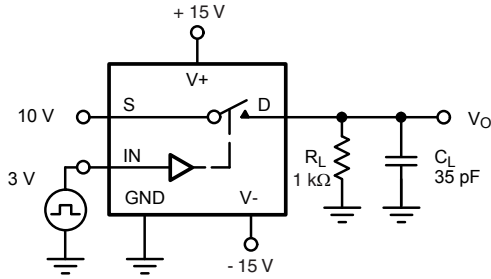


**Switching Time vs. Power Supply Voltage**

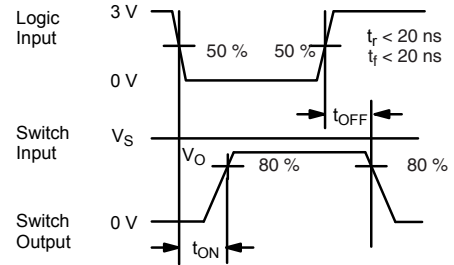


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**TEST CIRCUITS**

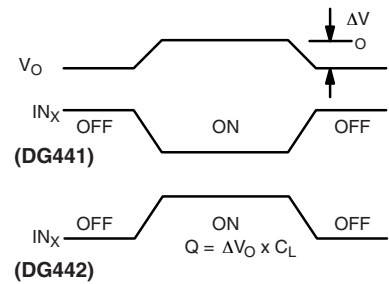
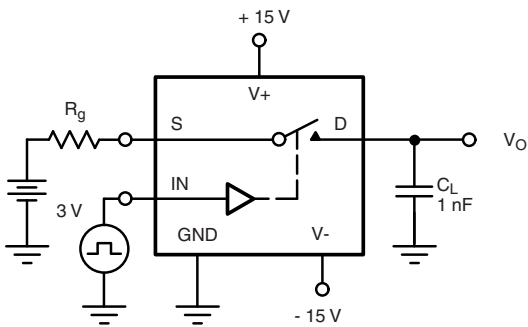


$C_L$  (includes fixture and stray capacitance)



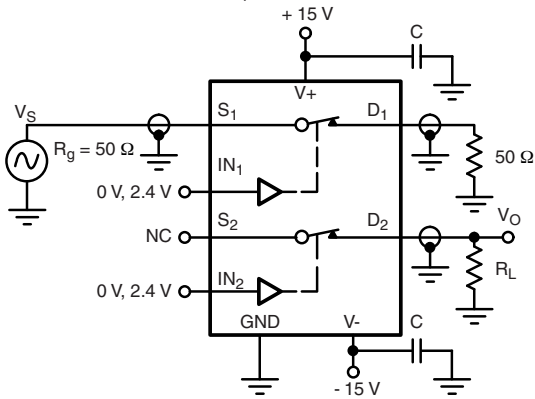
Note: Logic input waveform is inverted for DG442.

**Figure 2. Switching Time**



**Figure 3. Charge Injection**

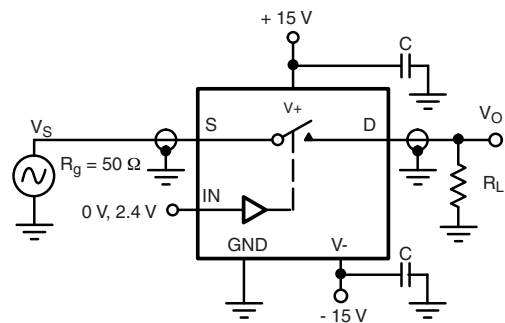
C = 1 mF tantalum in parallel with 0.01 mF ceramic



$$X_{\text{TALK Isolation}} = 20 \log \left| \frac{V_S}{V_O} \right|$$

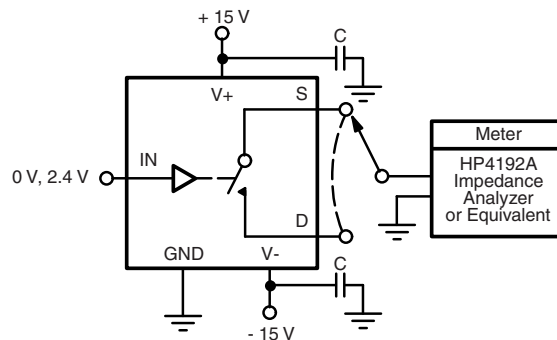
C = RF bypass

**Figure 4. Crosstalk**



$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

**Figure 5. Off Isolation**



**Figure 6. Source/Drain Capacitances**



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## APPLICATIONS

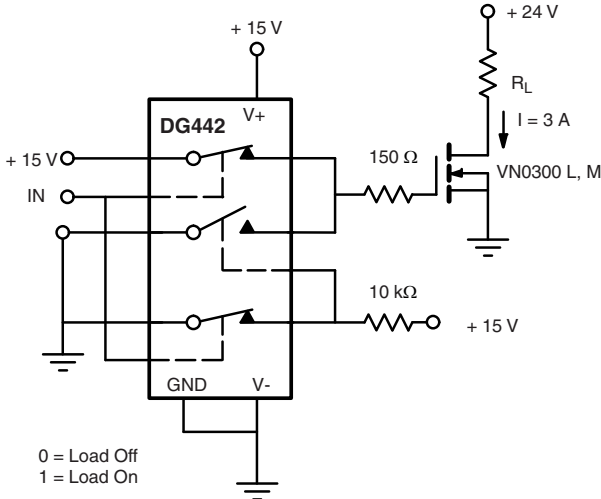


Figure 7. Power MOSFET Driver

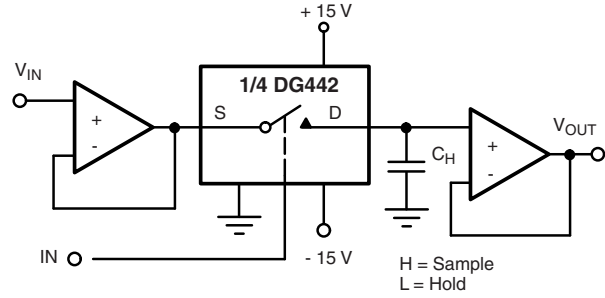


Figure 8. Open Loop Sample-and-Hold

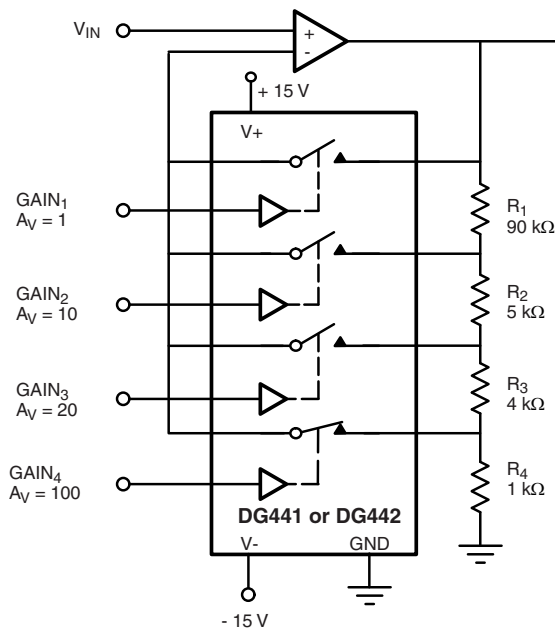


Figure 9. Precision-Weighted Resistor Programmable-Gain Amplifier

Gain error is determined only by the resistor tolerance. Op amp offset and CMRR will limit accuracy of circuit.

With SW<sub>4</sub> Closed

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100$$

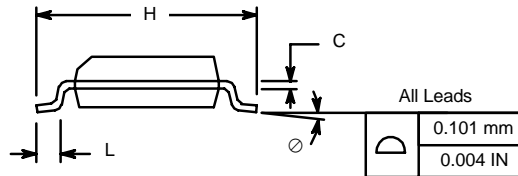
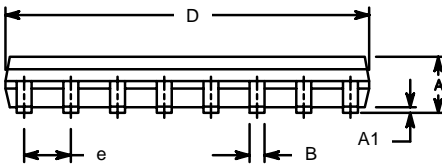
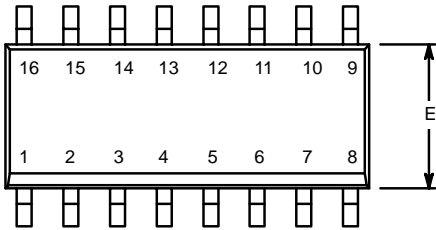
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?70053](http://www.vishay.com/ppg?70053).



## Package Information Vishay Siliconix

### SOIC (NARROW): 16-LEAD

JEDEC Part Number: MS-012



All Leads	
	0.101 mm
	0.004 IN

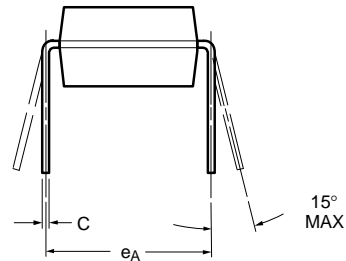
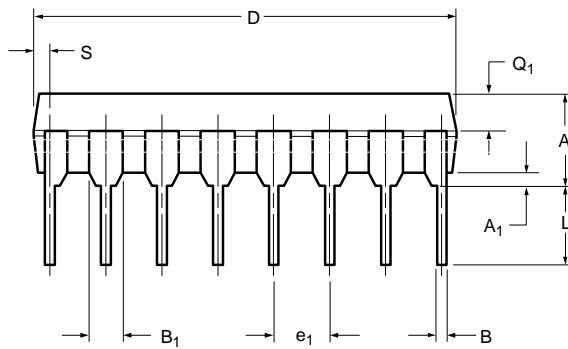
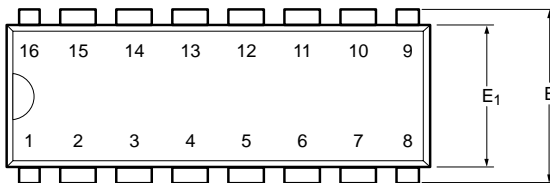
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
∅	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01  
DWG: 5300



**Package Information**  
**Vishay Siliconix**

**PDIP: 16-LEAD**



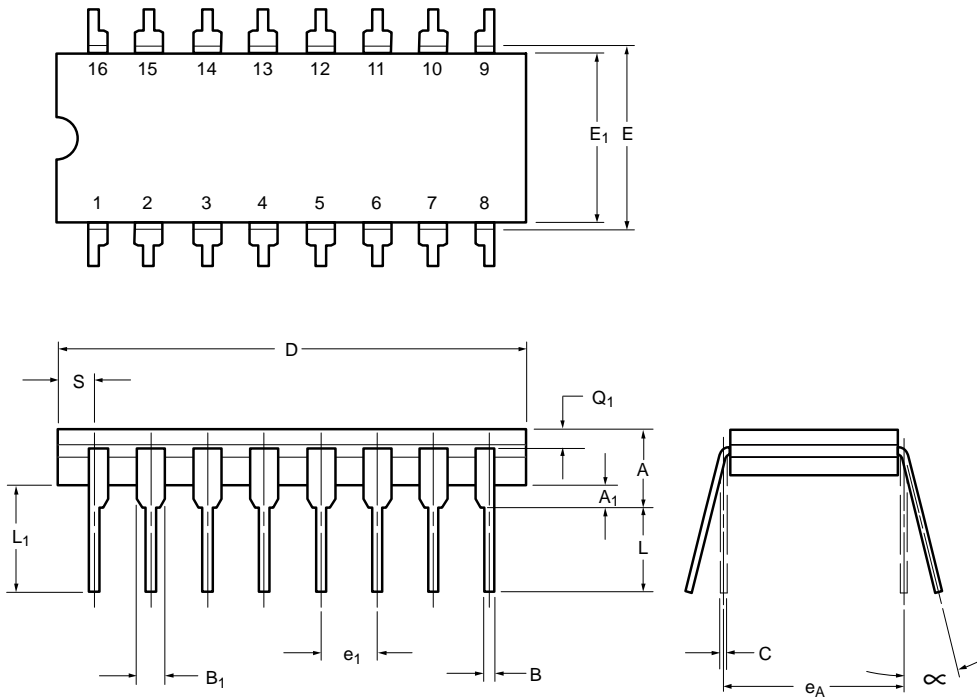
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	3.81	5.08	0.150	0.200
<b>A<sub>1</sub></b>	0.38	1.27	0.015	0.050
<b>B</b>	0.38	0.51	0.015	0.020
<b>B<sub>1</sub></b>	0.89	1.65	0.035	0.065
<b>C</b>	0.20	0.30	0.008	0.012
<b>D</b>	18.93	21.33	0.745	0.840
<b>E</b>	7.62	8.26	0.300	0.325
<b>E<sub>1</sub></b>	5.59	7.11	0.220	0.280
<b>e<sub>1</sub></b>	2.29	2.79	0.090	0.110
<b>e<sub>A</sub></b>	7.37	7.87	0.290	0.310
<b>L</b>	2.79	3.81	0.110	0.150
<b>Q<sub>1</sub></b>	1.27	2.03	0.050	0.080
<b>S</b>	0.38	1.52	.015	0.060

ECN: S-03946—Rev. D, 09-Jul-01  
DWG: 5482



**Package Information**  
**Vishay Siliconix**

**CERDIP: 16-LEAD**



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A <sub>1</sub>	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B <sub>1</sub>	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	19.05	19.56	0.750	0.770
E	7.62	8.26	0.300	0.325
E <sub>1</sub>	6.60	7.62	0.260	0.300
e <sub>1</sub>	2.54 BSC		0.100 BSC	
e <sub>A</sub>	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L <sub>1</sub>	3.81	5.08	0.150	0.200
Q <sub>1</sub>	1.27	2.16	0.050	0.085
S	0.38	1.14	0.015	0.045
α	0°	15°	0°	15°

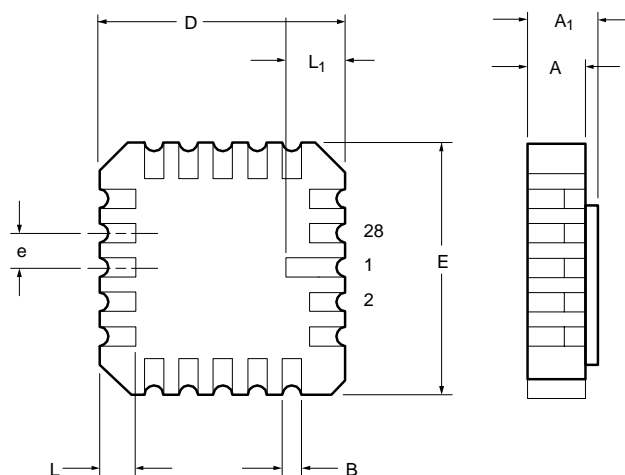
ECN: S-03946—Rev. G, 09-Jul-01  
 DWG: 5403



## Packaging Information

### Vishay Siliconix

#### 20-LEAD LCC



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	1.37	2.24	0.054	0.088
<b>A<sub>1</sub></b>	1.63	2.54	0.064	0.100
<b>B</b>	0.56	0.71	0.022	0.028
<b>D</b>	8.69	9.09	0.342	0.358
<b>E</b>	8.69	9.09	0.442	0.358
<b>e</b>	1.27 BSC		0.050 BSC	
<b>L</b>	1.14	1.40	0.045	0.055
<b>L<sub>1</sub></b>	1.96	2.36	0.077	0.093

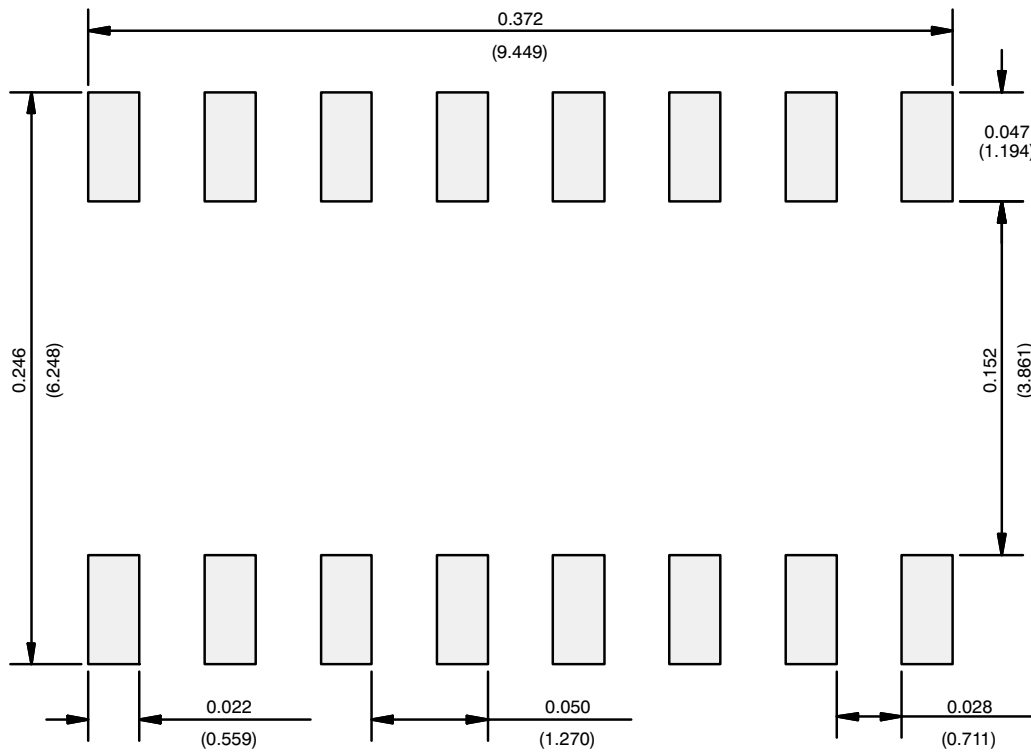
ECN: S-03946—Rev. B, 09-Jul-01  
 DWG: 5321

# Application Note 826

Vishay Siliconix



## RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads  
 Dimensions in Inches/(mm)

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APPLICATION NOTE



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