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Si9910 Adaptive Power MOSFET Driver Improves Performance in High-Voltage Half-Bridge Applications

The Si9910 is the first of a new generation of "adaptive" power MOSFET gate drivers. These adaptive drivers provide protection for the power MOSFET switching element while allowing direct control of high-voltage switching from logic signals. To achieve this protection, the Si9910 monitors the power MOSFET's operating conditions through feedback loops and alters its output characteristics.

The Si9910 adaptive driver allows the system designer to take full advantage of the increased performance and efficiency of power MOSFETs. Previous gate-drive techniques required designing a system for safe operation under worst-case conditions, even those which occur infrequently. Thus, these systems operated most of the time under less than optimum conditions with considerable performance and efficiency penalties. The Si9910, however, prevents power MOSFET destruction under worst-case operating conditions without compromising system performance and efficiency during normal operation.

SI9910 CIRCUIT DESCRIPTION

The Si9910 is a single-channel, non-inverting CMOS driver with a low-impedance, emitter-follower output and a Schmidt trigger input (see Figure 1). To take full advantage of the efficiency offered by the power MOSFET's capacitive input impedance characteristic, the Si9910 was designed to have extremely low quiescent current and low output gate-drive impedance.

A "power IC" process incorporating CMOS, DMOS, and bipolar device technologies are employed to optimize the Si9910 driver characteristics. The driver's CMOS logic section requires a maximum quiescent current of 1 µA (with the output high and the power MOSFET turned on), while the emitter-follower output stage is capable of delivering 1 A of peak current to quickly charge and discharge MOSFET gate capacitance. Using a bipolar emitter-follower output eliminates shoot-through and quiescent bias current losses in the low-impedance output stage.

HIGH-PERFORMANCE, HIGH-VOLTAGE MOTOR DRIVES

One potently damaging characteristic of a high-voltage motor-drive circuit is inductive flyback energy. Damaging voltages can result when inductor drive current is interrupted, unless some method is used to clamp the voltage and "free wheel" the inductive flyback energy (see Figure 2). For example, in unipolar motor-drive techniques, the flyback voltage is often clamped with a discrete diode to the motor supply or with a Zener diode to ground. One benefit that power MOSFETs offer is their intrinsic diodes which can serve as reliable and efficient voltage clamps.

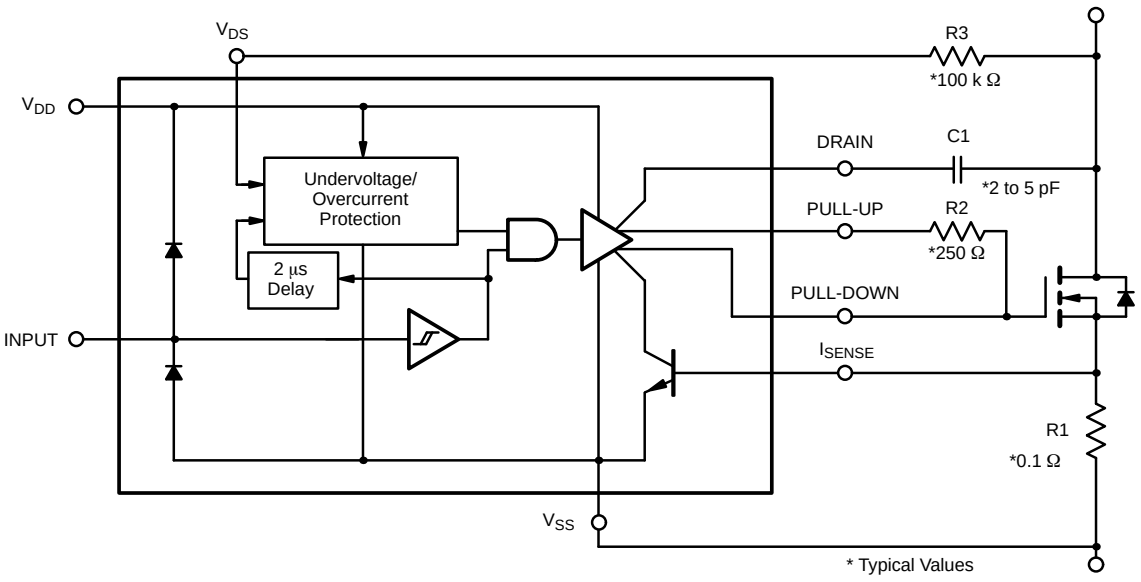


FIGURE 1. Si9910 Block Diagram

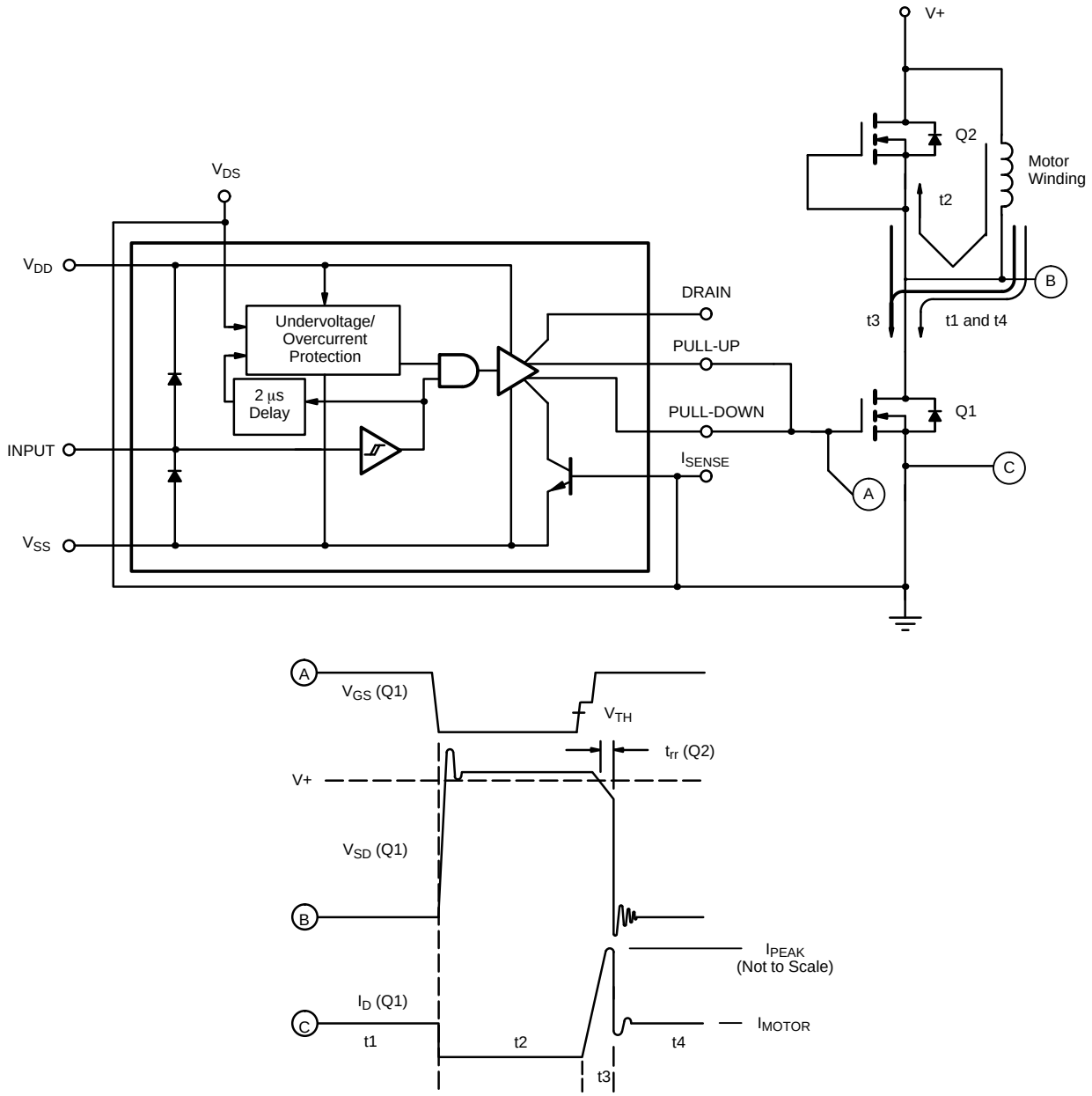


Figure 2. Clamping Inductive Flyback Energy

Most high-performance motor drives require bipolar drive techniques (not to be confused with bipolar semiconductor technology). The power switching arrangement most commonly used is the half-bridge configuration. In a half-bridge, each motor winding is connected to a common node between switching devices that can connect it to either the motor supply voltage or to the motor supply return. In half-bridge drives, the MOSFET's intrinsic diode characteristics (especially reverse recovery time, t_{rr}) become very important[1] any time a motor winding's drive is interrupted and then re-enabled in the same path while flyback current is recirculating in an opposing clamp diode.

PROTECTING THE POWER MOSFET IN MOTOR- DRIVE APPLICATIONS

The half-bridge configuration shown in Figure 2 will be used throughout this article to demonstrate the problems associated with power MOSFET protection. The gate of the upper power MOSFET is shorted to its source so the MOSFET functions only as a clamp diode. The motor winding (inductive load) is shorted to V_{motor} at one end and switched by the lower power MOSFET at the other end. In an actual motor-drive circuit, both power MOSFETs in the half-bridge would be active and the other end of the motor's winding would be tied to another half-bridge. Depending on the modulation technique employed, any of the half-bridge power MOSFETs can be used to clamp flyback energy and can be exposed to reverse-recovery current spikes by being turned on in opposition to a conducting diode. The problems demonstrated by this simplified circuit are indicative of those exhibited by either the upper or lower MOSFETs in the half-bridge.

As shown in Figure 2, during time t1 the lower MOSFET (Q1) is turned on and load current is conducted through the inductor to ground. At the leading edge of time t2, Q1 is turned off and flyback current from the inductor recirculates through the intrinsic diode in MOSFET Q2. Shoot-through current occurs during time t3 when Q1 is switched back on. As Q1 turns on, it begins to conduct load current as well as reverse current through the diode of Q2. When enough reverse current has been conducted to sweep out the minority carriers in the diode of Q2, it begins to recover. Duration of the shoot-through current spike is dependent on t_{rr} (which is, in part, a function of the diode's previous forward current and the forced di/dt during recovery). The magnitude of the current spike depends on the gate-drive voltage and forward transfer conductance (g_{fs}) of Q1 at the time of Q2 diode recovery and can be many times greater than the motor current.

LIMITING THE MOSFET'S DI/DT

As mentioned above, the current spike duration is dependent on the power MOSFET t_{rr} which is, in turn, a function of the diode forward current (motor flyback current) and di/dt during the forced recovery. Most commercial power MOSFETs have t_{rr} ratings specified with a recovery di/dt of 100 A/µs. Recovering at higher or lower di/dt rates will not change the amount of charge which must be "swept" out of the bipolar junction before recovery. Recovering at a higher di/dt rate results in higher peak currents of less duration. The only MOSFET failure mode *directly* triggered by excessive di/dt arises when it results in a peak current that is sufficient to force the MOSFET outside of its safe operating area (SOA). Until now, limiting di/dt has often been a technique used to limit the maximum rate of dv/dt (and its associated failure modes of commutating dv/dt and SOA).[2]

In a half-bridge that uses the adaptive controls of the Si9910, both the maximum recovery current and associated commutating dv/dt, which only occur when the system is delivering maximum motor current, are directly controlled.

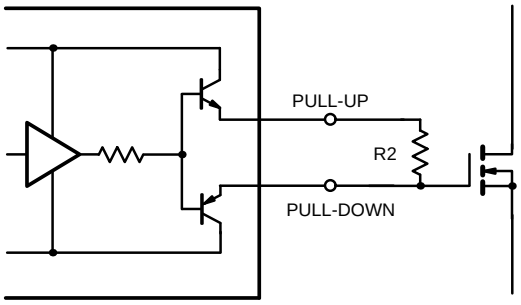


Figure 3. Simplified "Split" Emitter-Follower Output Circuit

The "split" emitter-follower output (Figure 3) of the Si9910 allows the addition of a single external resistor to set the maximum rate of system di/dt during MOSFET turn-on (Figure 4). This is a system parameter that is independently set and is not effected by variations in load current or operating conditions. With power MOSFETs, di/dt is a function of total gate capacitance during an "on" transition and the gate driver's pull-up resistance. Once a gate drive impedance and gate capacitance is established, di/dt will vary only as a result of dv/dt variations which reduce the amount of charge coupled to the MOSFET gate through the device's reverse transfer capacitance (Miller feedback capacitance).

As the value of gate-drive resistance (R2 in Figure 4) is increased, the dv_{GS}/dt of Q1 (during time t3) is reduced. The MOSFET's conducted current is a direct function of its gate voltage and transconductance (g_{fs}). Therefore, restricting dv_{GS}/dt directly reduces di/dt.

With the Si9910 adaptive MOSFET driver, the pull-up gate-drive resistance (R2) can be calculated based on a safe system di/dt level, without regard to peak current or dv/dt protection of the power MOSFETs.

[1] Addressing this issue in high-voltage (500 V) applications is a new line of MOSPOWER transistors from Vishay Siliconix with intrinsic diode recovery times rivaling discrete fast-recovery diodes. However, even these fast-recovery diodes don't solve all the problems associated with flyback energy and diode recovery. Power MOSFETs are capable of extremely fast voltage transitions and no commercially available 500-V diode (discrete or intrinsic) will be fast enough to allow the system switching losses to be absolutely minimized without regard to potentially damaging shoot-through currents.

[2] To recap, commutating or recovery dv/dt is proportional to the peak current level at the point of recovery. Peak recovery current is directly related to di/dt and t_{rr}. And a power MOSFET's t_{rr} increases as the diode's forward current increases, which is a direct function of the motor's winding current.

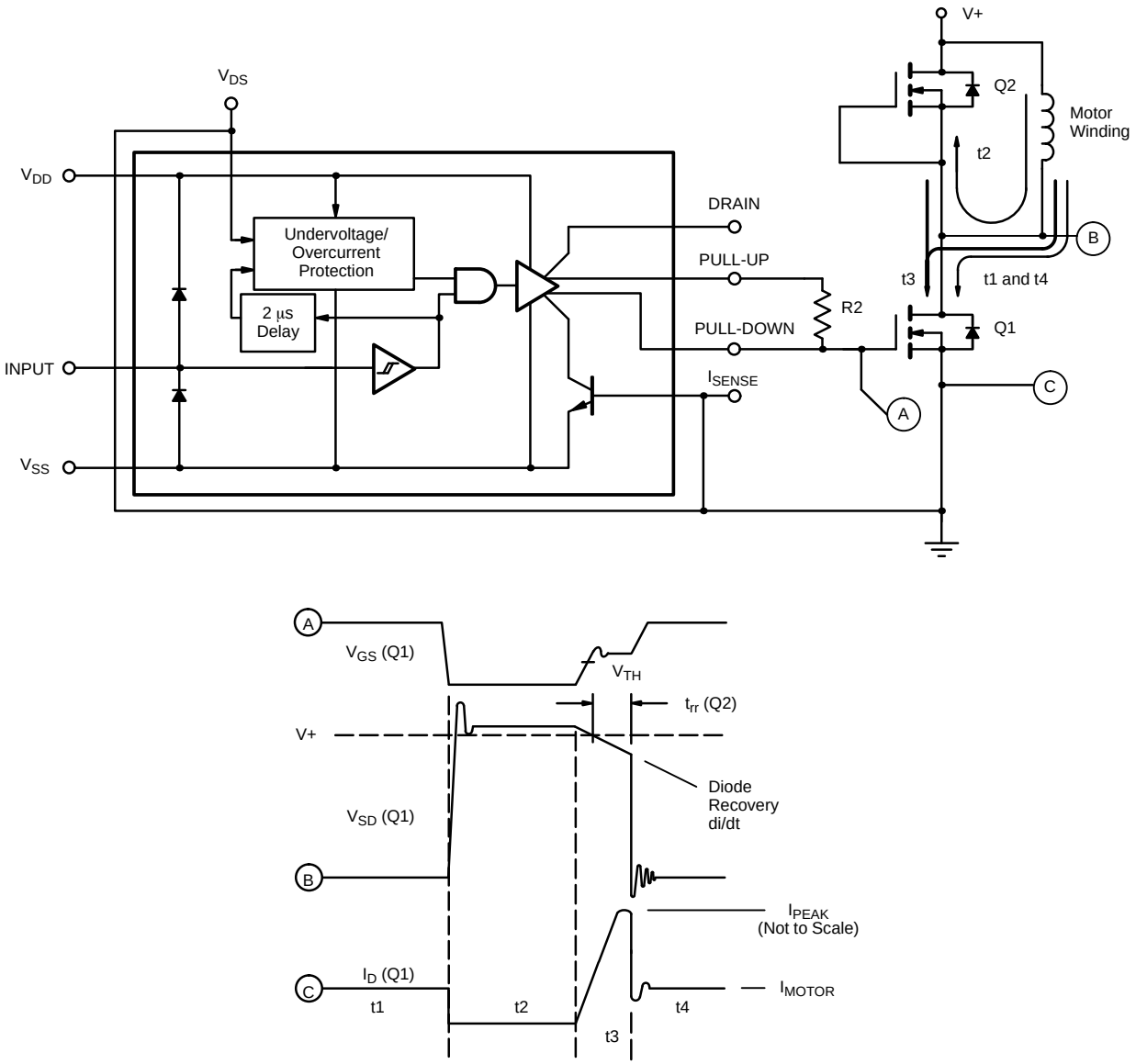


Figure 4. Controlling di/dt via MOSFET Gate Drive Impedance

LIMITING THE T_{RR}-INDUCED SHOOT-THROUGH CURRENT LEVEL

The Si9910 I_{SENSE} input can be used in conjunction with a very low-value external sense resistor to directly limit the maximum peak current (Figure 5). Figure 6 illustrates a simplified schematic of the Si9910's peak current limiting circuit. When the voltage drop across the external sense resistor (R_{SENSE}) exceeds the V_{BE} of internal transistor Q3, it begins to turn-on, shunting further increases in voltage at the common base of the output emitter-follower and, therefore, the MOSFET's gate-drive voltage (during time t3 in Figure 5).

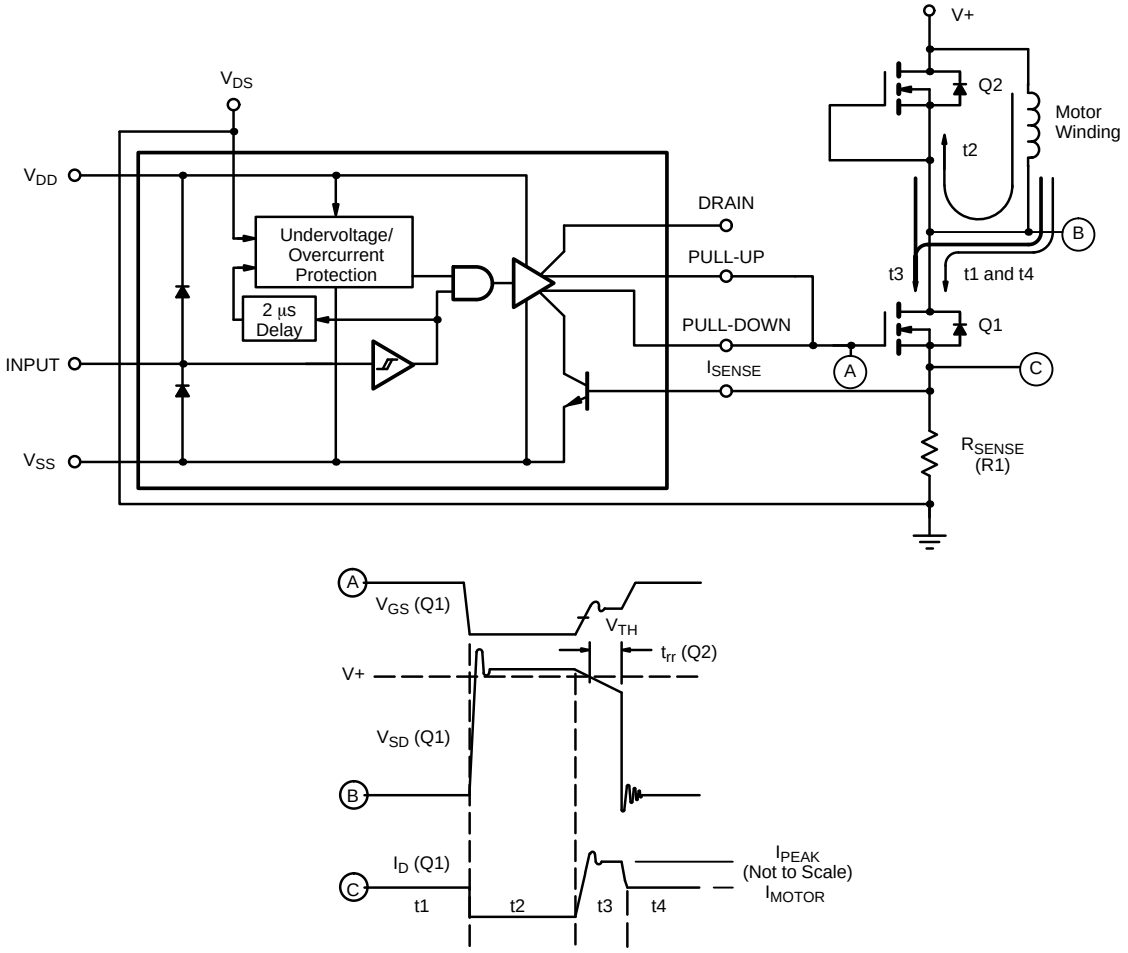


Figure 5. Limiting Peak Current

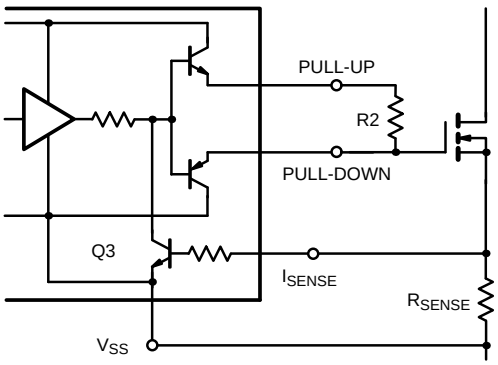


Figure 6. Simplified Peak Shoot-Through Current Limiting Circuit

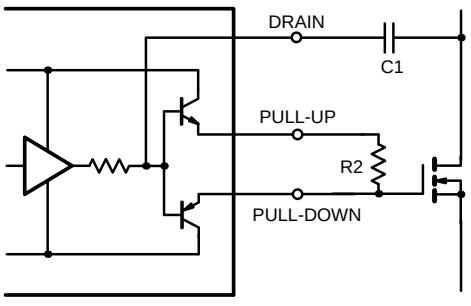


Figure 7. Simplified dv/dt Feedback Circuit

The value of external resistor R_{SENSE} should be calculated to limit the maximum shoot-through current level. The I_{SENSE} feedback is not intended to limit motor current since it restricts the MOSFET's dv_{GS}/dt, leaving the MOSFET in transition for a longer period of time. R_{SENSE} should be sized to limit current at a level approximately four times greater than the peak motor current.

$$R_{SENSE} = \frac{0.8\ V}{4 \times \text{Peak Motor Current}}$$

This transient current level is consistent with the power MOSFET's peak current rating which (in most commercially available power MOSFETs) is four times the continuous current rating.

DIRECTLY LIMITING THE MOSFET'S DV/DT

Figure 7 is a simplified schematic of the Si9910's feedback circuit used to sense and limit maximum half-bridge dv/dt. As the common base of the emitter-follower stage changes from a low to a high level, the output follows, turning the power MOSFET on. As the power MOSFET switches on, the voltage across its drain-source decreases rapidly. The rate of dv/dt will depend on all of the conditions described earlier that are associated with diode reverse recovery. When a switching transition occurs, it will couple charge through the external capacitor (C1) which decreases the rise time of the emitter-follower's common base and, in turn, limits the dv_{GS}/dt of the power MOSFET. In a typical motor-drive circuit, maximum dv/dt will only occur during worst-case motor current, which is a transient condition. This technique permits faster switching (and higher efficiency) during normal operation and provides dv/dt protection for the MOSFETs when it is required.

The drain input must be limited to low voltage, which requires connection to the MOSFET's drain via a capacitor capable of withstanding the full motor-drive voltage (Figure 8).

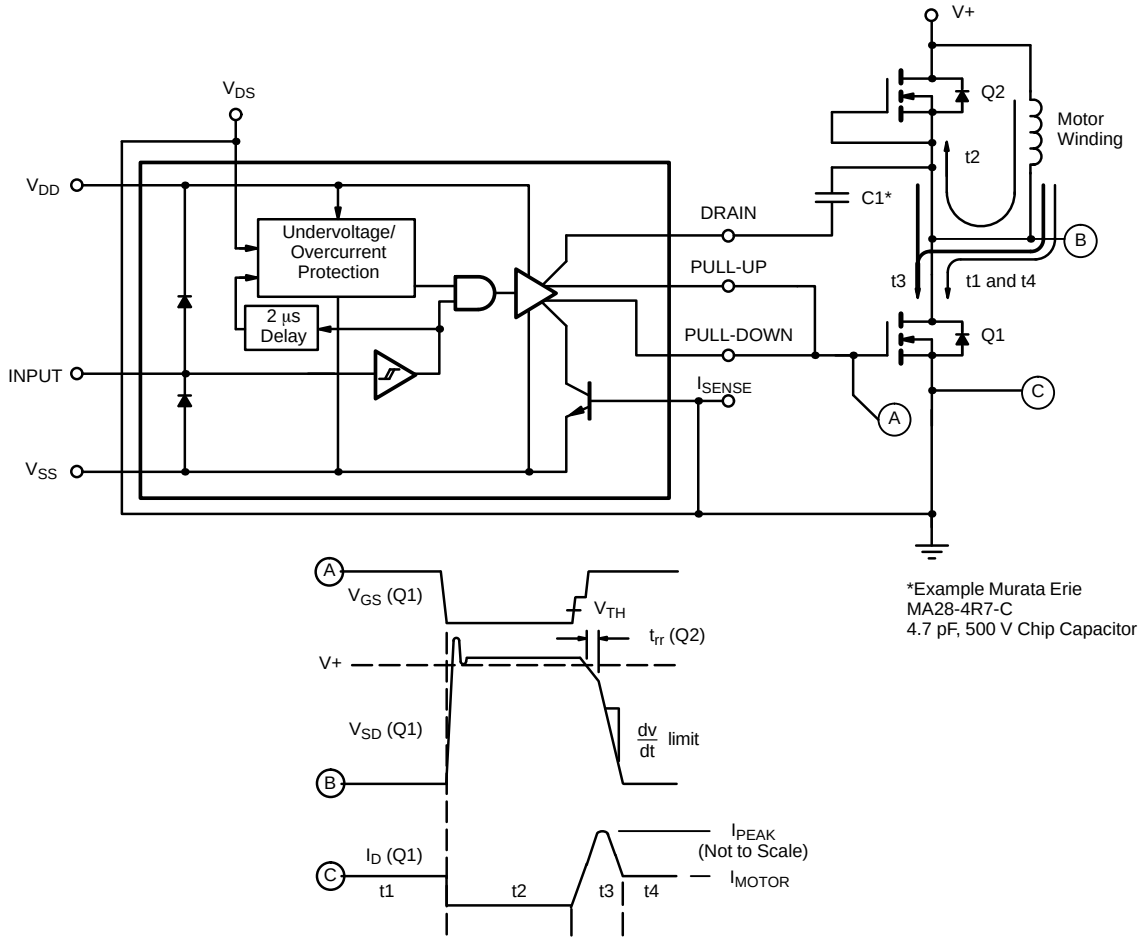
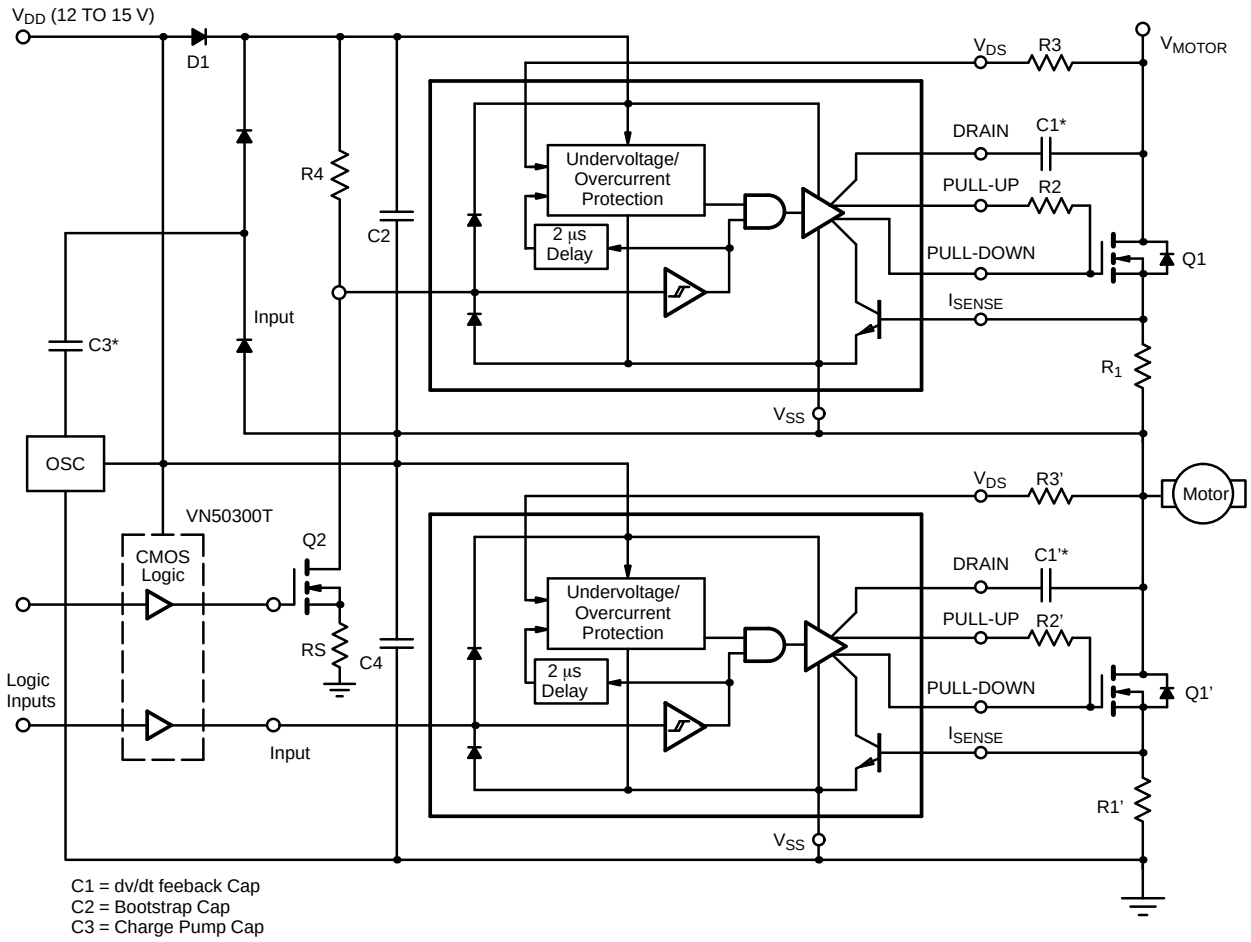


Figure 8. Direct dv/dt Limiting



C1 = dv/dt feeback Cap
C2 = Bootstrap Cap
C3 = Charge Pump Cap

*C1 – C3 0.3 to 1000 pF, 500 V, surface mount capacitors are available in a line of high Q porcelain ceramic capacitors from Murata.

Figure 9. High-Voltage Half-Bridge with Si9910 Drivers

"FLOATING" HIGH-SIDE DRIVE APPLICATIONS

As demonstrated in Figure 9, the Si9910 is intended for use as both a ground-referenced gate driver and as a "high-side" or source-referenced gate driver in half-bridge applications. Several features of the Si9910 facilitate its use in half-bridge high-side drive applications.

The Si9910 was designed to be compatible with two of the most commonly used floating supply techniques: the bootstrap and the charge pump. Both of these techniques have limitations when used alone. A properly designed bootstrap circuit can provide low-impedance drive which minimizes transition losses, but it does not provide static (100% duty-cycle) drive. Eventually the bootstrap capacitor's charge will be depleted by system leakages, resulting in reduced (potentially damaging) levels of gate-drive voltage. A charge pump circuit can provide static operation but usually yields increased gate-drive impedance, which ultimately results in slower transition rates and increased switching losses. As the charge pump capacitance is increased to provide faster transition rates, the oscillator circuit is subjected to higher peak currents in the presence of the dv/dt rates that exist in half-bridge motor drives. This limits the extent to which the charge pump capacitor can be increased.

The Si9910 is configured to take advantage of either floating supply technique, (if the application is not sensitive to their particular limitations), or a combination of both techniques (if switching losses must be minimized and static operation is necessary). Figure 9 illustrates both the charge pump and bootstrap circuits used in conjunction with an Si9910 in a high-side driver application.

BOOTSTRAP UNDERVOLTAGE LOCKOUT

When using a bootstrap capacitor as a high-side floating supply, sufficient time must be allowed to recharge the bootstrap capacitor prior to turn-on of the high-side MOSFET. As protection against catastrophic transient conditions such as start-up, loss of power, etc., an internal voltage monitor has been included which monitors the bootstrap voltage when the Si9910 is in the low state. The Si9910 will not respond to a high input signal until the voltage on the bootstrap capacitor is sufficient to fully enhance the power MOSFET gate.

MAXIMUM V_{DS} MONITOR

The Si9910 V_{DS} input monitors the source-drain voltage drop across the MOSFET in the "on" state. Excess V_{DS} can occur as a result of high on-resistance ($r_{DS(ON)}$) at increased temperature, insufficient gate enhancement voltage, or excessive current. Regardless of the cause, the effects can be catastrophic. The first priority of the Si9910 is to protect the power MOSFET. Therefore, a maximum V_{DS} monitor is enabled 2 µs after each positive-going input transition. Voltage exceeding the V_{DS} maximum (data sheet limit) will cause the gate driver to go to a low state and to wait for the next positive-going input command.

The V_{DS} pin is a low-voltage input which must be isolated from the high voltages at the power MOSFET's drain by an external resistor. The value of the external resistor is not critical to the operation of the maximum V_{DS} shutdown circuit. A 100-kΩ resistor is sufficient to isolate the high-voltage with minimum power losses and still drive the low capacitance input with tolerable response times.

INPUT LEVEL TRANSLATION

Input logic signals must be level shifted to control the driver in the high-side of a half-bridge application. The circuit illustrated in Figure 9 uses a simple passive pull-up (R4) and a high-voltage, small-signal MOSFET (Q2) for level translation. The VN50300 was selected for its extremely low drain capacitance (1.8 pF typical). The drain capacitance of Q2 is important because of the direct effect it has on the value of R4.

The value of R4 should be sufficient to provide an RC time constant that is faster than the turn-on rate of Q1. The capacitance that must be driven is the total at the Si9910's input node (2 pF typical for the Si9910 plus 1.8 pF typical for the VN50300 plus any stray wiring and board capacitances).

R4 must also have a value that is high enough (relative to the on-resistance of Q2) to maintain a logic level of zero (3 V maximum) when the low-side device is turned on.

The minimum value of R4 necessary to achieve a safe RC time constant depends on the turn-on rate of Q1, which can be altered by adjusting the value of R2. (For most mid-sized MOSFETs [1000–3000 pF C_{iss}] typical values are 250 Ω for R2, 5 pF for the input-node capacitance, and 10 kΩ for R4.) Observing the half-bridge's positive-going output-voltage transition with an oscilloscope will reveal any "input-laging-output" imbalance as a sawtooth voltage waveform. Trying to observe the input-voltage transition directly is difficult since addition of any scope probe capacitance can significantly alter the node's switching characteristics.

Some applications will require current limiting of Q2. It is common, for instance, in brushless, three-phase motor drives to encounter a condition where both the high and low-side MOSFETs (Q1 and Q1') are off for some period during each cycle. During this time, for a particular phase, Q2 will be on, but since the lower output MOSFET is not on, the output voltage from the bridge is defined by the back EMF of the motor (which may be as much as 80 to 90% of V+ at maximum velocity). If Q2 is a VN50300, inherent protection results from the device's low saturation current capability (see the VN50300 characteristic curves in Vishay Siliconix Low Power Discretes Data Book). If level-shift devices that have higher-saturation current capability are substituted, measures may have to be implemented (such as series resistance in the source or drain of Q2) to protect the level-shift device and/or the input of the Si9910.

FLEXIBLE FEEDBACK OPTIONS

Each of the feedback options — dv/dt limiting, peak current limiting and maximum V_{DS} — may be used separately or in any combination. Figure 10 shows all the external feedback options connected and the resulting voltage/current waveforms. If the designer chooses not to use the V_{DS} input to monitor maximum V_{DS}, it should be tied to V_{SS}. When the drain input is not in use, it must be left open. When the I_{SENSE} input is not in use, it should be shorted to V_{SS}.

PACKAGING CONCEPT: USING SURFACE-MOUNT SI9910S WITH POWER MOSFET CHIPS

Using surface-mount driver ICs, such as the Si9910DY shown in Figure 11, on a substrate with power MOSFET chips holds great promise for next-generation motor drives. The power MOSFET can be mounted directly on a substrate with good thermal transfer characteristics, thus solving the density and power dissipation problems commonly associated with motor controllers. Power MOSFETs are relatively easy to handle in die form and can be tested prior to packaging. Handling ICs in die form, however, presents problems which can be avoided with low-cost, compact surface-mount packages such as the Si9910DY.

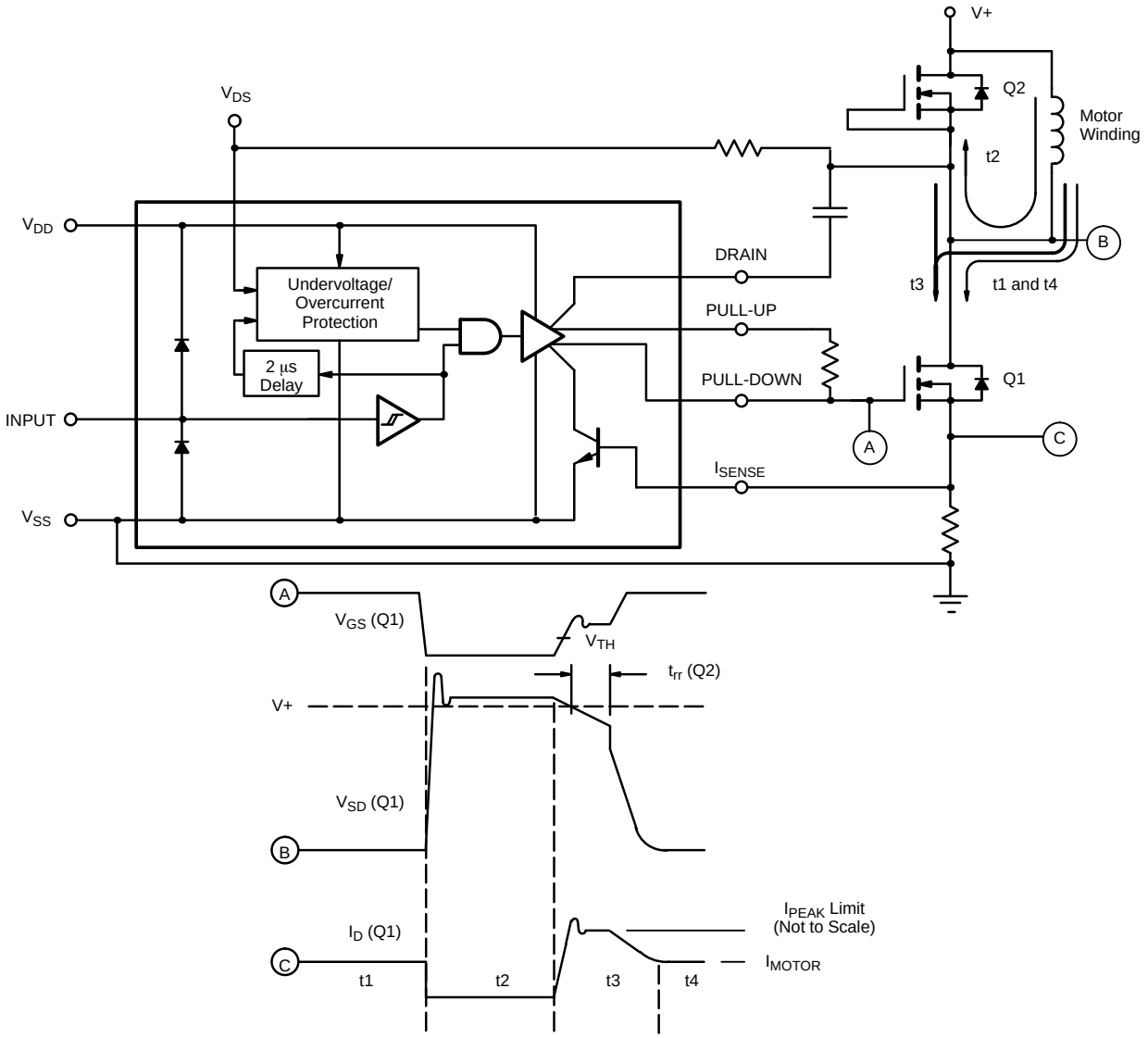


Figure 10. All Feedback Options Active

SUMMARY

The Si9910 introduces a new generation of “adaptive” power MOSFET gate drivers that use active feedback to protect the power MOSFET, while allowing logic-level control of high-voltage signals. The Si9910’s first priority is to protect the power MOSFET that it drives.

When all of its protective options are enabled, the Si9910 is capable of controlling the power MOSFET dv/dt, di/dt, maximum peak current, minimum gate-drive voltage, and maximum source-drain voltage drop. The Si9910 allows the system designer to take full advantage of the increased performance and efficiency characteristics of power MOSFETs by designing the system with optimized switching losses and efficiency, while leaving worst-case system protection to the driver.

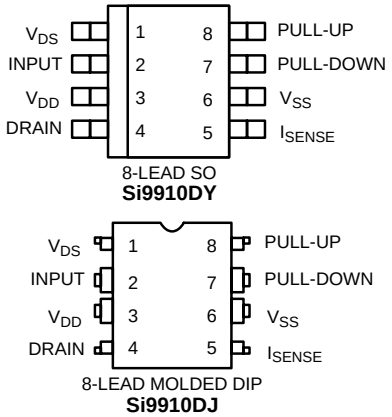


Figure 11. Si9910DY and Si9910DJ Package Pin-Outs