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## AOD604

### Complementary Enhancement Mode Field Effect Transistor

#### General Description

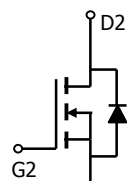
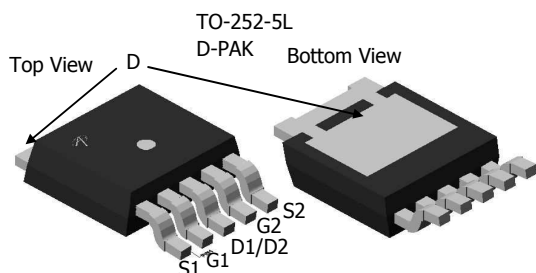
The AOD604 uses advanced trench technology MOSFETs to provide excellent  $R_{DS(ON)}$  and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

- RoHS Compliant
- Halogen Free\*

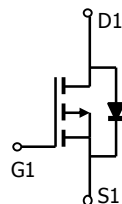
#### Features

|                                   |                                      |
|-----------------------------------|--------------------------------------|
| n-channel                         | p-channel                            |
| $V_{DS}$ (V) = 40V                | -40V                                 |
| $I_D$ = 8A ( $V_{GS}=10V$ )       | -8A ( $V_{GS} = -10V$ )              |
| $R_{DS(ON)}$                      | $R_{DS(ON)}$                         |
| < 33 m $\Omega$ ( $V_{GS}=10V$ )  | < 50 m $\Omega$ ( $V_{GS} = -10V$ )  |
| < 47 m $\Omega$ ( $V_{GS}=4.5V$ ) | < 70 m $\Omega$ ( $V_{GS} = -4.5V$ ) |

**100% UIS Tested!**



n-channel



p-channel

#### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

| Parameter   | Symbol         | Max n-channel          | Max p-channel | Units            |
|---|----------------|------------------------|---------------|------------------|
| Drain-Source Voltage                                      | $V_{DS}$       | 40                     | -40           | V                |
| Gate-Source Voltage                                       | $V_{GS}$       | $\pm 20$               | $\pm 20$      | V                |
| Continuous Drain Current <sup>G</sup>                     | $I_D$          | 8                      | -8            | A                |
| $T_C=25^\circ\text{C}$                                    |                | 6.3                    | -6.3          |                  |
| Pulsed Drain Current <sup>C</sup>                         | $I_{DM}$       | 30                     | -30           |                  |
| Avalanche Current <sup>C</sup>                            | $I_{AR}$       | 8                      | -8            | A                |
| Repetitive avalanche energy $L=0.1\text{mH}$ <sup>C</sup> | $E_{AR}$       | 20                     | 30            | mJ               |
| Power Dissipation <sup>B</sup>                            | $P_D$          | 20                     | 30            | W                |
|   |                | $T_C=25^\circ\text{C}$ | 10            |                  |
| Power Dissipation <sup>A</sup>                            | $P_{DSM}$      | 1.6                    | 1.7           | W                |
|   |                | $T_A=25^\circ\text{C}$ | 1             |                  |
| Junction and Storage Temperature Range                    | $T_J, T_{STG}$ | -55 to 175             | -55 to 175    | $^\circ\text{C}$ |

#### Thermal Characteristics: n-channel and p-channel

| Parameter                                | Symbol          | Device | Typ | Max | Units              |
|--|-----------------|--------|-----|-----|--------------------|
| Maximum Junction-to-Ambient <sup>A</sup> | $R_{\theta JA}$ | n-ch   | 25  | 30  | $^\circ\text{C/W}$ |
| $t \leq 10\text{s}$                      |                 | n-ch   | 66  | 80  | $^\circ\text{C/W}$ |
| Maximum Junction-to-Ambient <sup>A</sup> | $R_{\theta JA}$ | p-ch   | 17  | 25  | $^\circ\text{C/W}$ |
| Steady-State                             |                 | p-ch   | 60  | 75  | $^\circ\text{C/W}$ |
| Maximum Junction-to-Case <sup>B</sup>    | $R_{\theta JC}$ | n-ch   | 7   | 7.5 | $^\circ\text{C/W}$ |
| Steady-State                             |                 | p-ch   | 4   | 5   | $^\circ\text{C/W}$ |

**AOD604**
**N-Channel MOSFET Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

| Symbol                      | Parameter                             | Conditions  | Min | Typ  | Max    | Units |
|-----------------------------|---------------------------------------|---|-----|------|--------|-------|
| <b>STATIC PARAMETERS</b>    |                                       |   |     |      |        |       |
| BV <sub>DSS</sub>           | Drain-Source Breakdown Voltage        | I <sub>D</sub> =10mA, V <sub>GS</sub> =0V   | 40  |      |        | V     |
| I <sub>DSS</sub>            | Zero Gate Voltage Drain Current       | V <sub>DS</sub> =32V, V <sub>GS</sub> =0V<br>T <sub>J</sub> =55°C                         |     |      | 1<br>5 | μA    |
| I <sub>GSS</sub>            | Gate-Body leakage current             | V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V  |     |      | 100    | nA    |
| V <sub>GS(th)</sub>         | Gate Threshold Voltage                | V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA                                  | 1   | 2.3  | 3      | V     |
| I <sub>D(ON)</sub>          | On state drain current                | V <sub>GS</sub> =10V, V <sub>DS</sub> =5V   | 30  |      |        | A     |
| R <sub>DS(ON)</sub>         | Static Drain-Source On-Resistance     | V <sub>GS</sub> =10V, I <sub>D</sub> =8A  |     | 25   | 33     | mΩ    |
|                             |                                       | T <sub>J</sub> =125°C   |     | 39   | 52     |       |
|                             |                                       | V <sub>GS</sub> =4.5V, I <sub>D</sub> =6A   |     | 34   | 47     | mΩ    |
| g <sub>FS</sub>             | Forward Transconductance              | V <sub>DS</sub> =5V, I <sub>D</sub> =8A   |     | 25   |        | S     |
| V <sub>SD</sub>             | Diode Forward Voltage                 | I <sub>S</sub> =1A, V <sub>GS</sub> =0V   |     | 0.76 | 1      | V     |
| I <sub>S</sub>              | Maximum Body-Diode Continuous Current |   |     |      | 8      | A     |
| <b>DYNAMIC PARAMETERS</b>   |                                       |   |     |      |        |       |
| C <sub>iss</sub>            | Input Capacitance                     | V <sub>GS</sub> =0V, V <sub>DS</sub> =20V, f=1MHz   |     | 404  |        | pF    |
| C <sub>oss</sub>            | Output Capacitance                    |   |     | 95   |        | pF    |
| C <sub>rss</sub>            | Reverse Transfer Capacitance          |   |     | 37   |        | pF    |
| R <sub>g</sub>              | Gate resistance                       | V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz  |     | 2.7  |        | Ω     |
| <b>SWITCHING PARAMETERS</b> |                                       |   |     |      |        |       |
| Q <sub>g(10V)</sub>         | Total Gate Charge                     | V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =8A                            |     | 9.2  |        | nC    |
| Q <sub>g(4.5V)</sub>        | Total Gate Charge                     |   |     | 4.5  |        | nC    |
| Q <sub>gs</sub>             | Gate Source Charge                    |   |     | 1.6  |        | nC    |
| Q <sub>gd</sub>             | Gate Drain Charge                     |   |     | 2.6  |        | nC    |
| t <sub>D(on)</sub>          | Turn-On DelayTime                     | V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, R <sub>L</sub> =2.5Ω,<br>R <sub>GEN</sub> =3Ω |     | 3.5  |        | ns    |
| t <sub>r</sub>              | Turn-On Rise Time                     |   |     | 6    |        | ns    |
| t <sub>D(off)</sub>         | Turn-Off DelayTime                    |   |     | 13.2 |        | ns    |
| t <sub>f</sub>              | Turn-Off Fall Time                    |   |     | 3.5  |        | ns    |
| t <sub>rr</sub>             | Body Diode Reverse Recovery Time      | I <sub>F</sub> =8A, di/dt=100A/μs   |     | 22.9 |        | ns    |
| Q <sub>rr</sub>             | Body Diode Reverse Recovery Charge    | I <sub>F</sub> =8A, di/dt=100A/μs   |     | 18.3 |        | nC    |

A: The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.

D: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

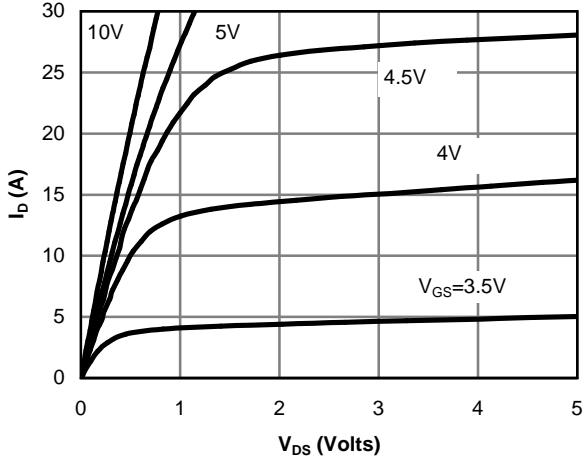
\*This device is guaranteed green after data code 8X11 (Sep 1<sup>ST</sup> 2008).

Rev3: Sep. 2008

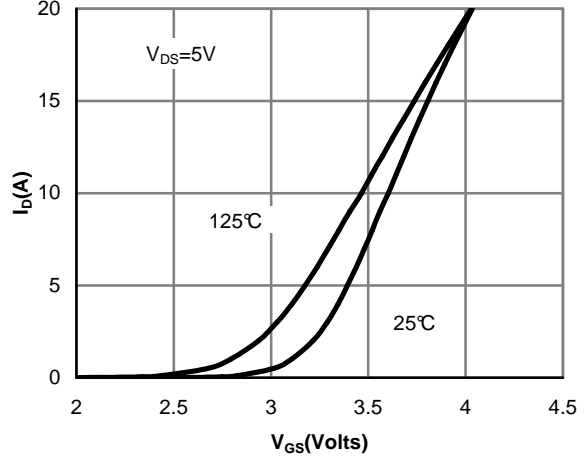
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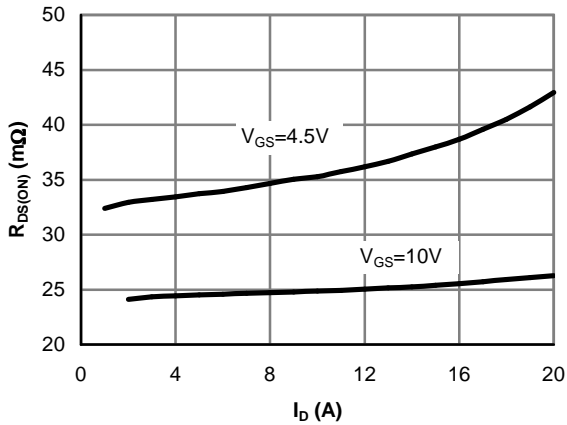
**N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



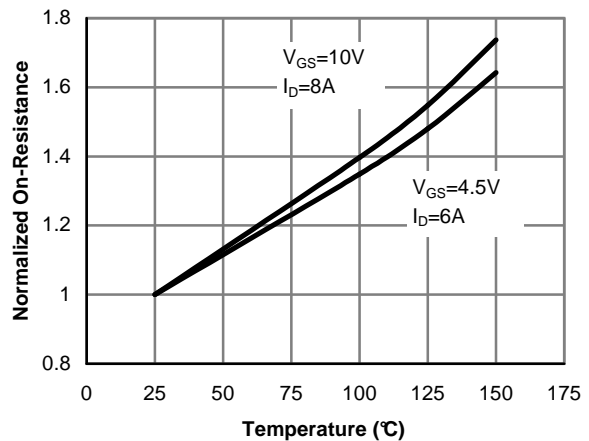
**Fig 1: On-Region Characteristics**



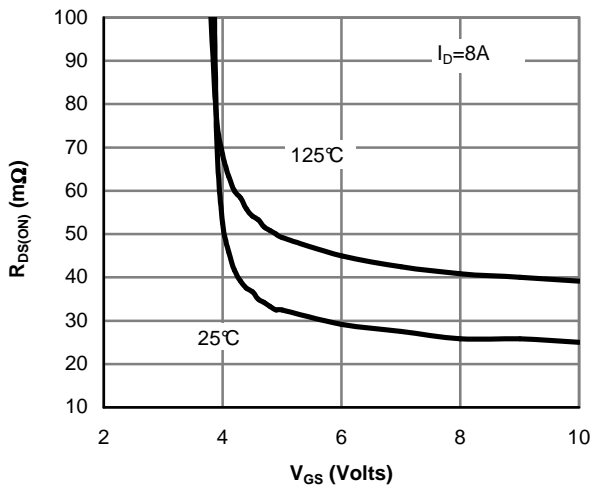
**Figure 2: Transfer Characteristics**



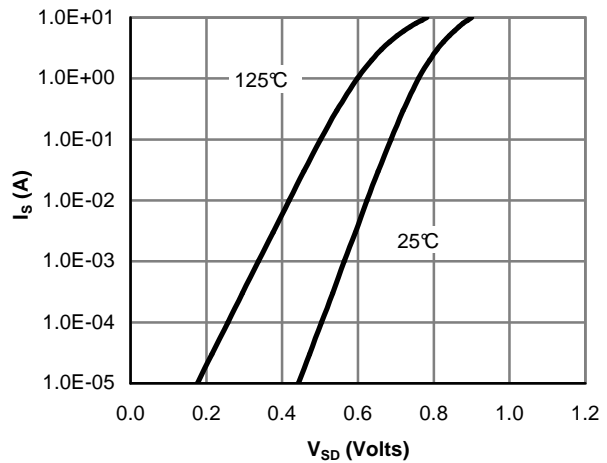
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**



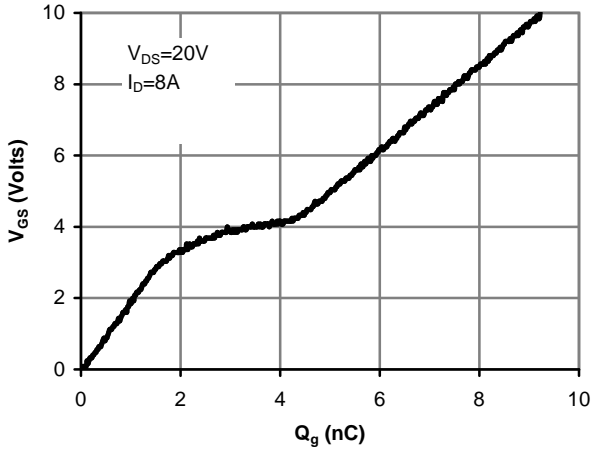
**Figure 5: On-Resistance vs. Gate-Source Voltage**



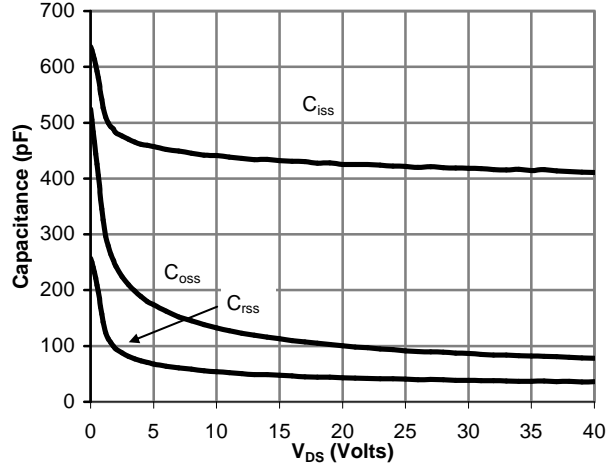
**Figure 6: Body-Diode Characteristics**

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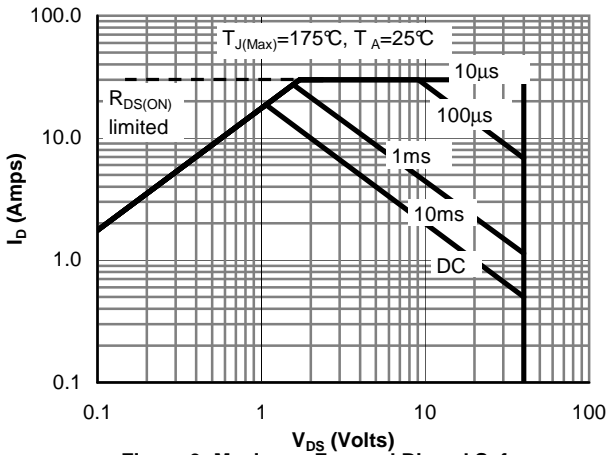
**N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



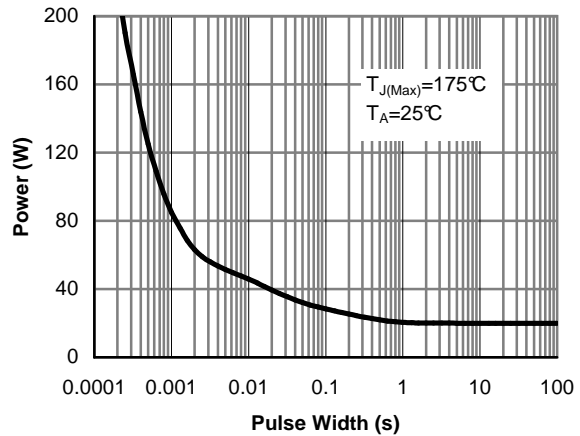
**Figure 7: Gate-Charge Characteristics**



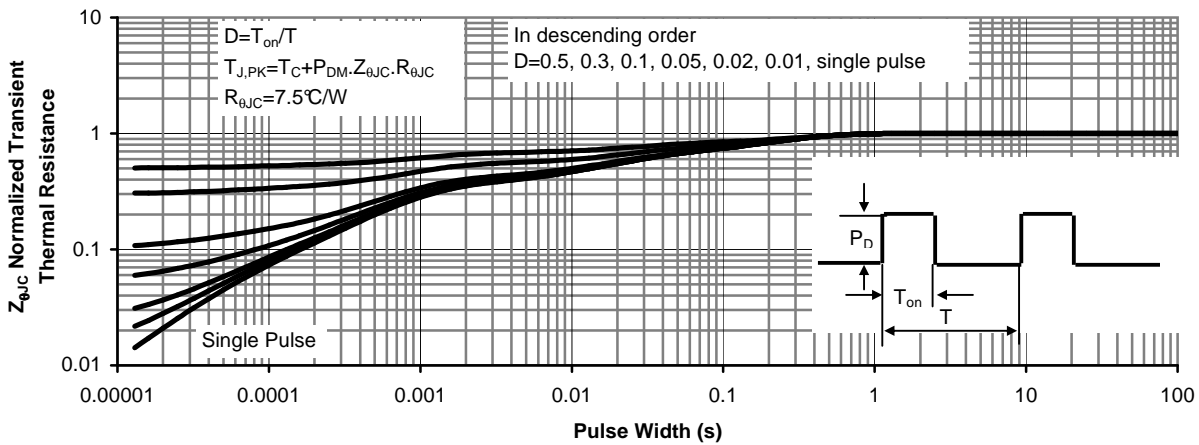
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**AOD604**

**N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

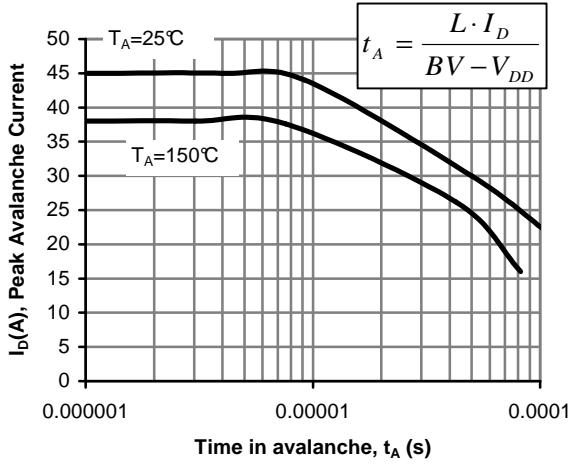


Figure 12: Single Pulse Avalanche capability

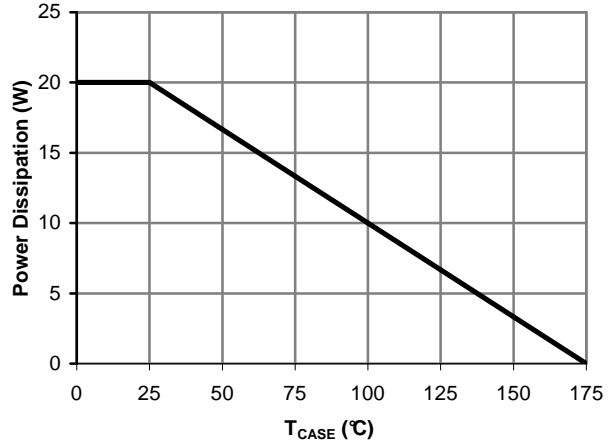


Figure 13: Power De-rating (Note B)

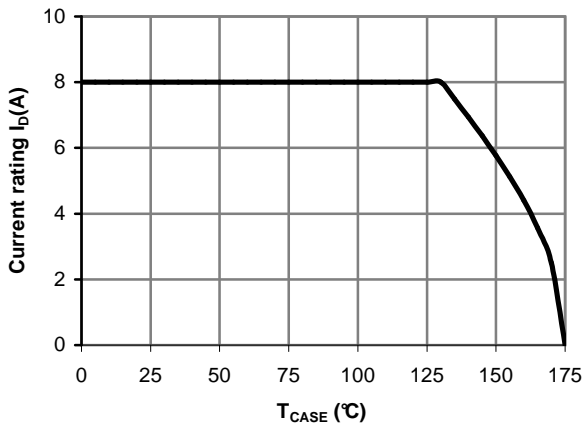


Figure 14: Current De-rating (Note B)

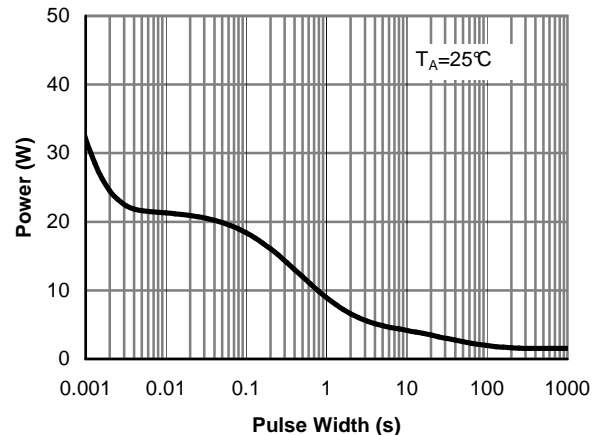


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

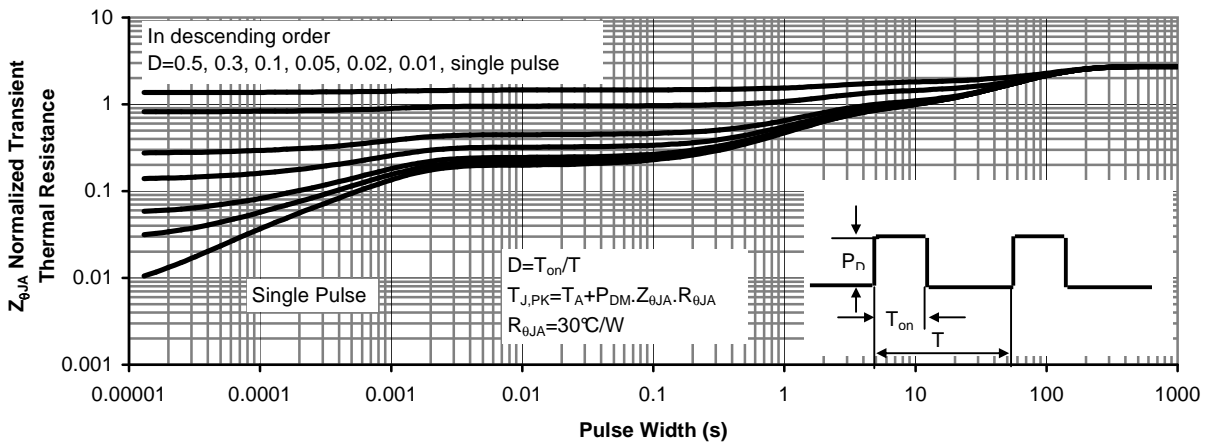


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

**AOD604**
**P-Channel MOSFET Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

| Symbol                      | Parameter                             | Conditions  | Min                                | Typ      | Max      | Units |
|-----------------------------|---------------------------------------|---|------------------------------------|----------|----------|-------|
| <b>STATIC PARAMETERS</b>    |                                       |   |                                    |          |          |       |
| BV <sub>DSS</sub>           | Drain-Source Breakdown Voltage        | I <sub>D</sub> =-10mA, V <sub>GS</sub> =0V  | -40                                |          |          | V     |
| I <sub>DSS</sub>            | Zero Gate Voltage Drain Current       | V <sub>DS</sub> =-32V, V <sub>GS</sub> =0V<br>T <sub>J</sub> =55°C                          |                                    |          | -1<br>-5 | μA    |
| I <sub>GSS</sub>            | Gate-Body leakage current             | V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V  |                                    |          | ±100     | nA    |
| V <sub>GS(th)</sub>         | Gate Threshold Voltage                | V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =-250μA                                     | -1                                 | -1.8     | -3       | V     |
| I <sub>D(ON)</sub>          | On state drain current                | V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V   | -30                                |          |          | A     |
| R <sub>DS(ON)</sub>         | Static Drain-Source On-Resistance     | V <sub>GS</sub> =-10V, I <sub>D</sub> =-8A<br>T <sub>J</sub> =125°C                         |                                    | 41<br>62 | 50       | mΩ    |
|                             |                                       | V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A   |                                    | 57       | 70       | mΩ    |
| g <sub>FS</sub>             | Forward Transconductance              | V <sub>DS</sub> =-5V, I <sub>D</sub> =-8A   |                                    | 16       |          | S     |
| V <sub>SD</sub>             | Diode Forward Voltage                 | I <sub>S</sub> =-1A, V <sub>GS</sub> =0V  | -0.75                              |          | -1       | V     |
| I <sub>S</sub>              | Maximum Body-Diode Continuous Current |   |                                    |          | -8       | A     |
| <b>DYNAMIC PARAMETERS</b>   |                                       |   |                                    |          |          |       |
| C <sub>iss</sub>            | Input Capacitance                     | V <sub>GS</sub> =0V, V <sub>DS</sub> =-20V, f=1MHz  |                                    | 657      |          | pF    |
| C <sub>oss</sub>            | Output Capacitance                    |   |                                    | 143      |          | pF    |
| C <sub>rss</sub>            | Reverse Transfer Capacitance          |   |                                    | 63       |          | pF    |
| R <sub>g</sub>              | Gate resistance                       | V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz  |                                    | 6.5      |          | Ω     |
| <b>SWITCHING PARAMETERS</b> |                                       |   |                                    |          |          |       |
| Q <sub>g(10V)</sub>         | Total Gate Charge (10V)               | V <sub>GS</sub> =-10V, V <sub>DS</sub> =-20V, I <sub>D</sub> =-8A                           |                                    | 14.1     |          | nC    |
| Q <sub>g(4.5V)</sub>        | Total Gate Charge (4.5V)              |   |                                    | 7        |          | nC    |
| Q <sub>gs</sub>             | Gate Source Charge                    |   |                                    | 2.2      |          | nC    |
| Q <sub>gd</sub>             | Gate Drain Charge                     |   |                                    | 4.1      |          | nC    |
| t <sub>D(on)</sub>          | Turn-On DelayTime                     | V <sub>GS</sub> =-10V, V <sub>DS</sub> =-20V, R <sub>L</sub> =2.5Ω,<br>R <sub>GEN</sub> =3Ω |                                    | 8        |          | ns    |
| t <sub>r</sub>              | Turn-On Rise Time                     |   |                                    | 12.2     |          | ns    |
| t <sub>D(off)</sub>         | Turn-Off DelayTime                    |   |                                    | 24       |          | ns    |
| t <sub>f</sub>              | Turn-Off Fall Time                    |   |                                    | 12.5     |          | ns    |
| t <sub>rr</sub>             | Body Diode Reverse Recovery Time      |   | I <sub>F</sub> =-8A, dI/dt=100A/μs |          | 23.2     |       |
| Q <sub>rr</sub>             | Body Diode Reverse Recovery Charge    | I <sub>F</sub> =-8A, dI/dt=100A/μs  |                                    | 18.2     |          | nC    |

A: The value of R<sub>qJA</sub> is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation PDSM is based on R<sub>qJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation PD is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.

D: The R<sub>qJA</sub> is the sum of the thermal impedance from junction to case R<sub>qJC</sub> and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 ms pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

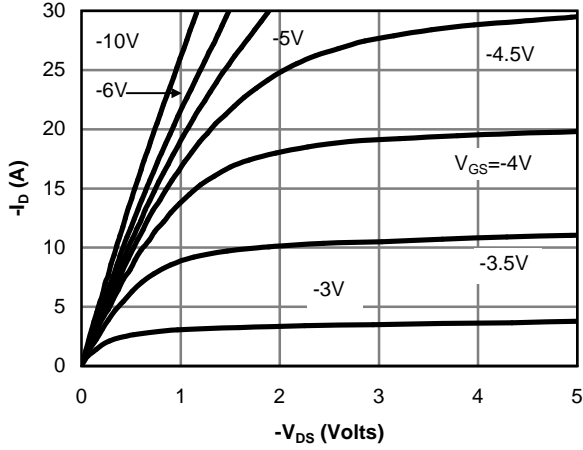
\*This device is guaranteed green after data code 8X11 (Sep 1<sup>ST</sup> 2008).

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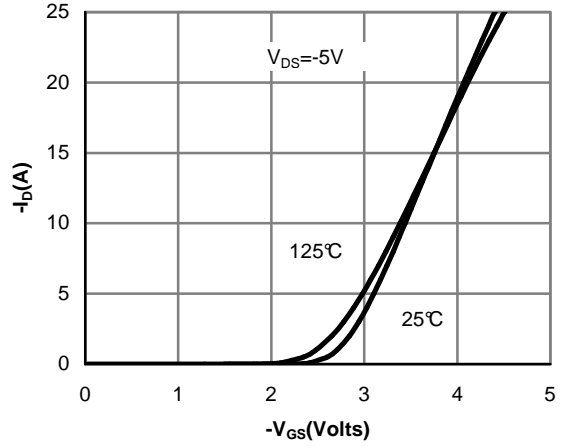
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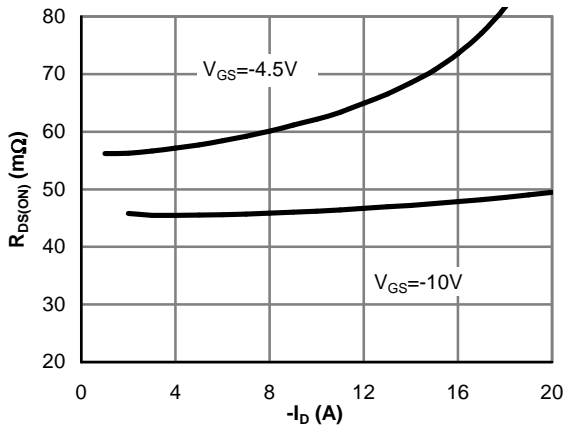
**P-Channel MOSFET Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**



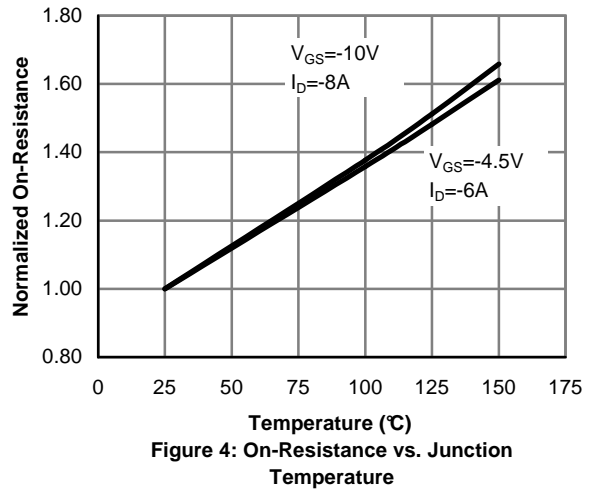
**Fig 1: On-Region Characteristics**



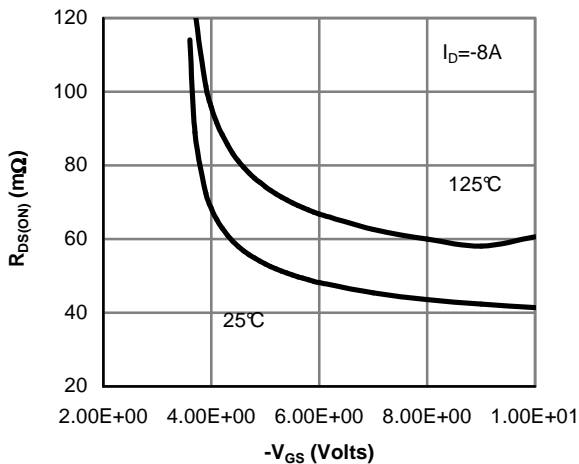
**Figure 2: Transfer Characteristics**



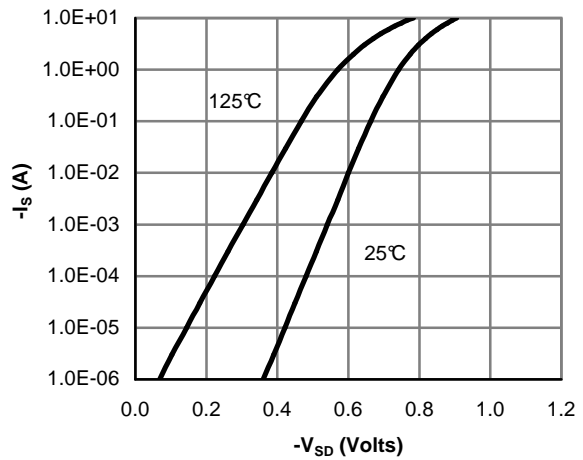
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**



**Figure 5: On-Resistance vs. Gate-Source Voltage**

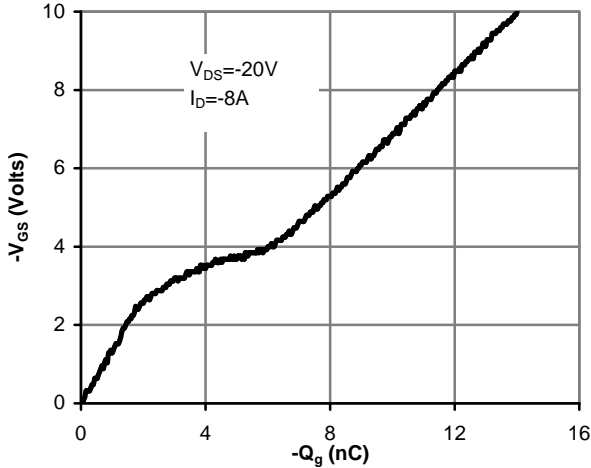


**Figure 6: Body-Diode Characteristics**

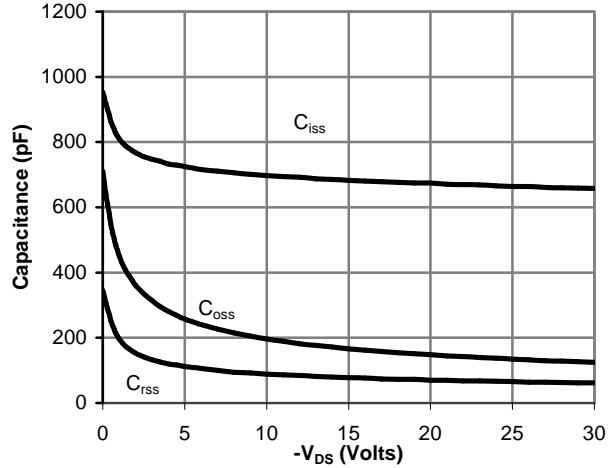


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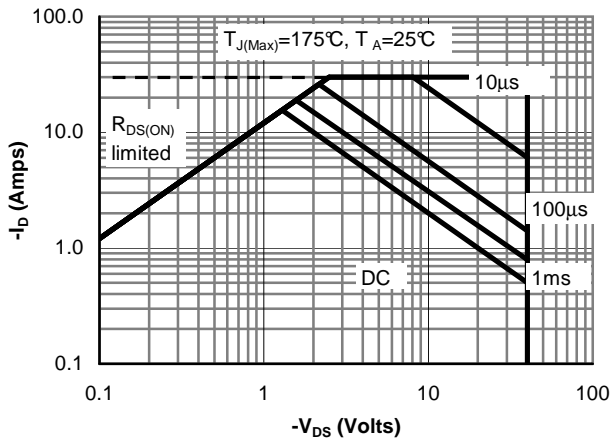
**P-Channel MOSFET Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)**



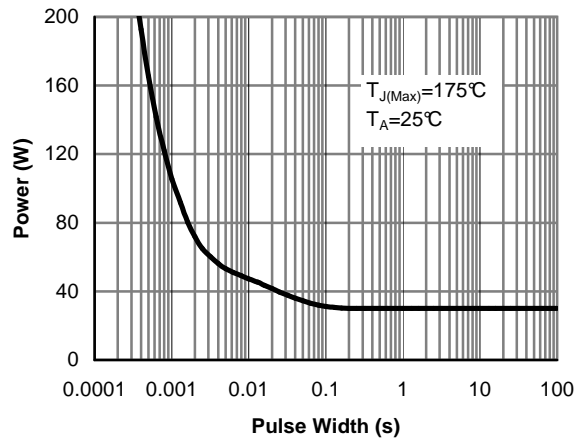
**Figure 7: Gate-Charge Characteristics**



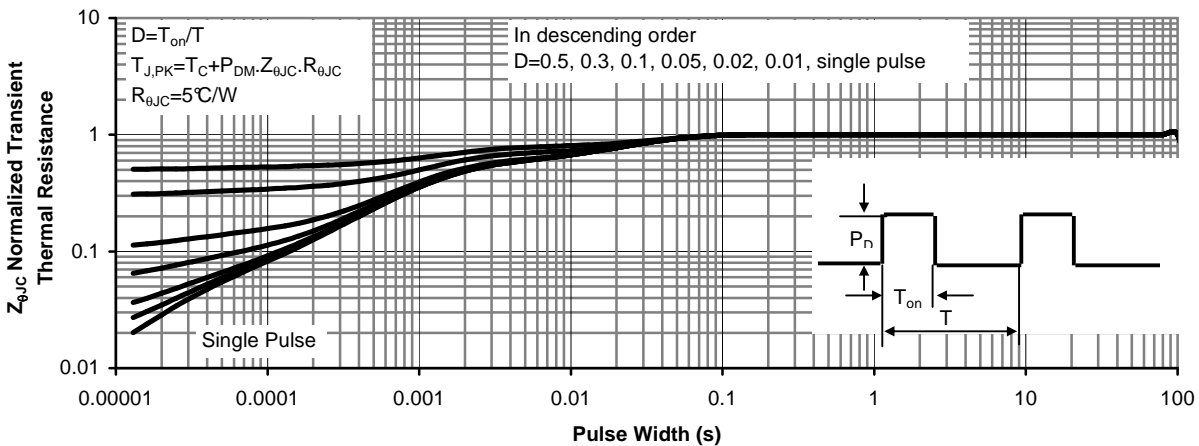
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**AOD604**

**P-Channel MOSFET Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

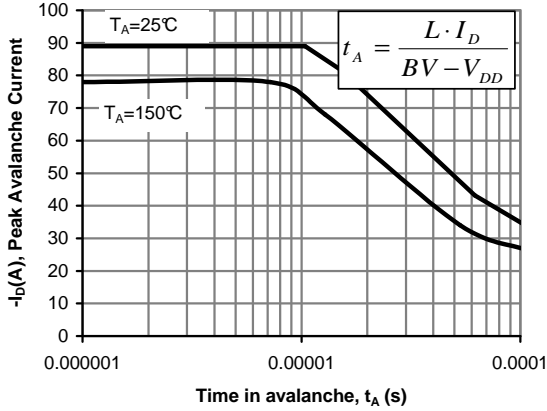


Figure 12: Single Pulse Avalanche capability

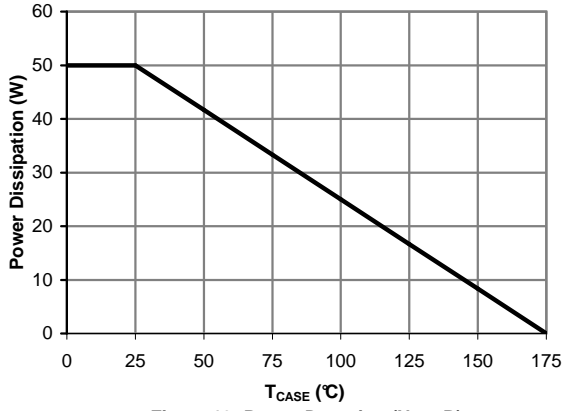


Figure 13: Power De-rating (Note B)

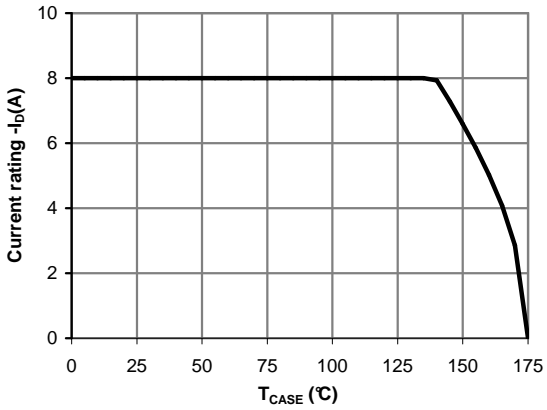


Figure 14: Current De-rating (Note B)

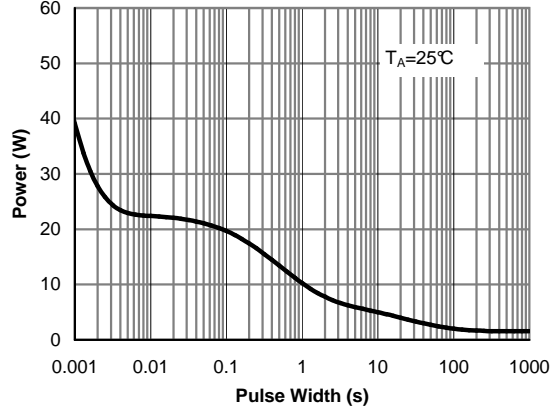


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

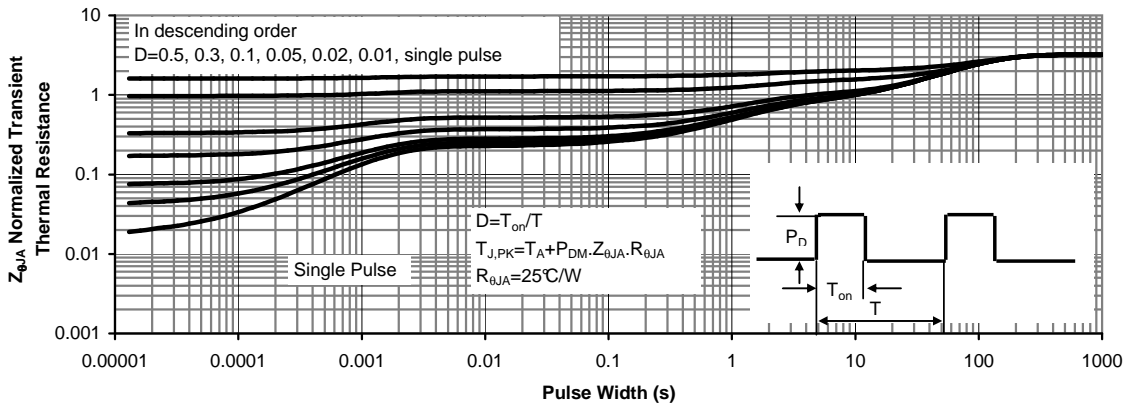
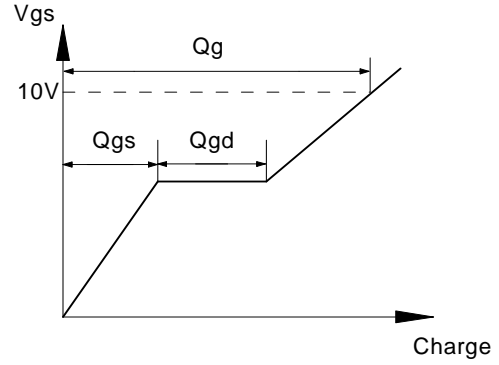
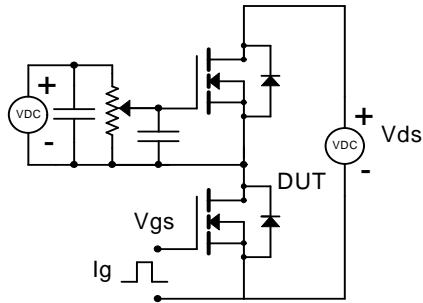


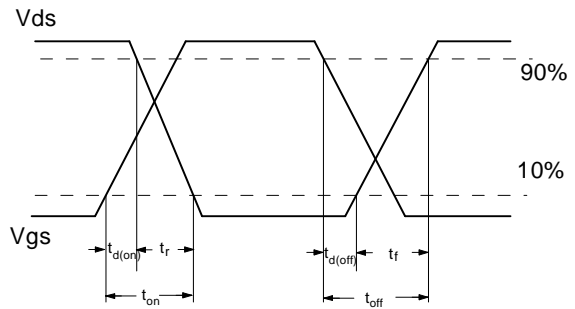
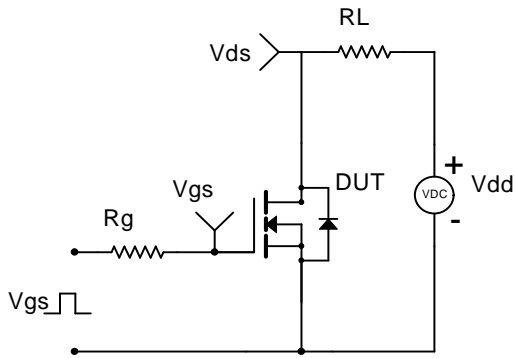
Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

AOD604 N-Channel

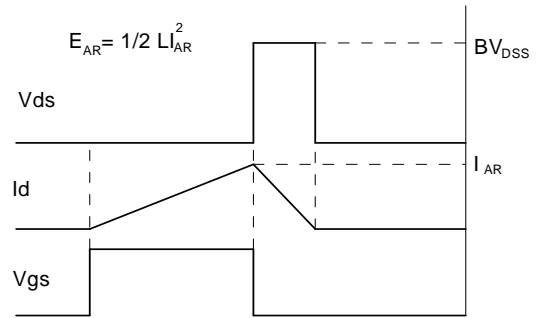
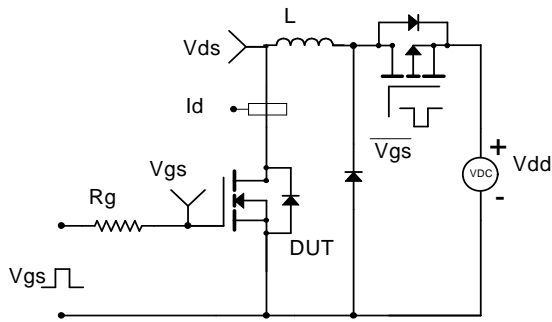
Gate Charge Test Circuit & Waveform



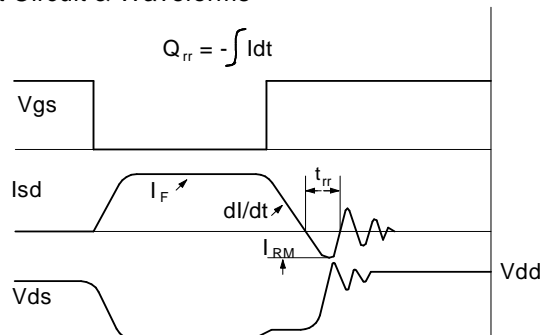
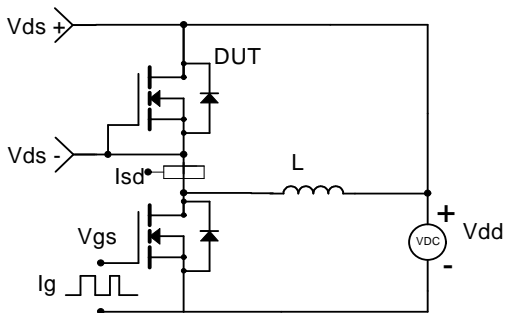
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

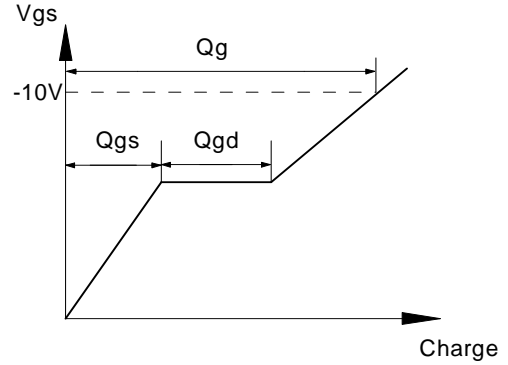
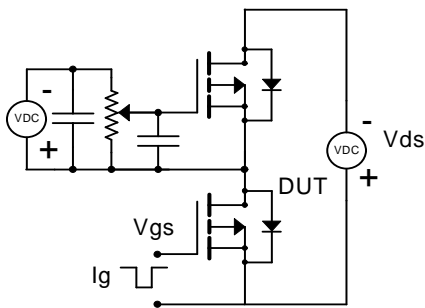


Diode Recovery Test Circuit & Waveforms

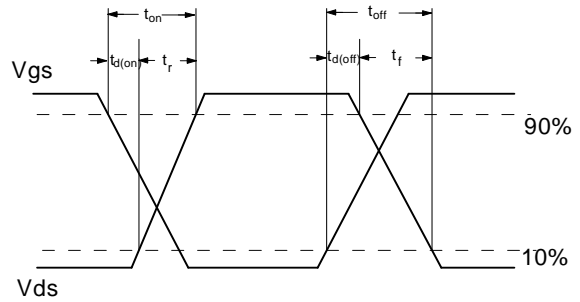
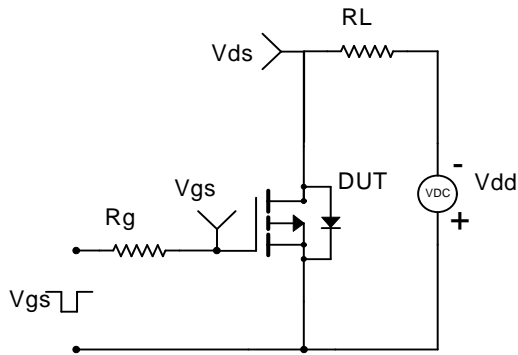


AOD604 P-Channel

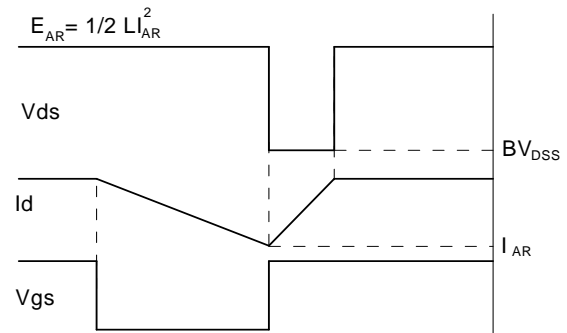
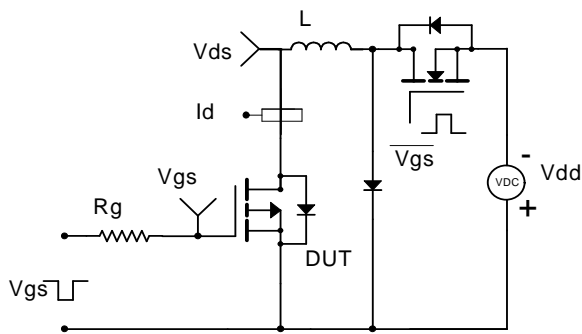
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

