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Cypress Semiconductor
CY2410SXC-5

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CY2410

MPEG Clock Generator with VCXO

Features

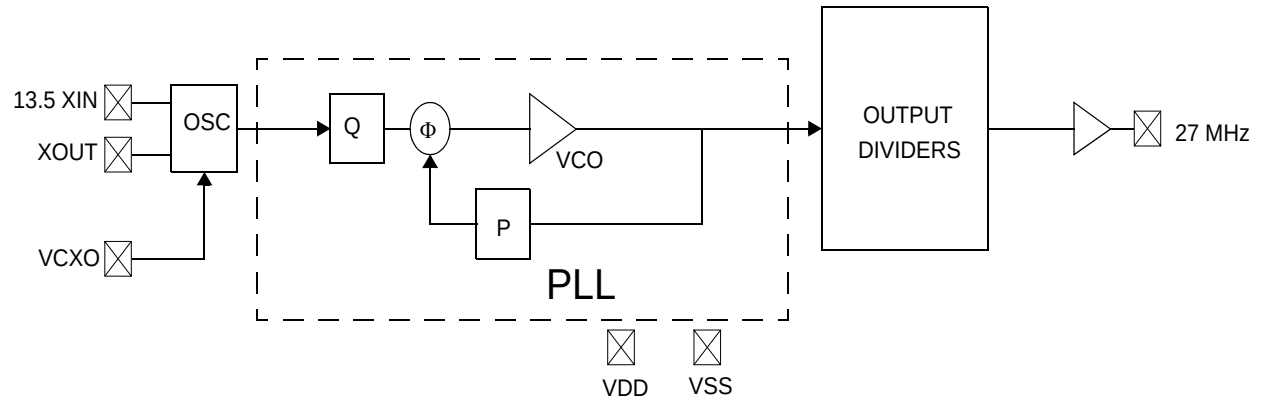
- Integrated phase-locked loop (PLL)
- Low-jitter, high-accuracy outputs
- VCXO with analog adjust
- 3.3V operation
- Compatible with MK3727 (–1, –5)

Benefits

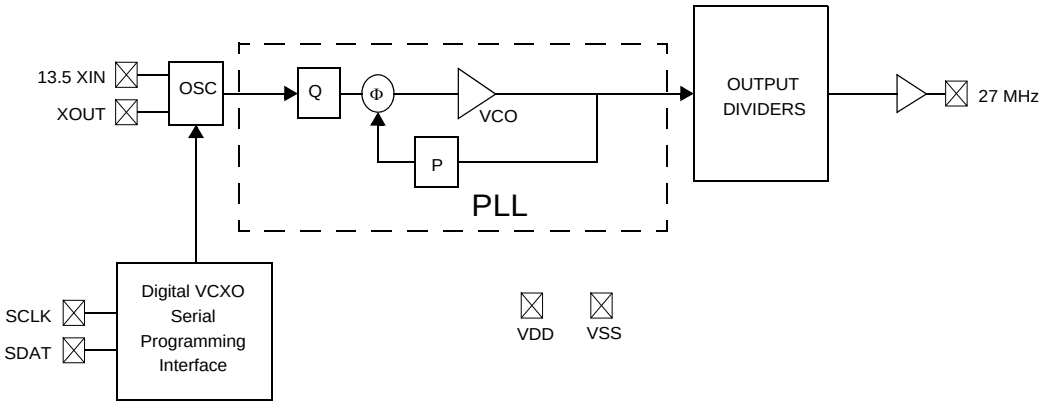
- Highest-performance PLL tailored for multimedia applications
- Meets critical timing requirements in complex system designs
- Large ±150-ppm range, better linearity
- Application compatibility for a wide variety of designs
- Enables design compatibility
- Advanced Features
- Matches nonlinear MK3727A VCXO control curve (-5)
- Digital VCXO control
- Electromagnetic interference (EMI) reduction for standards compliance
- Second source for existing designs

Part Number	Outputs	Input Frequency Range	Output Frequencies	VCXO Control Curve	Other Features
CY2410–1	1	13.5-MHz pullable crystal input per Cypress specification	1 copy of 27 MHz	linear	Compatible with MK3727
CY2410–5	1	13.5-MHz pullable crystal input per Cypress specification	1 copy of 27 MHz	nonlinear	Matches MK3727A nonlinear VCXO Control Curve

CY2410-1, -5 Logic Block Diagram



CY2410-3 Logic Block Diagram



Pin Configuration

Figure 1. CY2410-1, CY2401-5 8-Pin SOIC

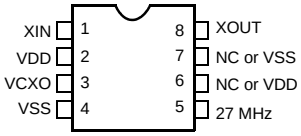


Table 1. Pin Definitions for CY2410–1, –5

Name	Pin Number	Description
X_{IN}	1	Reference crystal input
V_{DD}	2	Voltage supply
V_{CXO}	3	Input analog control for V_{CXO}
V_{SS}	4	Ground
27 MHz	5	27-MHz clock output
NC/V_{DD}	6	No Connect or voltage supply
NC/V_{SS}	7	No Connect or ground
X_{OUT}[1]	8	Reference crystal output

Note
1. Float X_{OUT} if X_{IN} is externally driven.

Pullable Crystal Specifications [2]

Parameter	Description	Condition	Min	Typ.	Max	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	–	13.5	–	MHz
C_{LNOM}	Nominal load capacitance		–	14	–	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	–	–	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec.	3	–	–	
DL	Crystal drive level	No external series resistor assumed	–	0.5	2.0	mW
F_{3SEPHI}	Third overtone separation from $3*F_{NOM}$	High side	300	–	–	ppm
F_{3SEPLO}	Third overtone separation from $3*F_{NOM}$	Low side	–	–	–150	ppm
C_0	Crystal shunt capacitance		–	–	7	pF
C_0/C_1	Ratio of shunt to motional capacitance		180	–	250	
C_1	Crystal motional capacitance		14.4	18	21.6	pF

Note
2. Crystals that meet this specification includes: Ecliptek ECX-5788-13.500M,Siward XTL001050A-13.5-14-400, Raltron A-13.500-14-CL,PDI HA13500XFSA14XC.

Figure 2. Data Valid and Data Transition Periods

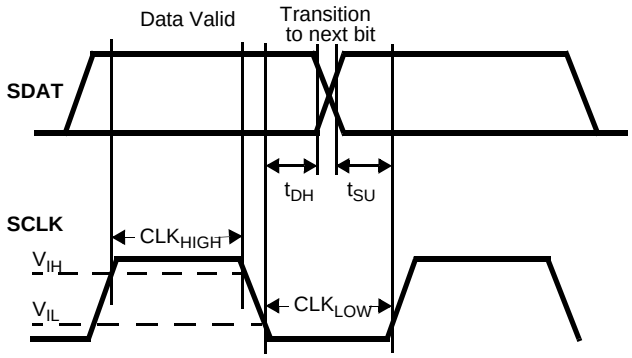


Figure 3. Start and Stop Frame

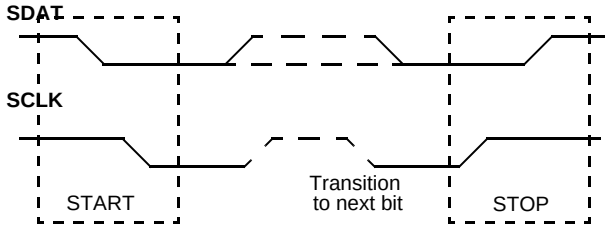


Figure 4. Duty Cycle Definition; DC = t2/t1

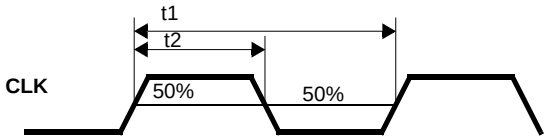
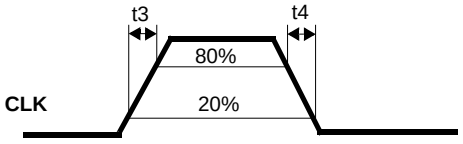


Figure 5. Rise and Fall Time Definitions: ER = 0.6 x VDD / t3, EF = 0.6 x VDD / t4



Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	–0.5	7.0	V
T_S	Storage Temperature[3]	–65	125	°C
T_J	Junction Temperature	–	125	°C
	Digital Inputs	V_{SS} – 0.3	V_{DD} + 0.3	V
	Digital Outputs referred to V_{DD}	V_{SS} – 0.3	V_{DD} + 0.3	V
	Electrostatic Discharge	2000		V

Recommended Operating Conditions

Parameter	Description	Min	Typ.	Max	Unit
V_{DD}	Operating Voltage	3.135	3.3	3.465	V
T_A	Ambient Temperature	0	–	70	°C
C_{LOAD}	Max. Load Capacitance	–	–	15	pF
f_{REF}	Reference Frequency	–	13.5	–	MHz
t_{PU}	Power up time for V_{DD} to reach minimum specified voltage (power ramp must be monotonic)	0.05	–	500	ms

DC Electrical Specifications

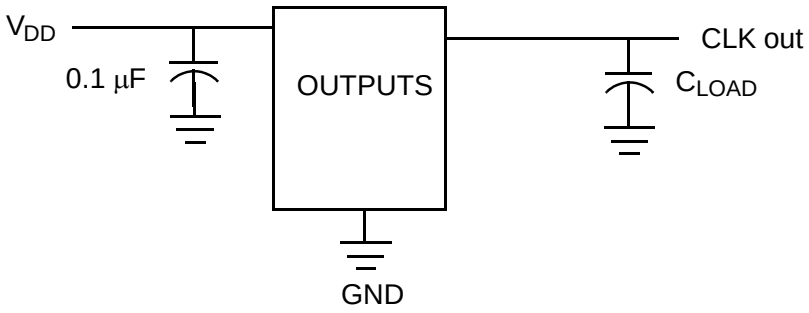
Parameter	Name	Description	Min	Typ.	Max	Unit
I_{OH}	Output HIGH Current –1,–5	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3V$	12	24	–	mA
I_{OL}	Output LOW Current –1,–5	$V_{OL} = 0.5$, $V_{DD} = 3.3V$	12	24	–	mA
C_{IN}	Input Capacitance		–	–	7	pF
I_{IZ}	Input Leakage Current		–	5	–	µA
$f_{\Delta XO}$	V_{CXO} pullability range:–1,–5		±150	–	–	ppm
V_{VCXO}	V_{CXO} input range		0	–	V_{DD}	V
I_{VDD}	Supply Current		–	30	35	mA

AC Electrical Specifications (V_{DD} = 3.3V)[4]

Parameter[4]	Name	Description	Min	Typ.	Max	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 4, 50% of V_{DD}	45	50	55	%
ER_{OR}	Rising Edge Rate –1, –5	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD}, CLOAD = 15 pF See Figure 5.	0.8	1.4	–	V/ns
ER_{OF}	Falling Edge Rate –1, –5	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD}, CLOAD = 15 pF See Figure 5.	0.8	1.4	–	V/ns
t_9	Clock Jitter –1, –5	Peak-to-peak period jitter	–	140	–	ps
t_{10}	PLL Lock Time		–	–	3	ms

Notes
3. Rated for ten years.
4. Not 100% tested.

Figure 6. Test and Measurement Setup

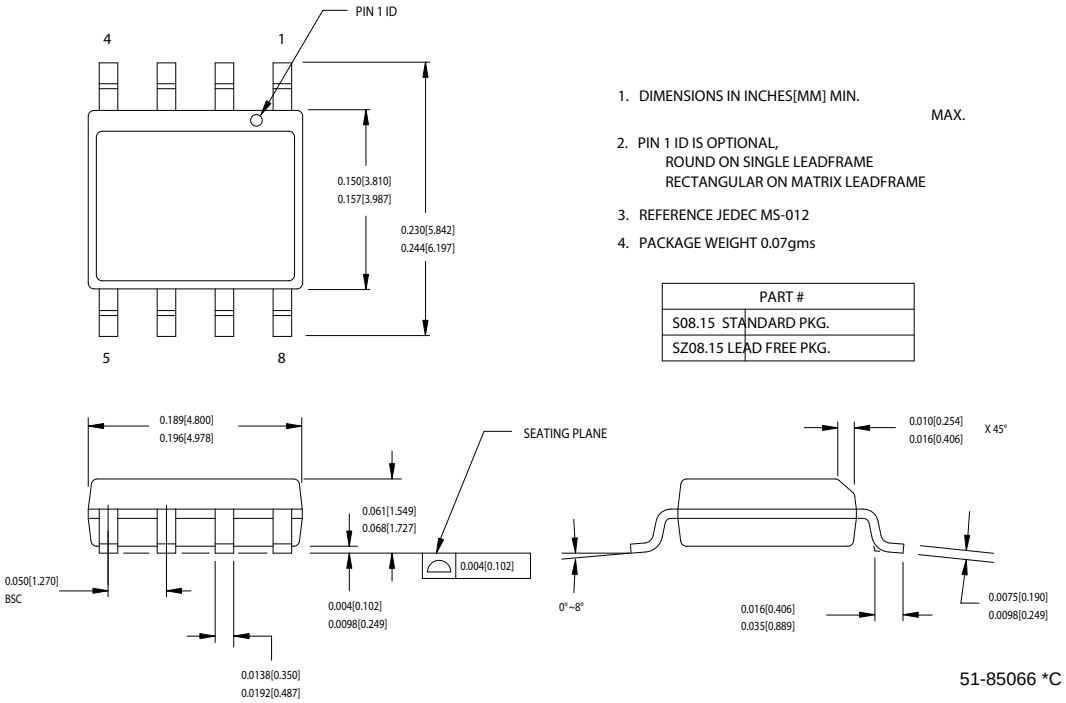


Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage	Features
Pb-Free				
CY2410SXC–1[5]	8-pin SOIC	Commercial	3.3V	Linear VCXO control curve
CY2410SXC–1T[5]	8-pin SOIC - Tape and Reel	Commercial	3.3V	Linear VCXO control curve
CY2410SXC–5[5]	8-pin SOIC	Commercial	3.3V	Matches nonlinear MK3727A VCXO control curve
CY2410SXC–5T[5]	8-pin SOIC - Tape and Reel	Commercial	3.3V	Matches nonlinear MK3727A VCXO control curve
CY2410KSXC–5	8-pin SOIC	Commercial	3.3V	Matches nonlinear MK3727A VCXO control curve
CY2410KSXC–5T	8-pin SOIC - Tape and Reel	Commercial	3.3V	Matches nonlinear MK3727A VCXO control curve

Package Drawing and Dimensions

Figure 7. 8-Lead (150-Mil) SOIC



Note
5. Not recommended for new designs.

Document History Page

Document Title: CY2410 MPEG Clock Generator with VCXO Document Number: 38-07317				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	111553	02/12/02	CKN	New Data Sheet
*A	114937	09/24/02	CKN	Added -6 to data sheet, Advance Information to Final
*B	121418	12/06/02	CKN	Updated the Pullable Crystal Specifications table on page 2
*C	126905	06/17/03	RGL	Added -7 part to data sheet Added new parameter on the Pullable Crystal table Power up requirements added to the operating conditions
*D	131100	01/20/03	RGL	Added VCXO –7 pullability range in the DC Specs with min. value of ±115ppm
*E	2440886	See ECN	AESA	Updated template. Added Note “Not recommended for new designs.” Added part number CY2410SXC-1, CY2410SXC-1T, CY2410SXC-5, CY2410SXC-5T, CY2410KSXC–5, and CY2410KSXC–5T in ordering information table. Removed all part numbers for non-Pb-free packages (part numbers beginning CY2410SC). Removed details specific to the -3, -4, -6 and -7 versions.

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