Excellent Integrated System Limited

Stocking Distributor

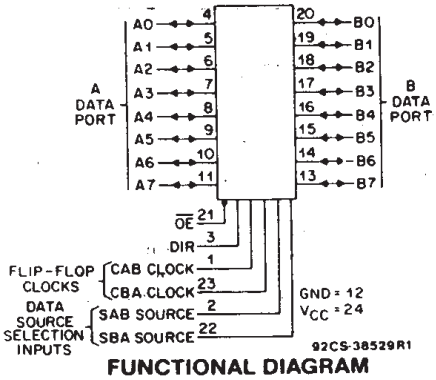
Click to view price, real time Inventory, Delivery & Lifecycle Information:

Texas Instruments
CD74AC646MG4

For any questions, you can email us directly:
sales@integrated-circuit.com

CD54/74AC646, CD54/74AC648
CD54/74ACT646, CD54/74ACT648

Data sheet acquired from Harris Semiconductor
SCHS293



FUNCTIONAL DIAGRAM

Octal-Bus Transceiver/Registers, 3-State

CD54/74AC/ACT646 - Non-Inverting
CD54/74AC/ACT648 - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 5.3 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC646 and CD54/74AC648 and the CD54/74ACT646 and CD54/74ACT648 3-state, octal-bus transceiver/registers use the RCA ADVANCED CMOS technology. The CD54/74AC648 and CD54/74ACT648 have inverting outputs. The CD54/74AC646 and CD54/74ACT646 have non-inverting outputs. These devices are bus transceivers with D-type flip-flops which act as internal storage registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Output Enable ($\overline{OE}$) and Direction (DIR) inputs control the transceiver functions. Data present at the high-impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The Select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The Direction control determines which data bus will receive data when the Output Enable ($\overline{OE}$) is LOW. In the high-impedance mode (Output Enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the Direction (DIR) and Output Enable ($\overline{OE}$) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

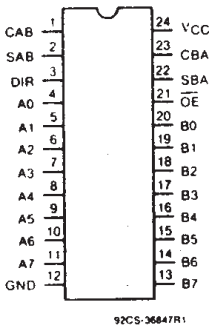
The CD74AC/ACT646 and CD74AC/ACT648 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 o +125°C).

The CD54AC/ACT646 and CD54AC/ACT648, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.



TERMINAL ASSIGNMENT

This data sheet is applicable to the CD74AC646 and CD74ACT646. The CD54AC646, CD54/74AC648, CD54ACT646, and CD54/74ACT648 were not acquired from Harris Semiconductor.

File Number **1970**

CD54/74AC646, CD54/74AC648
CD54/74ACT646, CD54/74ACT648

FUNCTION TABLE

INPUTS						DATA I/O#		OPERATION OR FUNCTION	
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	646	648
X	X	↓	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↓	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↓	↓	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

#The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
To prevent excess currents in the High-Z modes, all I/O terminals should be terminated with 10 kΩ resistors.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

9

CD54/74AC646, CD54/74AC648
CD54/74ACT646, CD54/74ACT648

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O= V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC646, CD54/74AC648
CD54/74ACT646, CD54/74ACT648

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C +25 MIN.	+25 MAX.	-40 to +85 MIN.	-40 to +85 MAX.	-55 to +125 MIN.	-55 to +125 MAX.	UNITS
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O= V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
DIR	0.67
$\overline{OE}$	1.17
An, Bn	0.4

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

9

CD54/74AC646, CD54/74AC648
CD54/74ACT646, CD54/74ACT648

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f_{max}	1.5 3.3* 5†	11 101 143	— — —	10 89 125	— — —	MHz
Setup Time Data to Clock	t_{su}	1.5 3.3 5	27 3.1 2.2	— — —	31 3.5 2.5	— — —	ns
Hold Time Data to Clock	t_H	1.5 3.3 5	2 2 2	— — —	2 2 2	— — —	ns
Clock Pulse Width	t_w	1.5 3.3 5	44 4.9 3.5	— — —	50 5.6 4	— — —	ns

*3.3 V: min. is @ 3 V
†5 V: min is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Store A Data to B Bus Store B Data to A Bus 646	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 4.8 3.5	154 17.1 12.3	— 4.7 3.4	169 18.9 13.5	ns
Store $\overline{A}$ Data to B Bus Store $\overline{B}$ Data to A Bus 648	t_{PLH} t_{PHL}	1.5 3.3 5	— 4.8 3.5	154 17.1 12.3	— 4.7 3.4	169 18.9 13.5	ns
A Data to B Bus B Data to A Bus 646	t_{PLH} t_{PHL}	1.5 3.3 5	— 4 2.8	125 14 10	— 3.9 2.8	138 15.4 11	ns
$\overline{A}$ Data to B Bus $\overline{B}$ Data to A Bus 648	t_{PLH} t_{PHL}	1.5 3.3 5	— 4 2.8	125 14 10	— 3.9 2.8	138 15.4 11	ns
Select to Data 646	t_{PLH} t_{PHL}	1.5 3.3 5	— 4.3 3.1	136 15.3 10.9	— 4.2 3	150 16.8 12	ns
Select to Data 648	t_{PLH} t_{PHL}	1.5 3.3 5	— 4.3 3.1	136 15.3 10.9	— 4.2 3	150 16.8 12	ns
3-State Enabling/ Disabling Time Bus to Output or Register to Output	t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	1.5 3.3 5	— 5.2 3.5	154 18.4 12.3	— 5.1 3.4	169 20.2 13.5	ns
Power Dissipation Capacitance	C_{PD}§	—	150 Typ.		150 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V
†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 C_{PD} f_i + \Sigma (V_{CC}^2 C_L f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

CD54/74AC646, CD54/74AC648
CD54/74ACT646, CD54/74ACT648

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f_{max}	5*	125	—	110	—	MHz
Setup Time Data to Clock	t_{SU}	5	2.2	—	2.5	—	ns
Hold Time Data to Clock	t_H	5	2	—	2	—	ns
Clock Pulse Width	t_W	5	3.9	—	4.5	—	ns

*5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Store A Data to B Bus, Store B Data to A Bus — 646	t_{PLH} t_{PHL}	5*	4	14.1	3.9	15.5	ns
Store $\overline{A}$ Data to B Bus, Store $\overline{B}$ Data to A Bus — 648	t_{PLH} t_{PHL}	5	4	14.1	3.9	15.5	ns
A Data to B Bus, B Data to A Bus — 646	t_{PLH} t_{PHL}	5	3.2	11.4	3.1	12.5	ns
$\overline{A}$ Data to B Bus, $\overline{B}$ Data to A Bus — 648	t_{PLH} t_{PHL}	5	3.2	11.4	3.1	12.5	ns
Select to Data — 646	t_{PLH} t_{PHL}	5	3.7	13.2	3.6	14.5	ns
Select to Data — 648	t_{PLH} t_{PHL}	5	4	14.1	3.9	15.5	ns
3-State Enabling/ Disabling Time Bus to Output or Register to Output	t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	5	4	14.1	3.9	15.5	ns
Power Dissipation Capacitance	C_{PD}§	—	150 Typ.		150 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC}\Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

9

CD54/74AC646, CD54/74AC648
CD54/74ACT646, CD54/74ACT648

PARAMETER MEASUREMENT INFORMATION

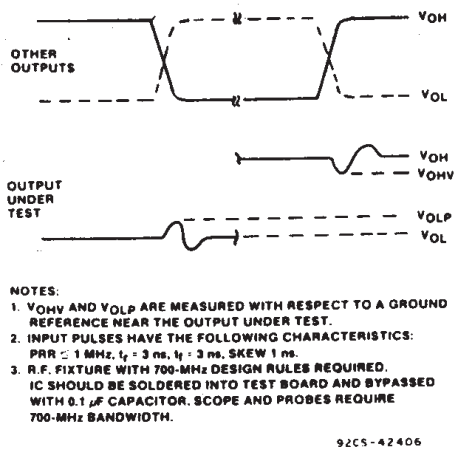


Fig. 1 - Simultaneous switching transient waveforms.

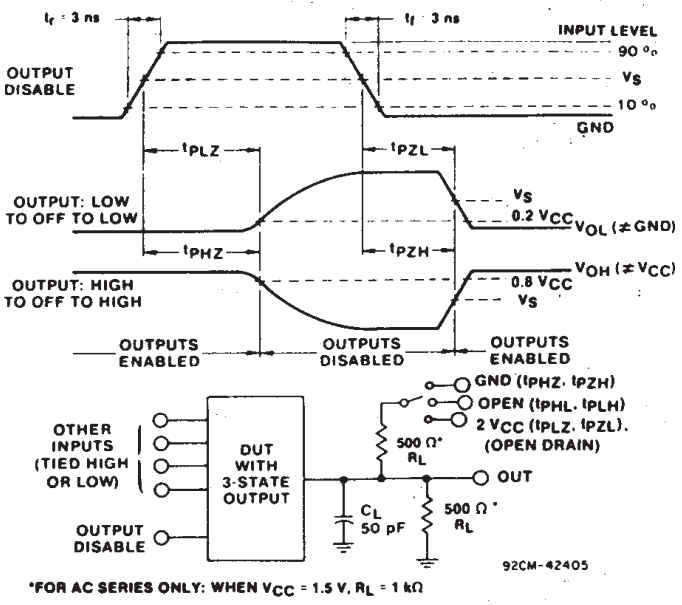


Fig. 2 - Three-state propagation delay waveforms and test circuit.

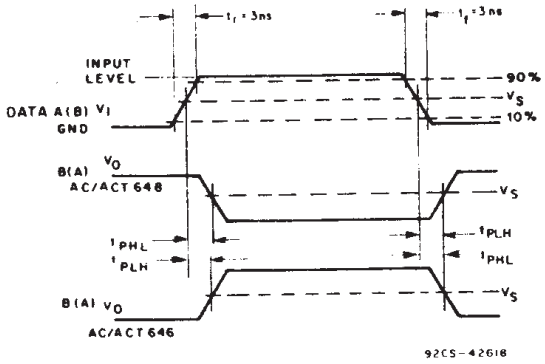


Fig. 3 - Propagation delay times.

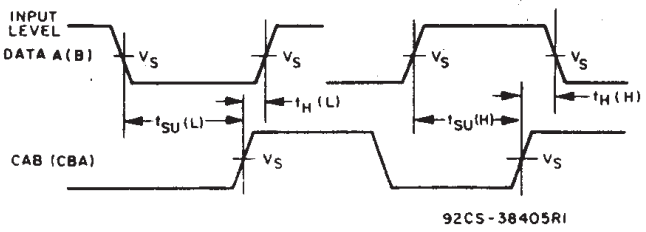


Fig. 4 - Data setup and hold times.

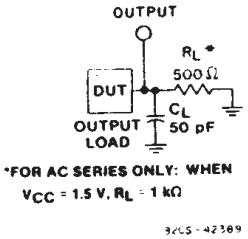


Fig. 5 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74AC646M	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC646M	Samples
CD74AC646M96	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC646M	Samples
CD74AC646MG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC646M	Samples
CD74ACT646M	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT646M	Samples
CD74ACT646M96	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT646M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

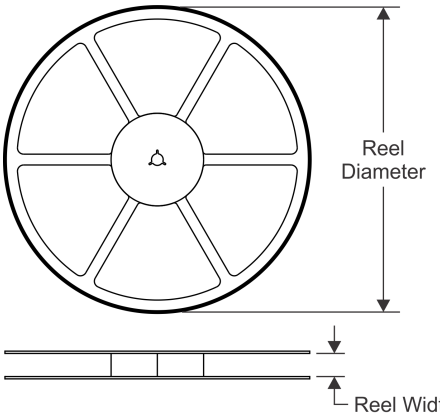
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

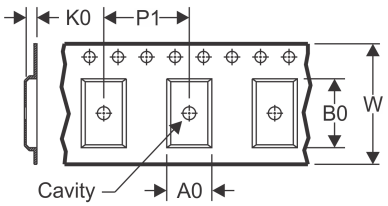
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

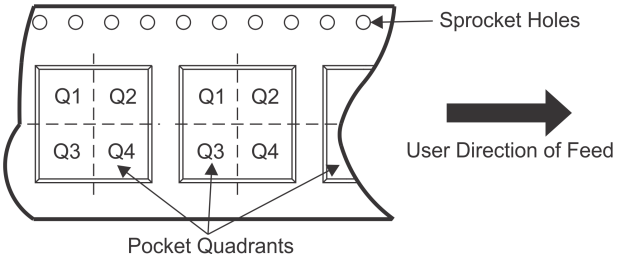


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

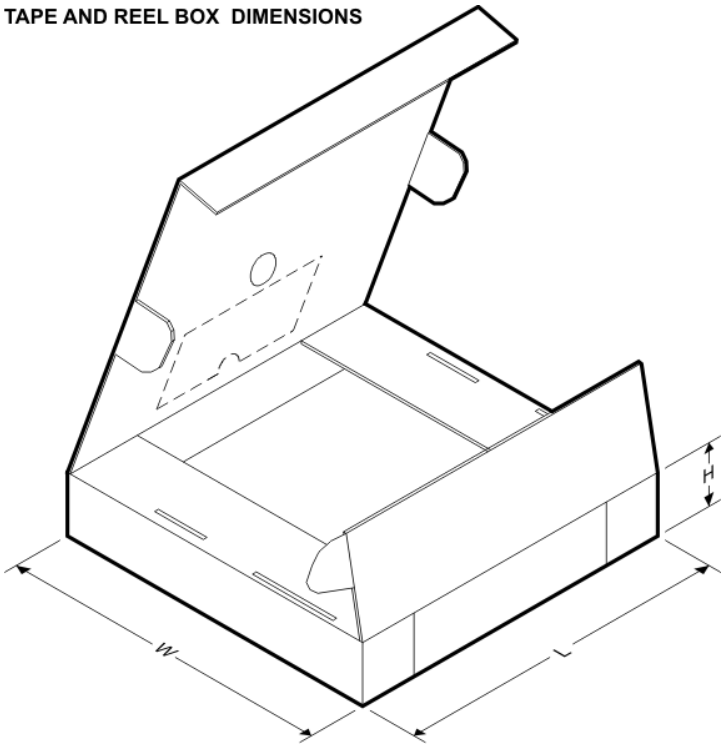


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC646M96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD74ACT646M96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

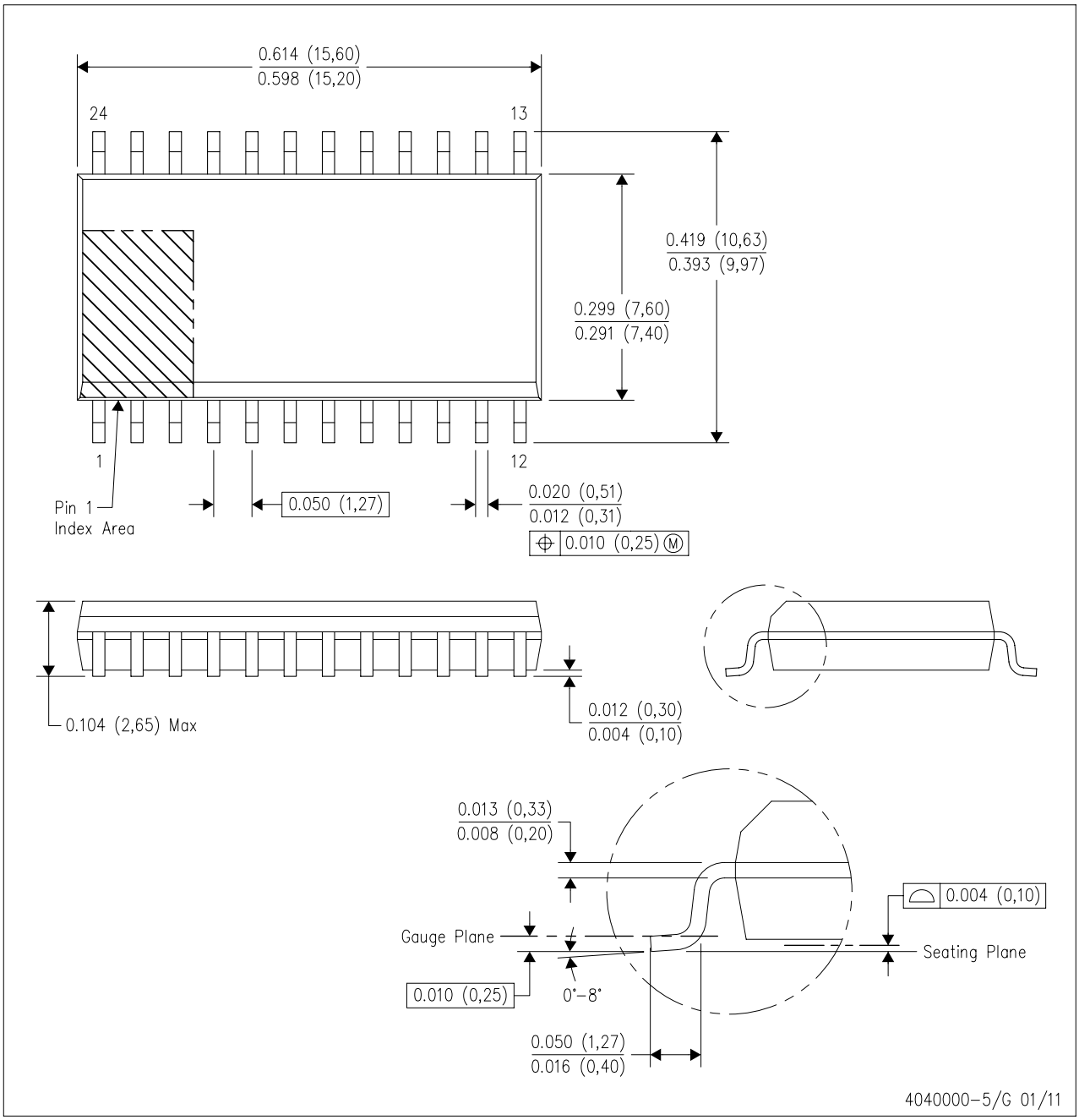


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC646M96	SOIC	DW	24	2000	367.0	367.0	45.0
CD74ACT646M96	SOIC	DW	24	2000	367.0	367.0	45.0

MECHANICAL DATA

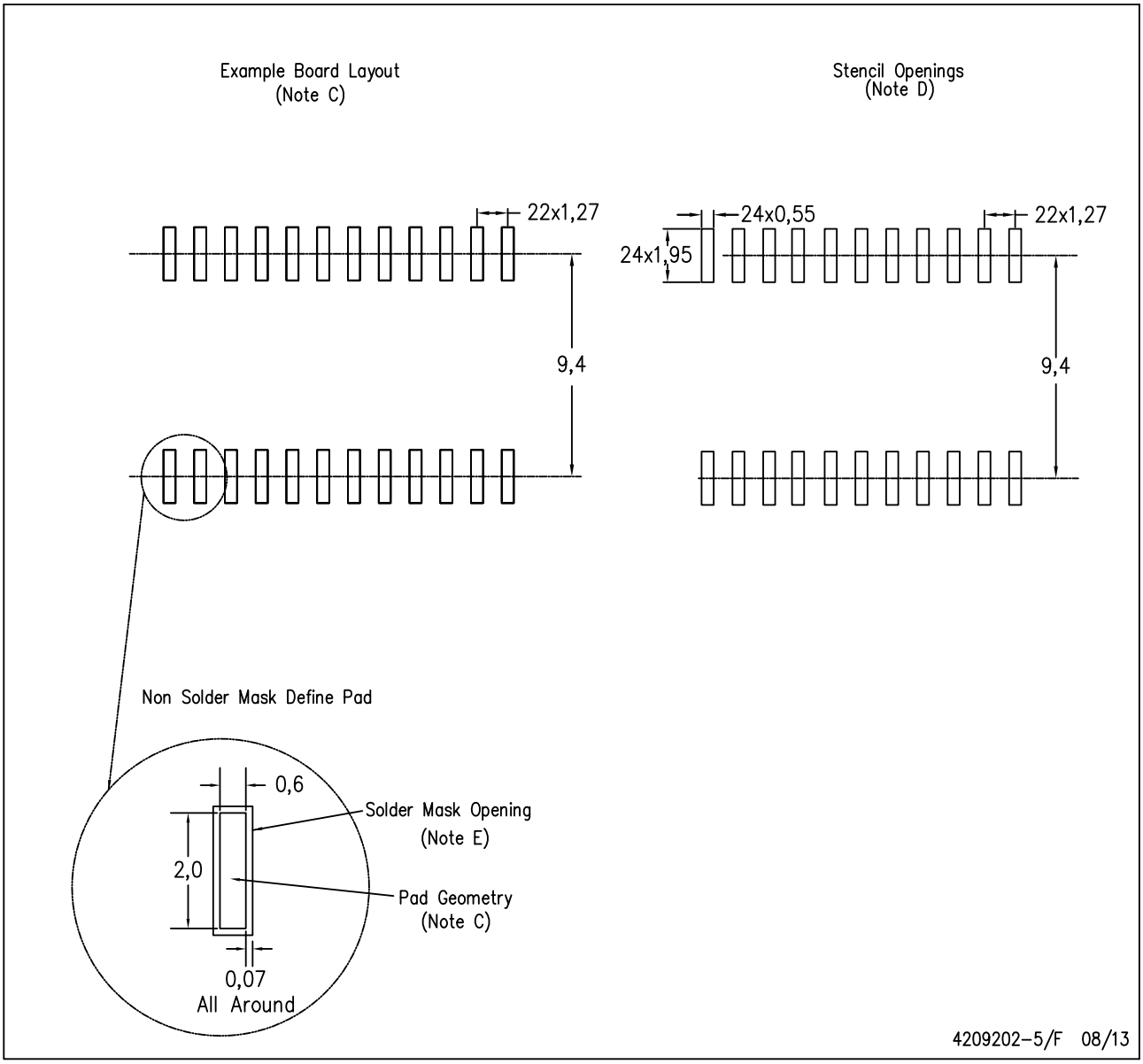
DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

LAND PATTERN DATA

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265