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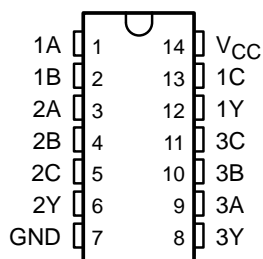
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SN54ALS11A, SN54AS11, SN74ALS11A, SN74AS11 TRIPLE 3-INPUT POSITIVE-AND GATES

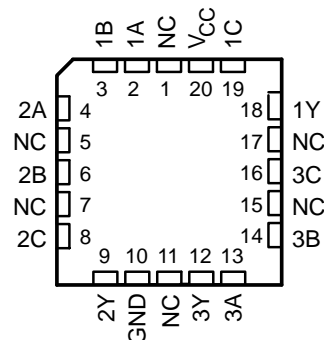
SDAS009D – MARCH 1984 – REVISED NOVEMBER 2002

- 4.5-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 5.5 ns at 5 V

SN54ALS11A, . . . J OR W PACKAGE
SN54AS11 . . . J PACKAGE
SN74ALS11A, SN74AS11 . . . D, N, OR NS PACKAGE
(TOP VIEW)



SN54ALS11A, SN54AS11 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain three independent 3-input positive-AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	PDIP – N	Tube	SN74ALS11AN	SN74ALS11AN	
			SN74AS11N	SN74AS11N	
	SOIC – D	Tube	SN74ALS11AD	ALS11A	
			Tape and reel		SN74ALS11ADR
			Tube	SN74AS11D	AS11
				Tape and reel	
SOP – NS	Tape and reel	SN74ALS11ANSR	ALS11A		
		SN74AS11NSR	74AS11		
–55°C to 125°C	CDIP – J	Tube	SNJ54ALS11AJ	SNJ54ALS11AJ	
			SNJ54AS11J	SNJ54AS11J	
	CFP – W	Tube	SNJ54ALS11AW	SNJ54ALS11AW	
	LCCC – FK	Tube	SNJ54ALS11AFK	SNJ54ALS11AFK	
SNJ54AS11FK			SNJ54AS11FK		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

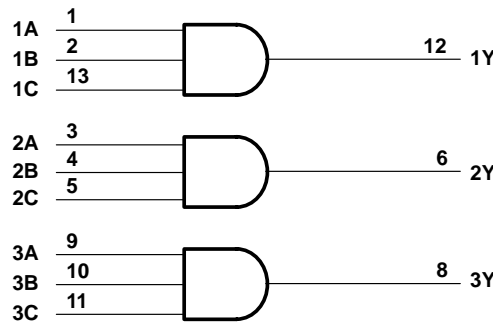
SN54ALS11A, SN54AS11, SN74ALS11A, SN74AS11
TRIPLE 3-INPUT POSITIVE-AND GATES

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FUNCTION TABLE
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic diagram, each gate (positive logic)



Pin numbers shown are for the D, J, N, NS, and W packages.

absolute maximum ratings over operating free-air temperature range (SN54ALS11A, SN74ALS11A) (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Package thermal impedance, θ_{JA} (see Note 1): D package	86°C/W
N package	80°C/W
NS package	76°C/W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

	SN54ALS11A			SN74ALS11A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage	0.8‡			0.8			V
	0.7§						
I_{OH} High-level output current	-0.4			-0.4			mA
I_{OL} Low-level output current	4			8			mA
T_A Operating free-air temperature	-55		125	0		70	°C

‡ Applies over temperature range -55°C to 70°C

§ Applies over temperature range 70°C to 125°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ALS11A, SN54AS11, SN74ALS11A, SN74AS11 TRIPLE 3-INPUT POSITIVE-AND GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS11A			SN74ALS11A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$		$V_{CC} - 2$			$V_{CC} - 2$		V
V_{OL}	$V_{CC} = 4.5\text{ V}$		0.25	0.4		0.25	0.4	V
		$I_{OL} = 4\text{ mA}$				0.35	0.5	
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			20			20	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$			-0.1			-0.1	mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	-20		-112	-30		-112	mA
I_{CCH}	$V_{CC} = 5.5\text{ V}$, $V_I = 4.5\text{ V}$		1	1.8		1	1.8	mA
I_{CCL}	$V_{CC} = 5.5\text{ V}$, $V_I = 0$		1.6	3		1.6	3	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V TO }5.5\text{ V}$, $C_L = 50\text{ PF}$, $R_L = 500\ \Omega$, $T_A = \text{MIN TO MAX}\S$				UNIT
			SN54ALS11A		SN74ALS11A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	Y	2	14	2	13	ns
t_{PHL}			2	12.5	2	10	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (SN54AS11, SN74AS11) (unless otherwise noted)¶

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Package thermal impedance, θ_{JA} (see Note 1): D package	86°C/W
N package	80°C/W
NS package	76°C/W
Storage temperature range	-65°C to 150°C

¶ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

SN54ALS11A, SN54AS11, SN74ALS11A, SN74AS11
TRIPLE 3-INPUT POSITIVE-AND GATES

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recommended operating conditions (see Note 2)

		SN54AS11			SN74AS11			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage	0.8			0.8			V
I _{OH}	High-level output current	-2			-2			mA
I _{OL}	Low-level output current	20			20			mA
T _A	Operating free-air temperature	-55		125	0		70	°C

 NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS11			SN74AS11			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA	-1.2			-1.2			V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA	V _{CC} -2			V _{CC} -2			V
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 20 mA	0.35		0.5	0.35		0.5	V
I _I	V _{CC} = 5.5 V, V _I = 7 V	0.1			0.1			mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V	20			20			μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V	-0.5			-0.5			mA
I _{O‡}	V _{CC} = 5.5 V, V _O = 2.25 V	-30		-112	-30		-112	mA
I _{CCH}	V _{CC} = 5.5 V, V _I = 4.5 V	4.3		7	4.3		7	mA
I _{CCL}	V _{CC} = 5.5 V, V _I = 0	11.2		18	11.2		18	mA

 † All typical values are at V_{CC} = 5 V, T_A = 25°C.

 ‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

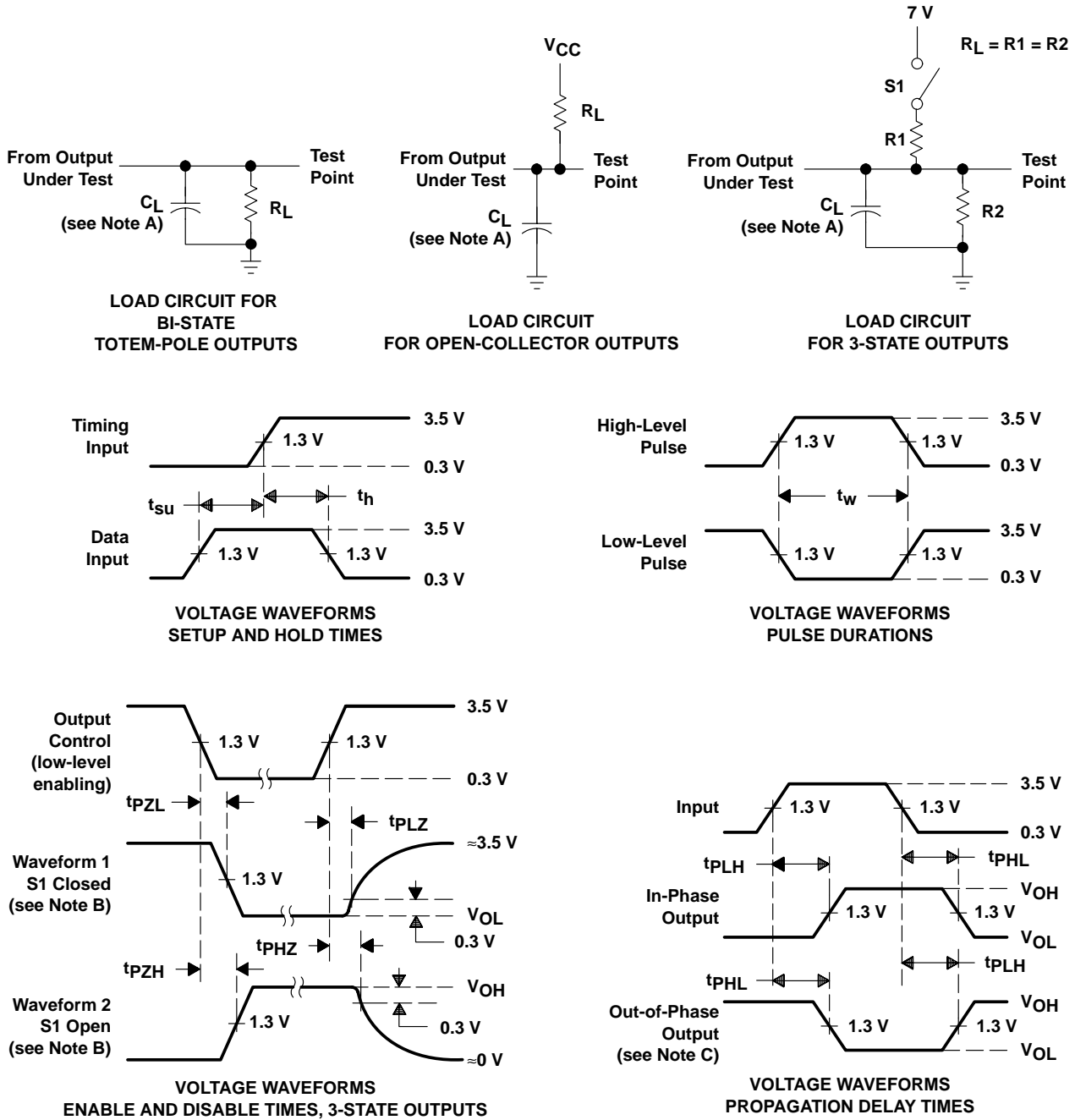
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V TO 5.5 V, C _L = 50 PF, R _L = 500 Ω, T _A = MIN TO MAX§				UNIT
			SN54AS11		SN74AS11		
			MIN	MAX	MIN	MAX	
t _{PLH}	A, B, or C	Y	1	6.5	1	6	ns
t _{PHL}			1	6.5	1	5.5	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN54ALS11A, SN54AS11, SN74ALS11A, SN74AS11
TRIPLE 3-INPUT POSITIVE-AND GATES**

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**PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-86841012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-86841012A SNJ54ALS11AFK	Samples
5962-8684101CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8684101CA SNJ54ALS11AJ	Samples
5962-8684101DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8684101DA SNJ54ALS11AW	Samples
5962-9756101QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9756101QC A SNJ54AS11J	Samples
JM38510/37402BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 37402BCA	Samples
M38510/37402BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 37402BCA	Samples
SN54ALS11AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54ALS11AJ	Samples
SN54AS11J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54AS11J	Samples
SN74ALS11AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS11A	Samples
SN74ALS11ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS11A	Samples
SN74ALS11ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS11A	Samples
SN74ALS11ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS11A	Samples
SN74ALS11AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS11AN	Samples
SN74ALS11ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS11A	Samples
SN74AS11D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS11	Samples
SN74AS11N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS11N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54ALS11AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-86841012A SNJ54ALS11AFK	Samples
SNJ54ALS11AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8684101CA SNJ54ALS11AJ	Samples
SNJ54ALS11AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8684101DA SNJ54ALS11AW	Samples
SNJ54AS11J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9756101QC A SNJ54AS11J	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



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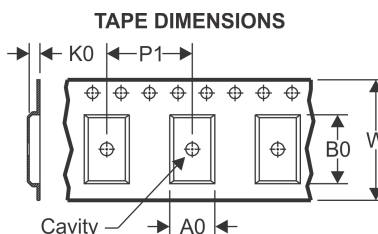
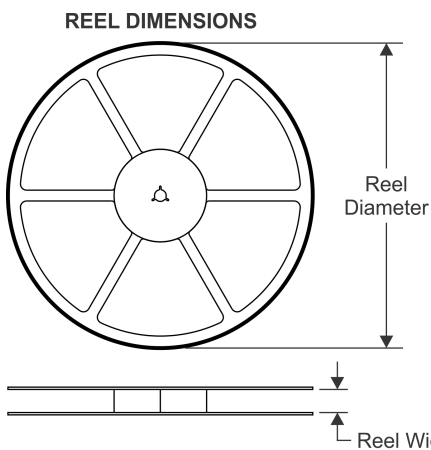
OTHER QUALIFIED VERSIONS OF SN54ALS11A, SN54AS11, SN74ALS11A, SN74AS11 :

- Catalog: [SN74ALS11A](#), [SN74AS11](#)
- Military: [SN54ALS11A](#), [SN54AS11](#)

NOTE: Qualified Version Definitions:

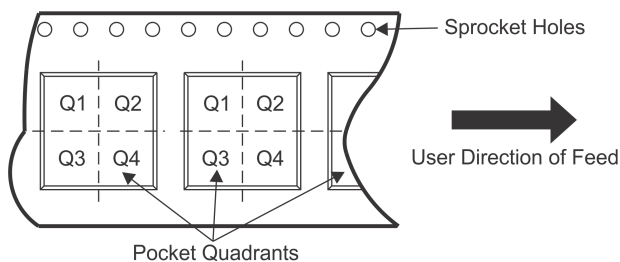
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

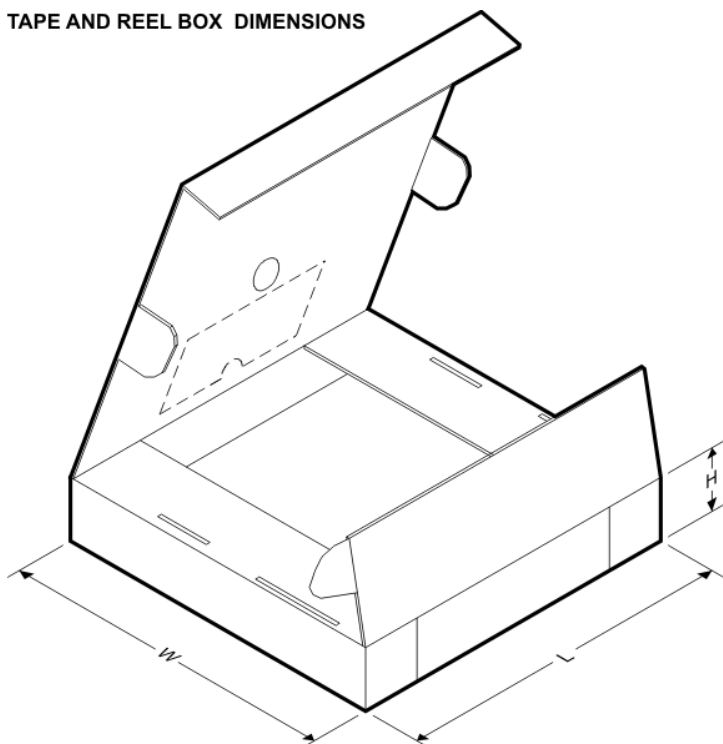
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS11ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ALS11ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



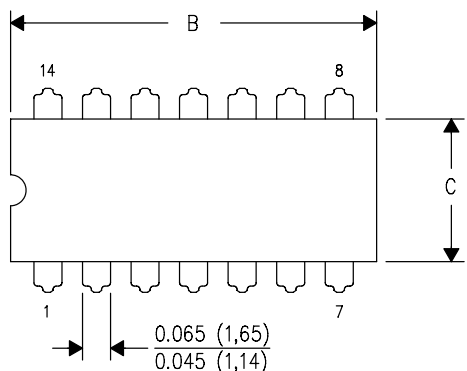
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS11ADR	SOIC	D	14	2500	367.0	367.0	38.0
SN74ALS11ANSR	SO	NS	14	2000	367.0	367.0	38.0

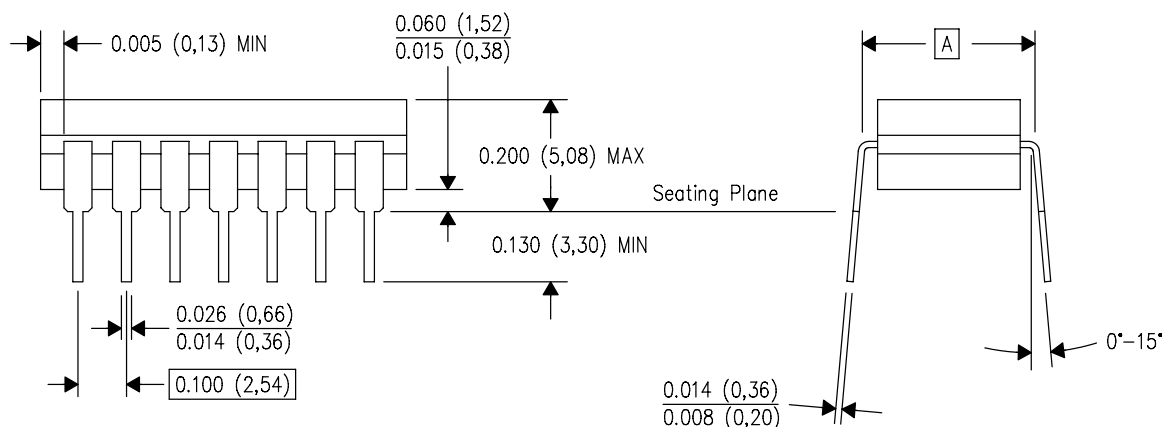
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



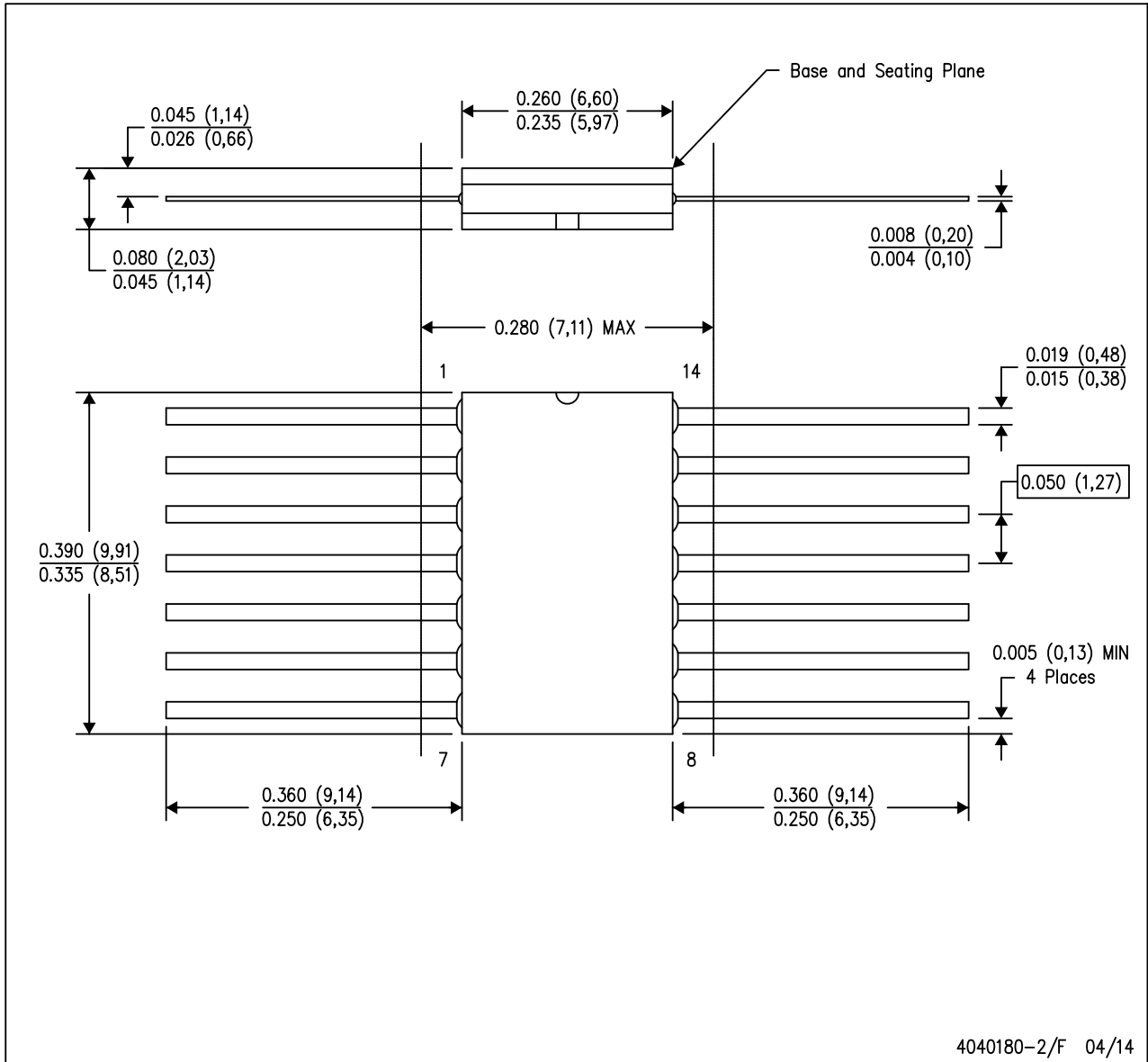
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

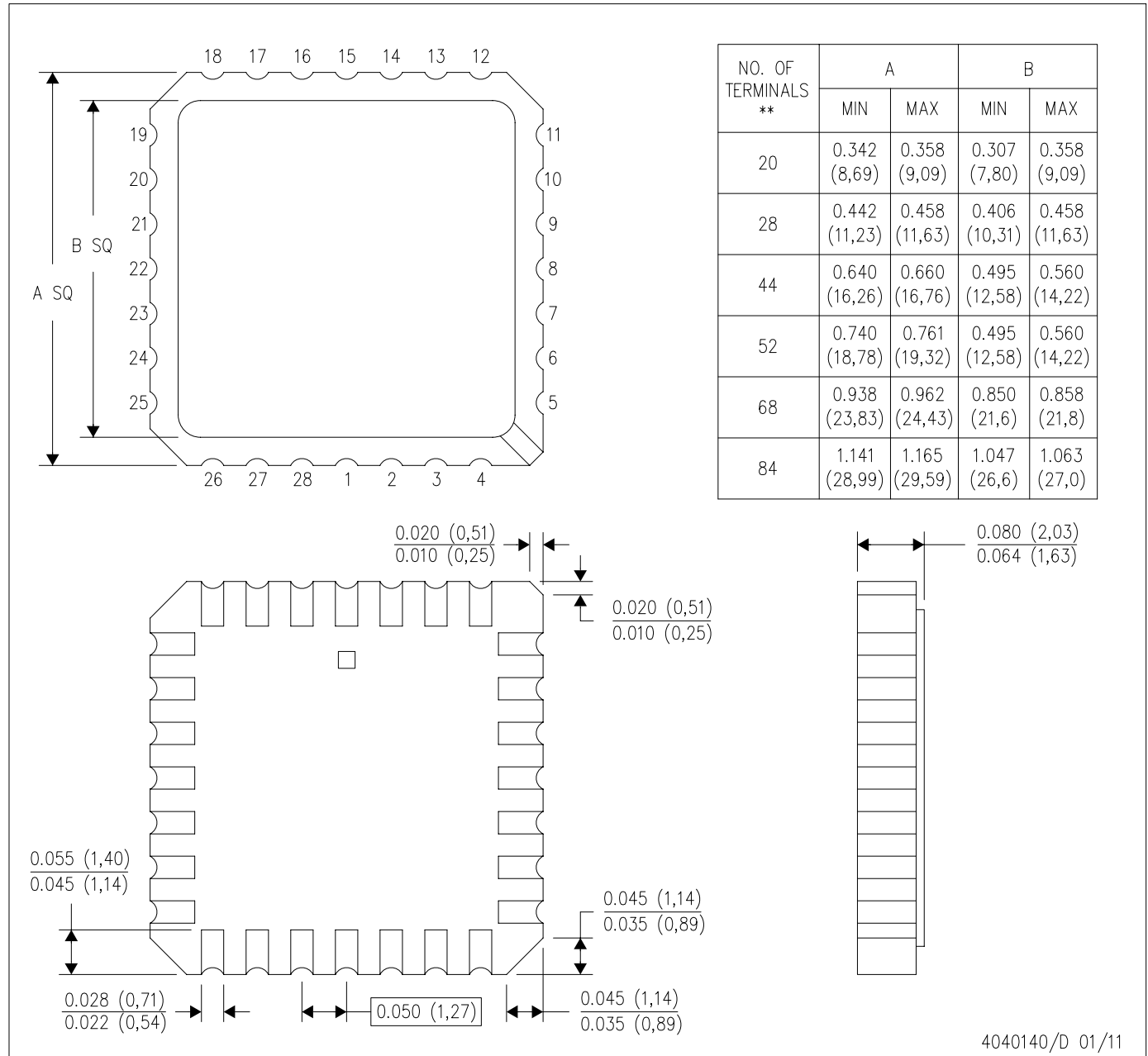


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 01/11

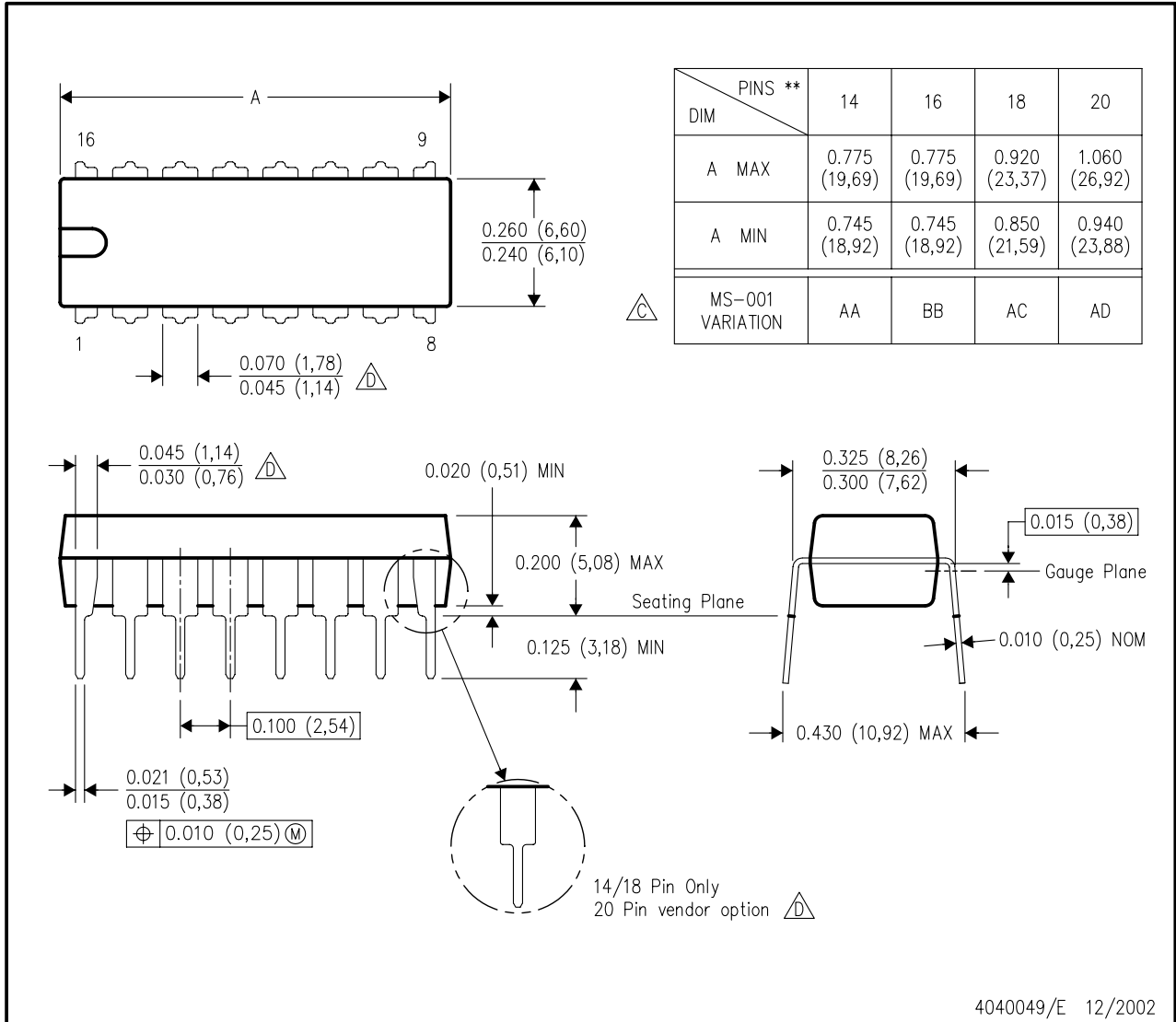
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

N (R-PDIP-T)**

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



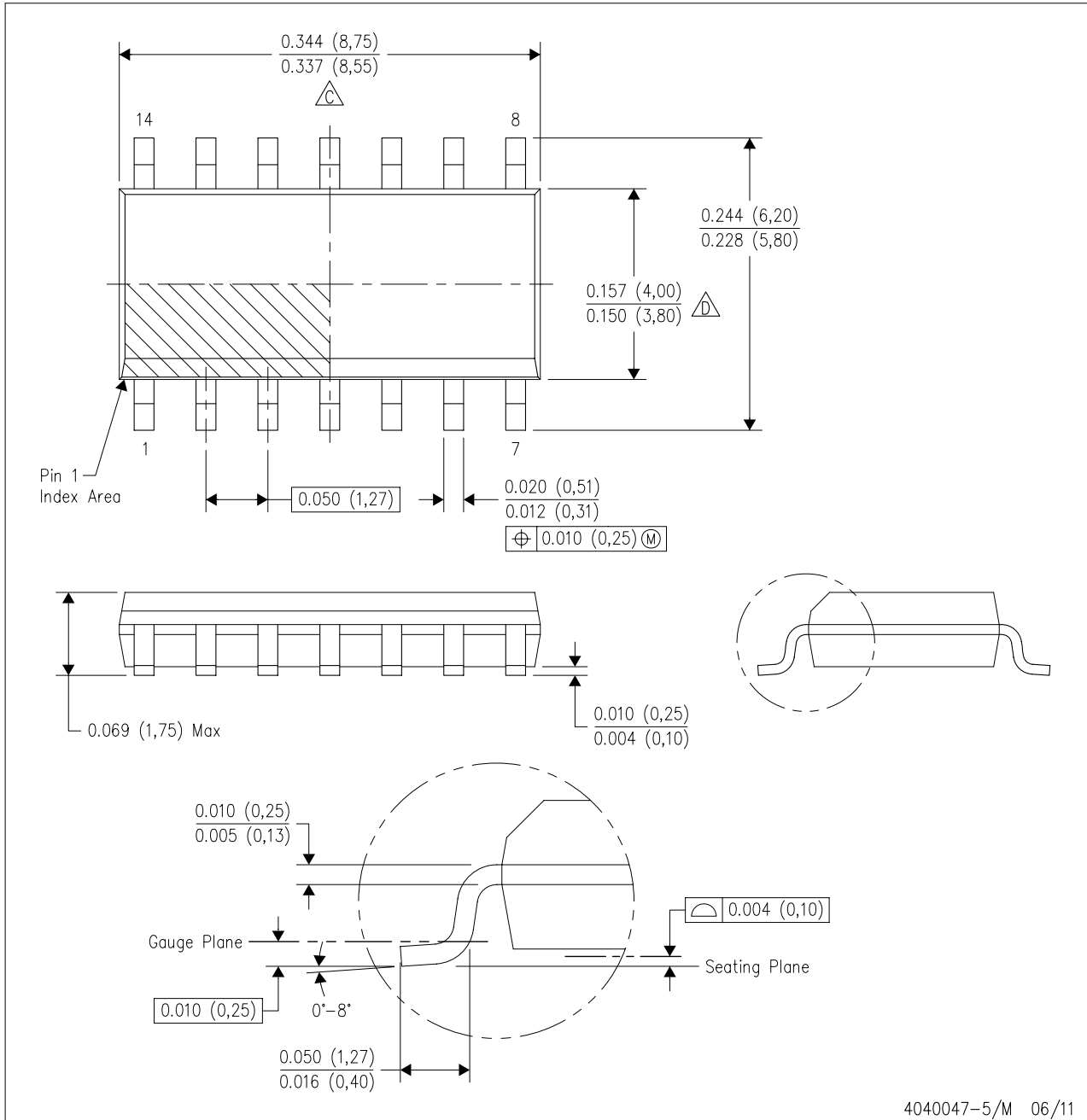
4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



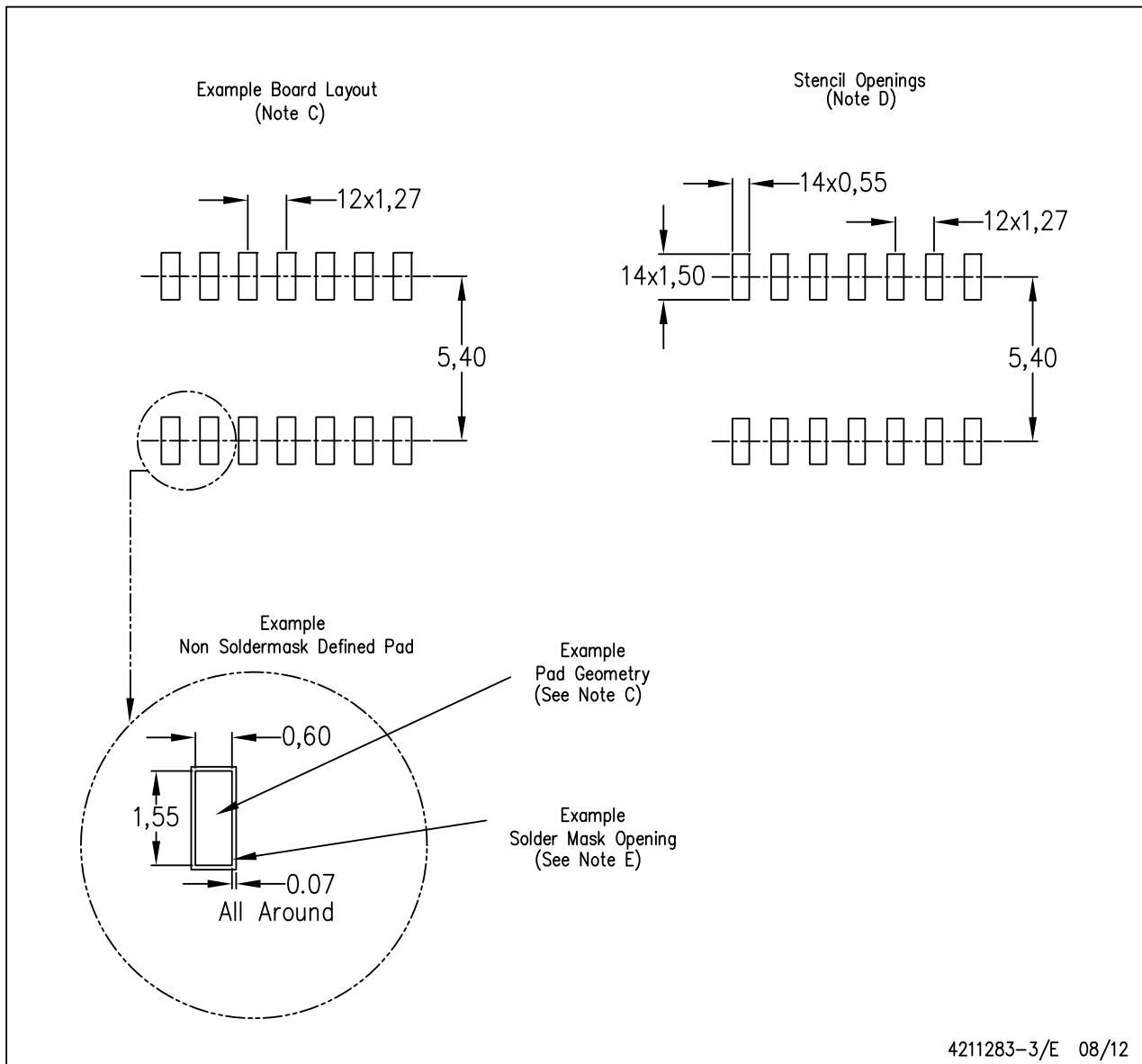
4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

LAND PATTERN DATA

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

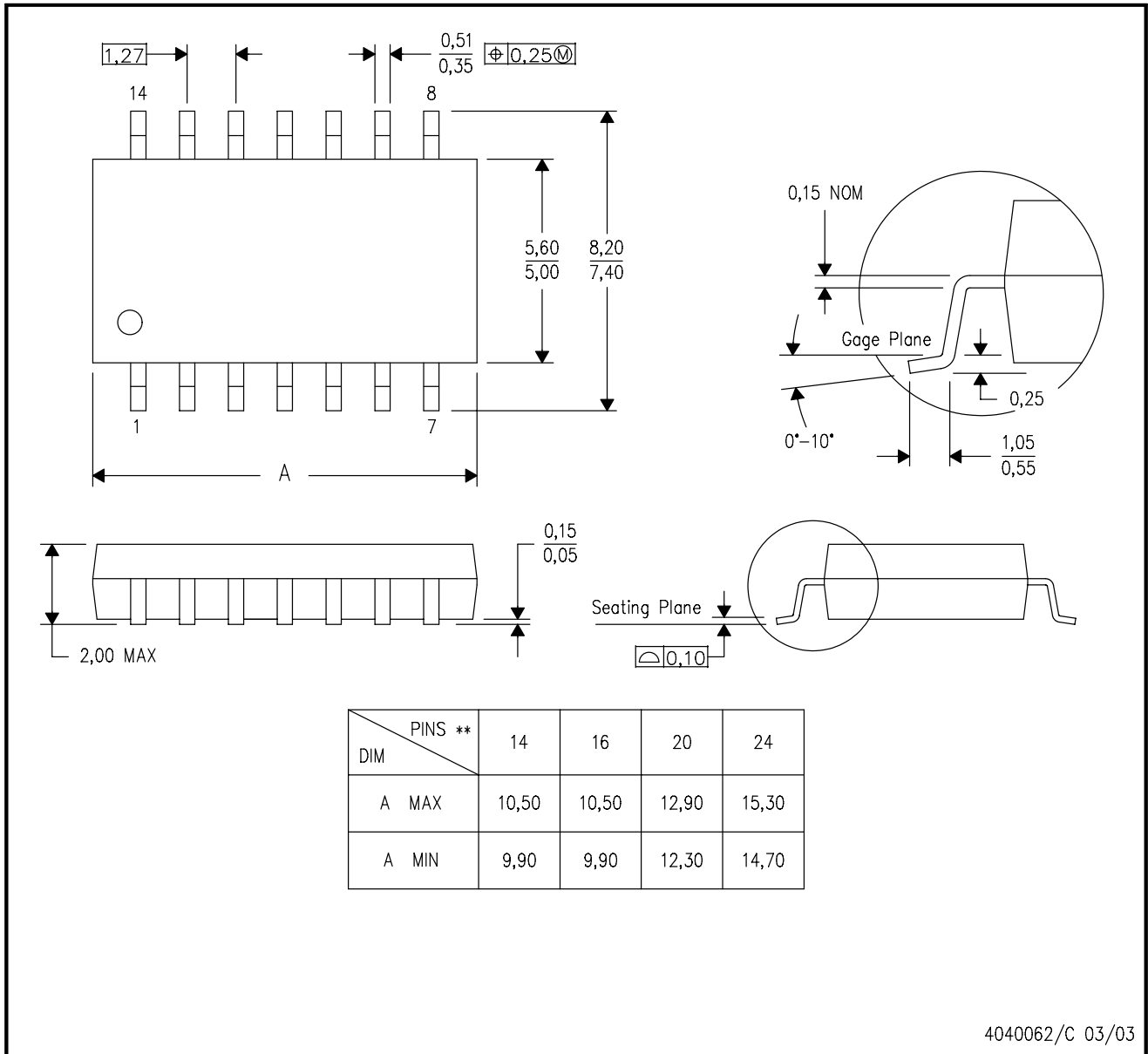
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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