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# **SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A** **OCTAL D-TYPE TRANSPARENT LATCHES** **WITH 3-STATE OUTPUTS**

SDAS048D – DECEMBER 1989 – REVISED JANUARY 1995

- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **True Logic Outputs**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N) and Ceramic (J) 300-mil DIPs, and Ceramic Flat (W) Packages**

## **description**

These octal D-type transparent latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

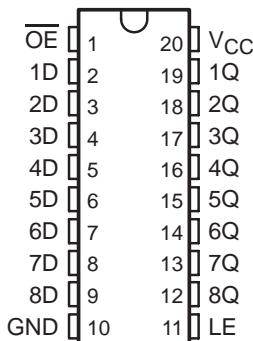
While the latch-enable (LE) input is high, outputs (Q) respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

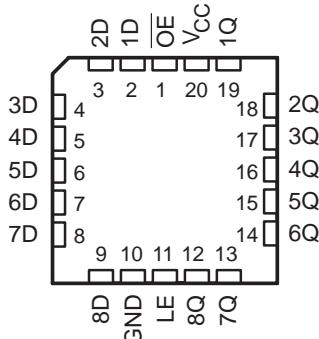
$\overline{OE}$  does not affect internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS573C and SN54AS573A are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS573C and SN74AS573A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**SN54ALS573C, SN54AS573A ... J OR W PACKAGE**  
**SN74ALS573C, SN74AS573A ... DW OR N PACKAGE**  
**(TOP VIEW)**



**SN54ALS573C, SN54AS573A ... FK PACKAGE**  
**(TOP VIEW)**



**FUNCTION TABLE**  
**(each latch)**

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

**PRODUCTION DATA** information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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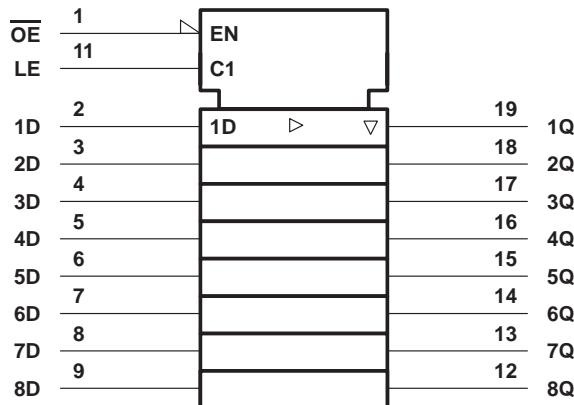
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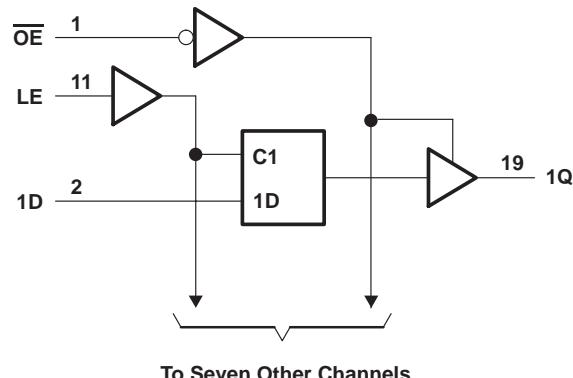
# **SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS**

SDAS048D – DECEMBER 1989 – REVISED JANUARY 1995

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54ALS573C			SN74ALS573C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2			V
V <sub>IL</sub>	Low-level input voltage			0.7			0.8	V
I <sub>OH</sub>	High-level output current			-1			-2.6	mA
I <sub>OL</sub>	Low-level output current			12			24	mA
t <sub>w</sub>	Pulse duration, LE high	25			10			ns
t <sub>su</sub>	Setup time, data before LE↓	10			10			ns
t <sub>h</sub>	Hold time, data after LE↓	7			7			ns
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

**SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A**  
**OCTAL D-TYPE TRANSPARENT LATCHES**  
**WITH 3-STATE OUTPUTS**

SDAS048D – DECEMBER 1989 – REVISED JANUARY 1995

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54ALS573C			SN74ALS573C			UNIT
		MIN	TYPT†	MAX	MIN	TYPT†	MAX	
$V_{IK}$	$V_{CC} = 4.5 \text{ V}$ , $I_I = -18 \text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 \text{ V}$ $I_{OH} = -1 \text{ mA}$	2.4	3.3					
$V_{OL}$	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4	0.25	0.4		V
		$I_{OL} = 24 \text{ mA}$			0.35	0.5		
$I_{OZH}$	$V_{CC} = 5.5 \text{ V}$ , $V_O = 2.7 \text{ V}$		20		20		$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 5.5 \text{ V}$ , $V_O = 0.4 \text{ V}$		-20		-20		$\mu\text{A}$	
$I_I$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 7 \text{ V}$		0.1		0.1		mA	
$I_{IH}$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 2.7 \text{ V}$		20		20		$\mu\text{A}$	
$I_{IL}$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 0.4 \text{ V}$		-0.13		-0.1		mA	
$I_O^{\ddagger}$	$V_{CC} = 5.5 \text{ V}$ , $V_O = 2.25 \text{ V}$	-20	-112	-30	-112		mA	
$I_{CC}$	$V_{CC} = 5.5 \text{ V}$	Outputs high	10	17	10	17		mA
		Outputs low	15	24	15	24		
		Outputs disabled	16	27	16	27		

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $C_L = 50 \text{ pF}$ , $R1 = 500 \Omega$ , $R2 = 500 \Omega$ , $T_A = \text{MIN to MAX}^{\$}$				UNIT	
			SN54ALS573C		SN74ALS573C			
			MIN	MAX	MIN	MAX		
$t_{PLH}$	D	Q	2	20	2	14	ns	
			2	17	2	14		
$t_{PLH}$	LE	Q	8	33	6	20	ns	
			8	24	6	19		
$t_{PZH}$	$\overline{OE}$	Q	4	28	3	18	ns	
			4	21	4	18		
$t_{PHZ}$	$\overline{OE}$	Q	2	20	1	10	ns	
			3	26	1	15		

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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# **SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS**

SDAS048D – DECEMBER 1989 – REVISED JANUARY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## **recommended operating conditions**

		SN54AS573A			SN74AS573A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-12			-15	mA
I <sub>OL</sub>	Low-level output current			32			48	mA
t <sub>w</sub> <sup>*</sup>	Pulse duration, LE high		5.5		4.5			ns
t <sub>su</sub> <sup>*</sup>	Setup time, data before LE↓		2		2			ns
t <sub>h</sub> <sup>*</sup>	Hold time, data after LE↓		3		3			ns
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS573A			SN74AS573A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = 4.5 \text{ V}$ , $I_I = -18 \text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $I_{OH} = -2 \text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -12 \text{ mA}$	2.4	3.2				
		$I_{OH} = -15 \text{ mA}$				2.4	3.3	
$V_{OL}$	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 32 \text{ mA}$	0.28	0.5				V
		$I_{OL} = 48 \text{ mA}$				0.33	0.5	
$I_{OZH}$	$V_{CC} = 5.5 \text{ V}$ , $V_O = 2.7 \text{ V}$			50			50	$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.5 \text{ V}$ , $V_O = 0.4 \text{ V}$			-50			-50	$\mu\text{A}$
$I_I$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 7 \text{ V}$			0.1			0.1	$\text{mA}$
$I_{IH}$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 2.7 \text{ V}$			20			20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 0.4 \text{ V}$			-0.1			-0.5	$\text{mA}$
$I_O^S$	$V_{CC} = 5.5 \text{ V}$ , $V_O = 2.25 \text{ V}$	-30	-112	-30	-112			$\text{mA}$
$I_{CC}$	$V_{CC} = 5.5 \text{ V}$	Outputs high		56	93		56	93
		Outputs low		55	90		55	90
		Outputs disabled		65	106		65	106

<sup>‡</sup>All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

**SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A**  
**OCTAL D-TYPE TRANSPARENT LATCHES**  
**WITH 3-STATE OUTPUTS**

SDAS048D – DECEMBER 1989 – REVISED JANUARY 1995

**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT	
			SN54AS573A		SN74AS573A			
			MIN	MAX	MIN	MAX		
t <sub>PLH</sub>	D	Q	3	11	3	8	ns	
t <sub>PHL</sub>			3	8	3	7		
t <sub>PLH</sub>	LE	Q	6	16.5	6	13	ns	
t <sub>PHL</sub>			4	9	4	7.5		
t <sub>PZH</sub>	OE	Q	2	8	2	6.5	ns	
t <sub>PZL</sub>			4	11	4	9.5		
t <sub>PHZ</sub>	OE	Q	2	8	2	6.5	ns	
t <sub>PLZ</sub>			2	8	2	7		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

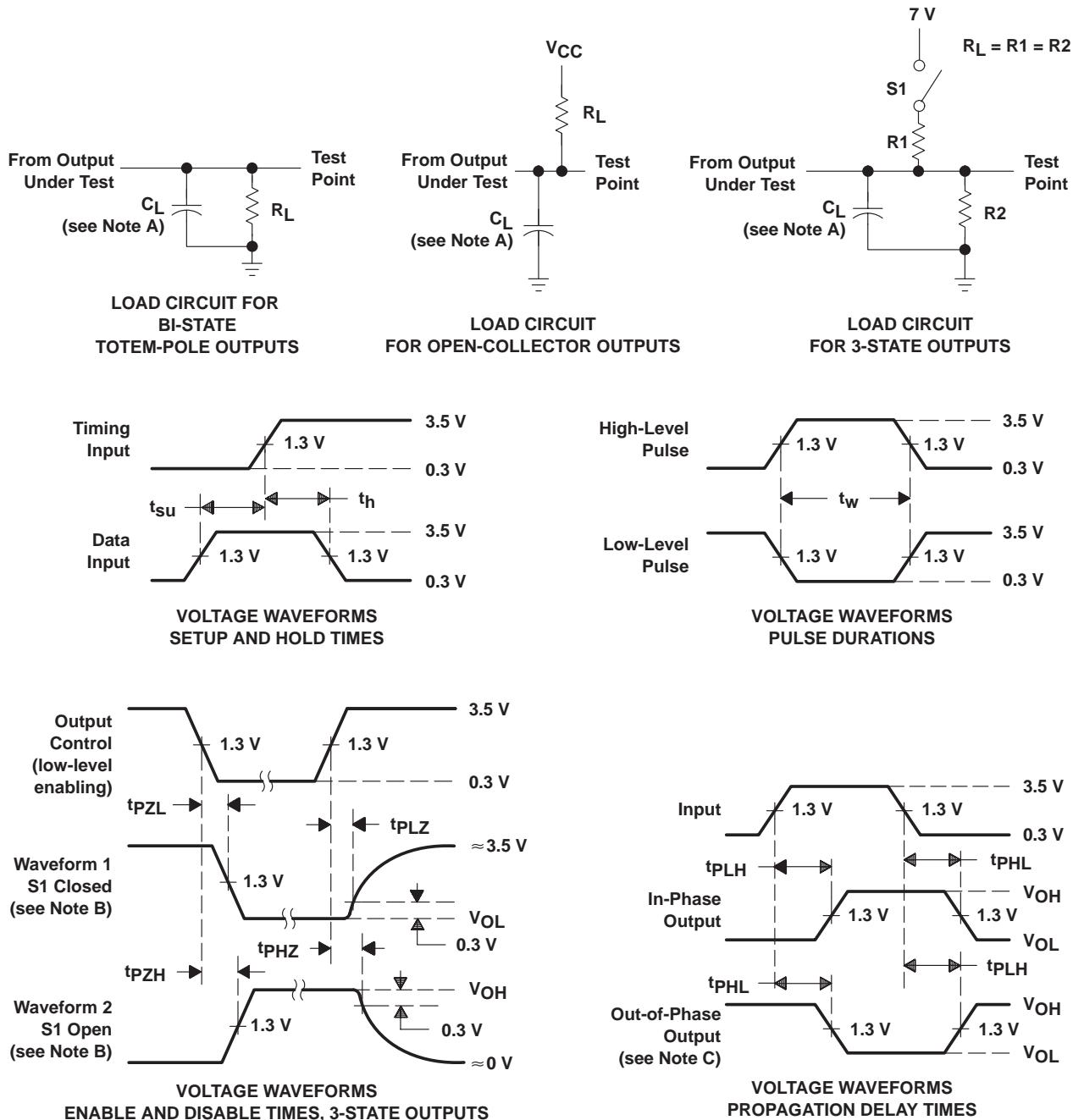


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**SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A**  
**OCTAL D-TYPE TRANSPARENT LATCHES**  
**WITH 3-STATE OUTPUTS**

SDAS048D - DECEMBER 1989 - REVISED JANUARY 1995

**PARAMETER MEASUREMENT INFORMATION**  
**SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics: PRR  $\leq$  1 MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84012012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84012012A SNJ54ALS 573CFK	<b>Samples</b>
8401201RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8401201RA SNJ54ALS573CJ	<b>Samples</b>
8401201SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8401201SA SNJ54ALS573CW	<b>Samples</b>
JM38510/38201B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 38201B2A	<b>Samples</b>
JM38510/38201BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 38201BRA	<b>Samples</b>
M38510/38201B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 38201B2A	<b>Samples</b>
M38510/38201BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 38201BRA	<b>Samples</b>
SN54ALS573CJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54ALS573CJ	<b>Samples</b>
SN54AS573AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54AS573AJ	<b>Samples</b>
SN74ALS573CDBLE	OBsolete	SSOP	DB	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS573CDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	G573C	<b>Samples</b>
SN74ALS573CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS573C	<b>Samples</b>
SN74ALS573CDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS573C	<b>Samples</b>
SN74ALS573CDWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS573C	<b>Samples</b>
SN74ALS573CDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS573C	<b>Samples</b>
SN74ALS573CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS573CN	<b>Samples</b>
SN74ALS573CN3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS573CNE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS573CN	<b>Samples</b>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS573CNSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS573C	<a href="#">Samples</a>
SN74ALS573CNSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS573C	<a href="#">Samples</a>
SN74AS573ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS573A	<a href="#">Samples</a>
SN74AS573ADWR	OBsolete	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74AS573ADWRE4	OBsolete	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74AS573ADWRG4	OBsolete	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74AS573AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS573AN	<a href="#">Samples</a>
SN74AS573AN3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74AS573ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS573AN	<a href="#">Samples</a>
SNJ54ALS573CFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84012012A SNJ54ALS573CFK	<a href="#">Samples</a>
SNJ54ALS573CJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8401201RA SNJ54ALS573CJ	<a href="#">Samples</a>
SNJ54ALS573CW	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8401201SA SNJ54ALS573CW	<a href="#">Samples</a>
SNJ54AS573AFK	OBsolete	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
SNJ54AS573AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54AS573AJ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "—" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A :**

• Catalog: [SN74ALS573C](#), [SN74AS573A](#)

• Military: [SN54ALS573C](#), [SN54AS573A](#)

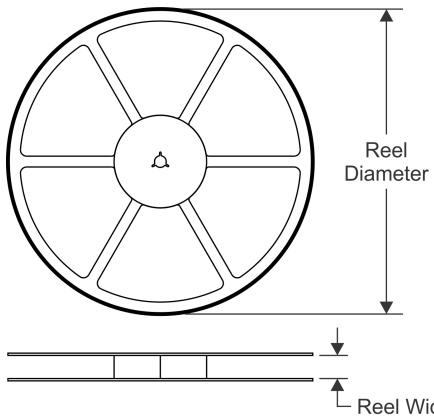
## NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

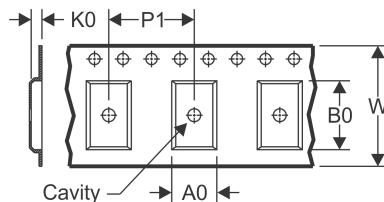
• Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**

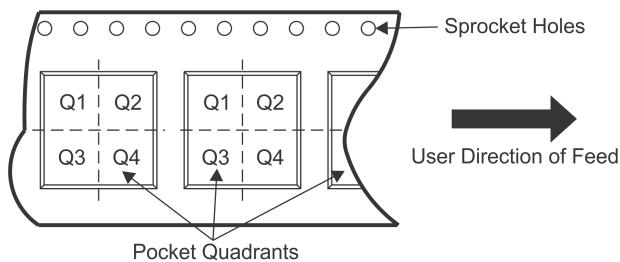


**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

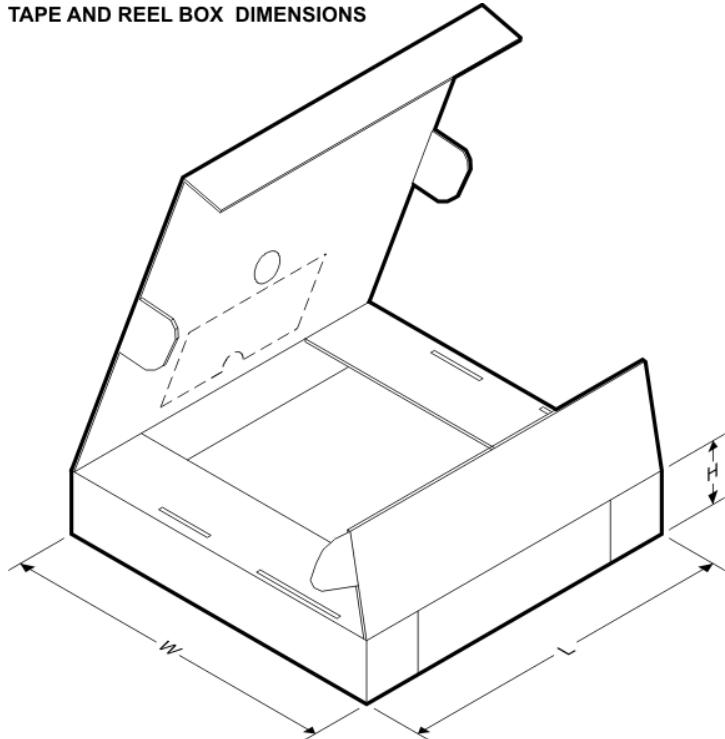
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS573CDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ALS573CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ALS573CNSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



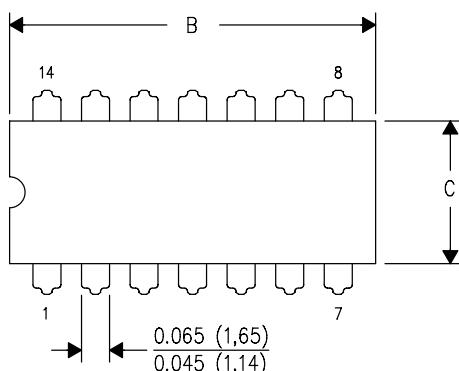
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS573CDBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74ALS573CDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS573CNSR	SO	NS	20	2000	367.0	367.0	45.0

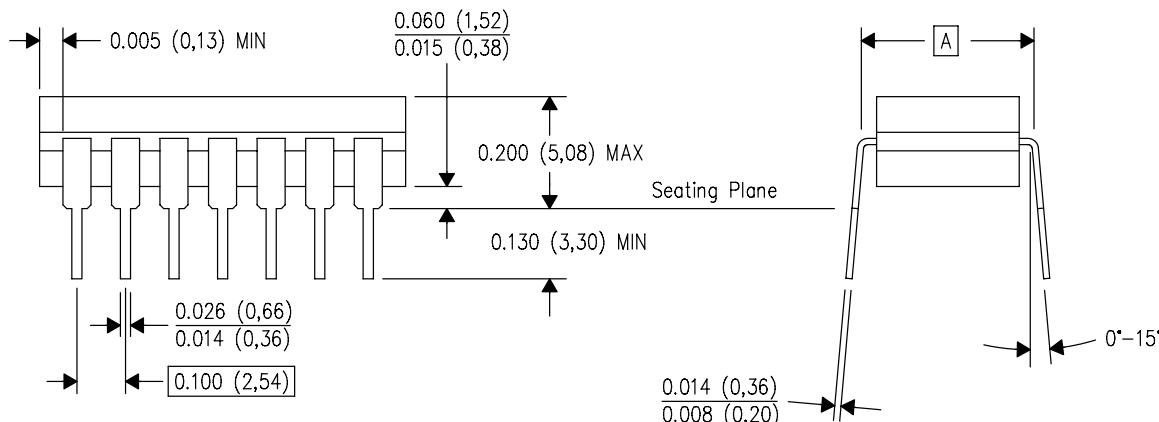
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM	PINS **	14	16	18	20
		A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX		0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN		—	—	—	—
C MAX		0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN		0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

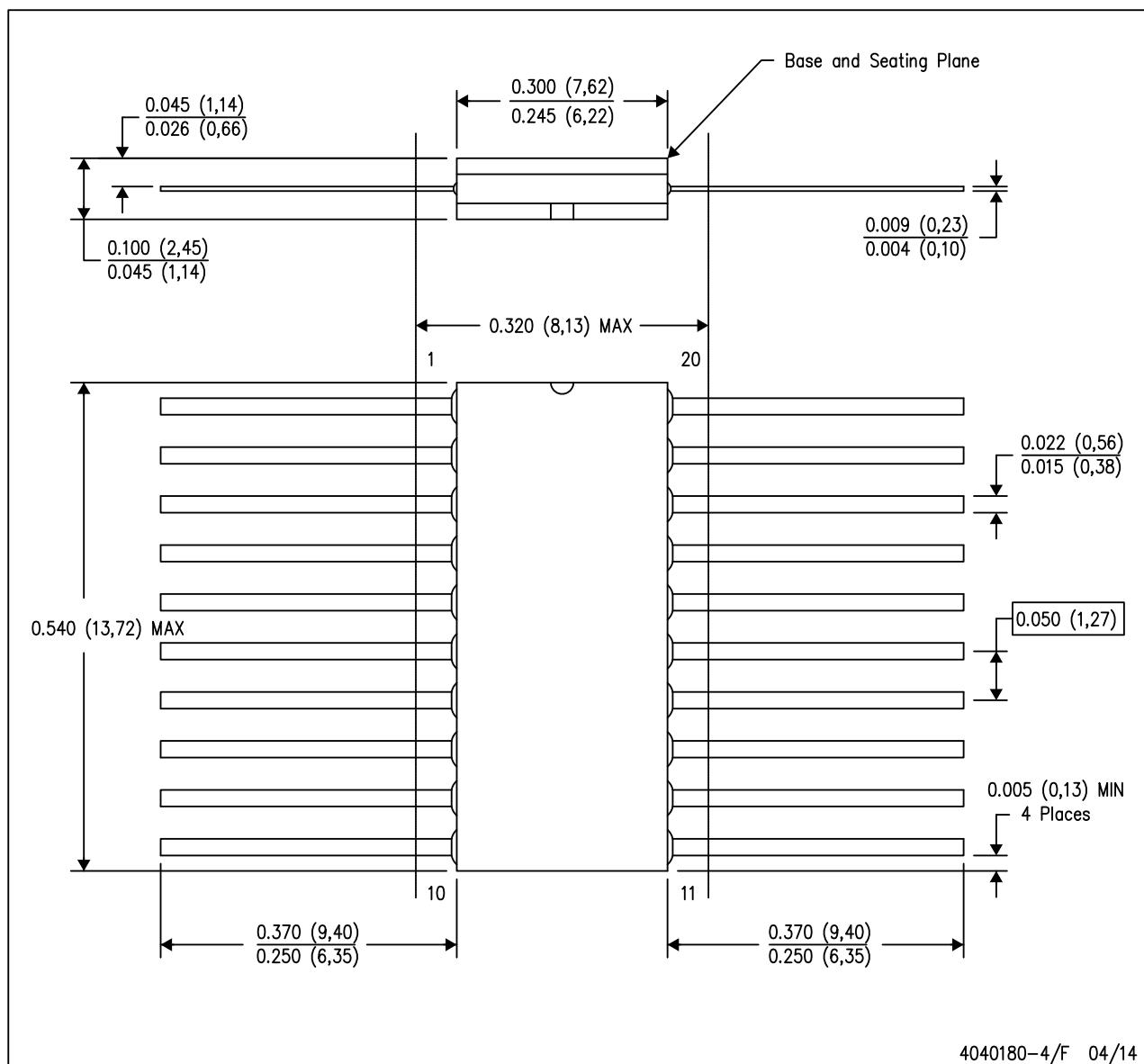
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## MECHANICAL DATA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



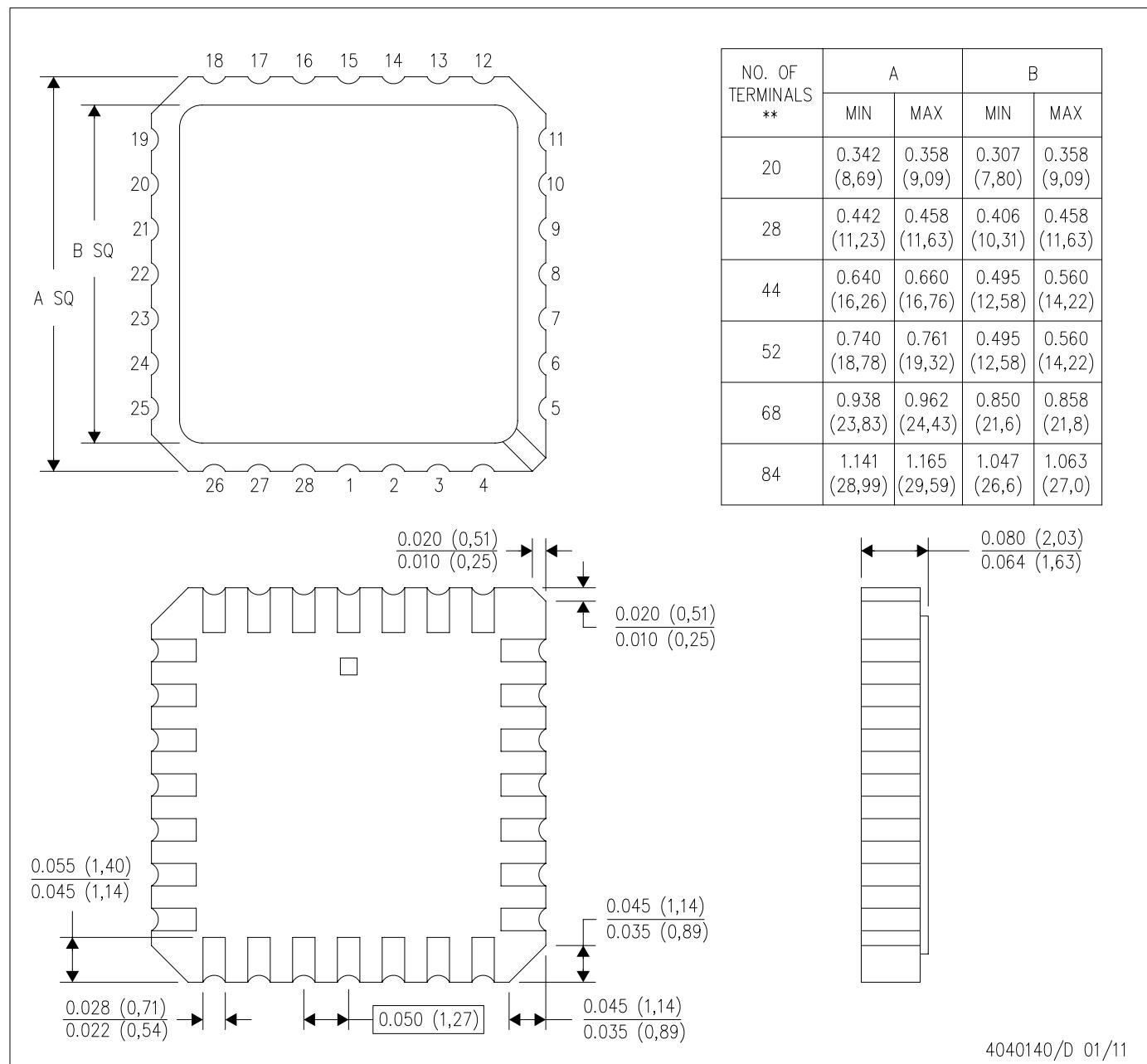
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within Mil-Std 1835 GDFP2-F20

**FK (S-CQCC-N\*\*)**

28 TERMINAL SHOWN

**LEADLESS CERAMIC CHIP CARRIER**



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a metal lid.  
 D. Falls within JEDEC MS-004

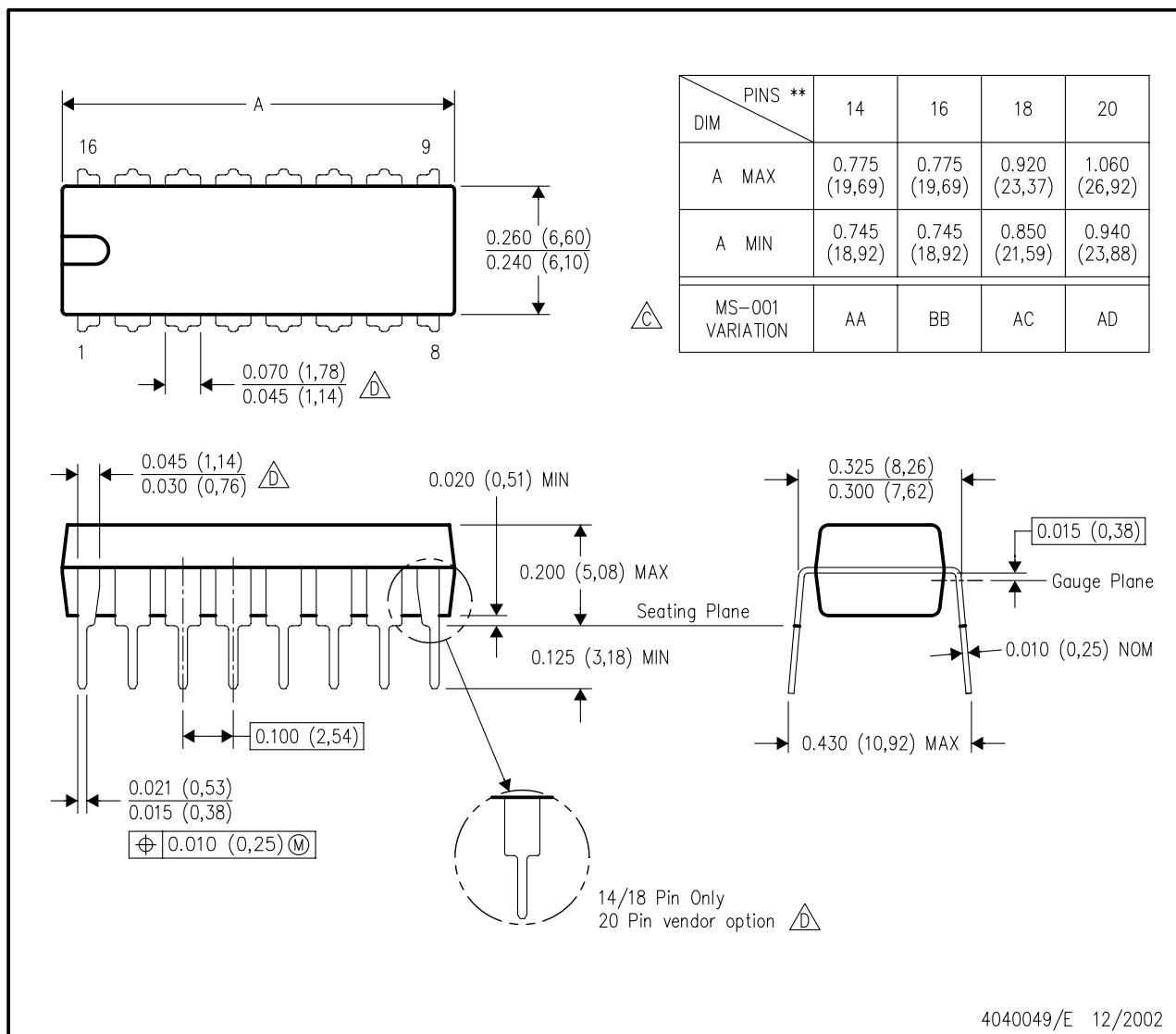
4040140/D 01/11

## MECHANICAL DATA

### N (R-PDIP-T\*\*)

16 PINS SHOWN

### PLASTIC DUAL-IN-LINE PACKAGE



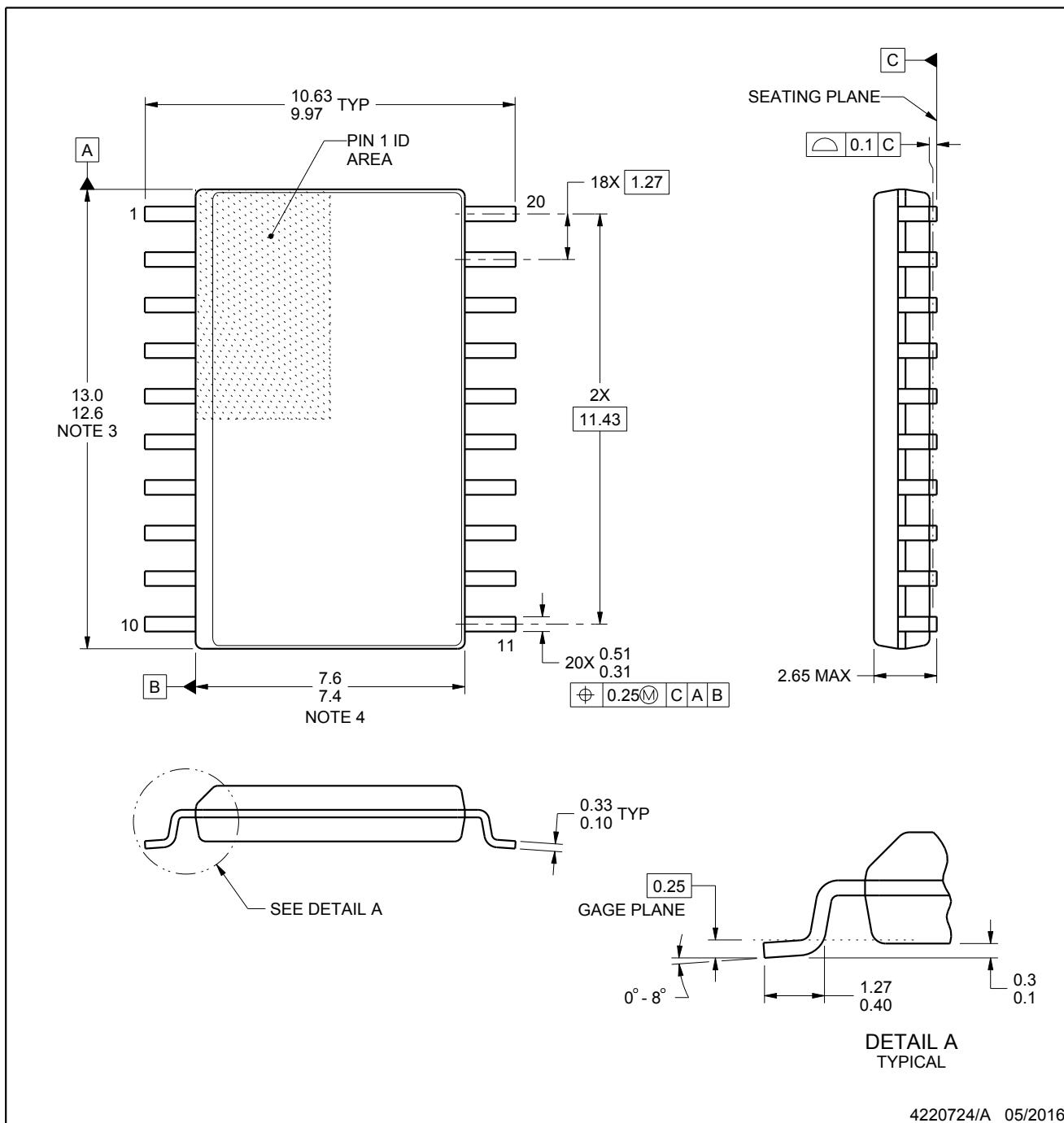


## PACKAGE OUTLINE

**DW0020A**

**SOIC - 2.65 mm max height**

SOIC



4220724/A 05/2016

**NOTES:**

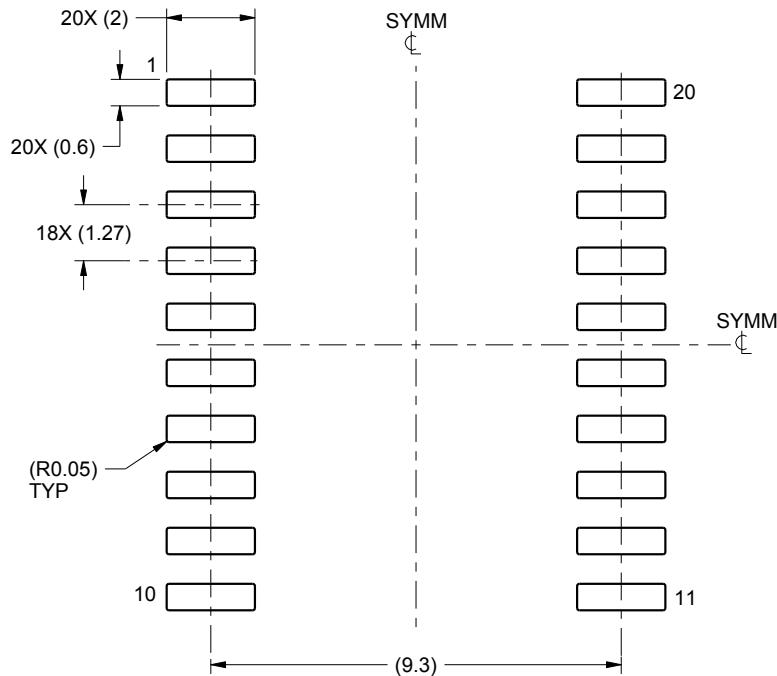
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

## EXAMPLE BOARD LAYOUT

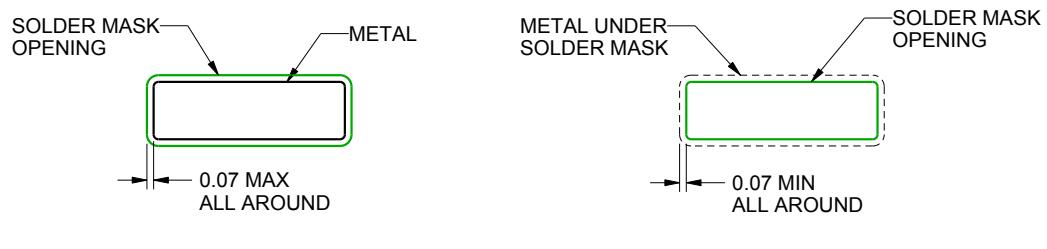
**DW0020A**

**SOIC - 2.65 mm max height**

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

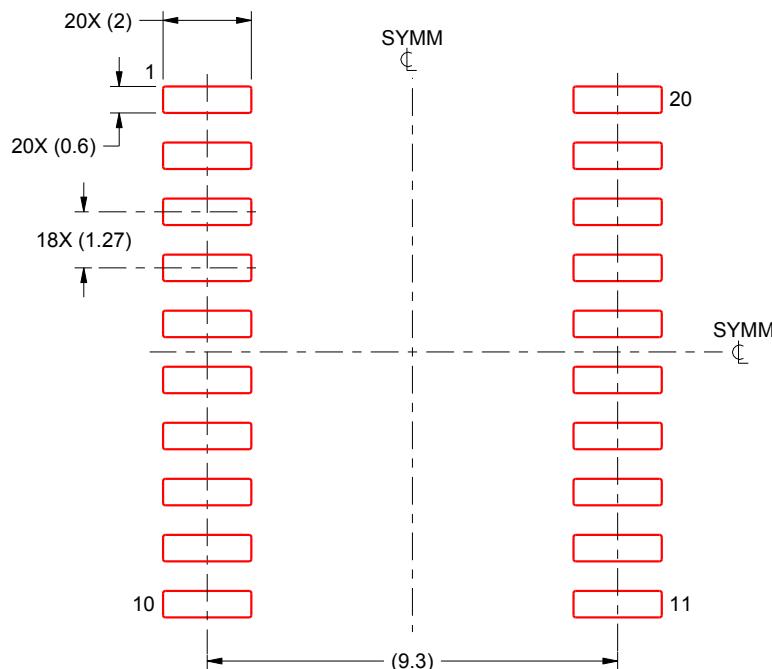
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**DW0020A**

**SOIC - 2.65 mm max height**

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

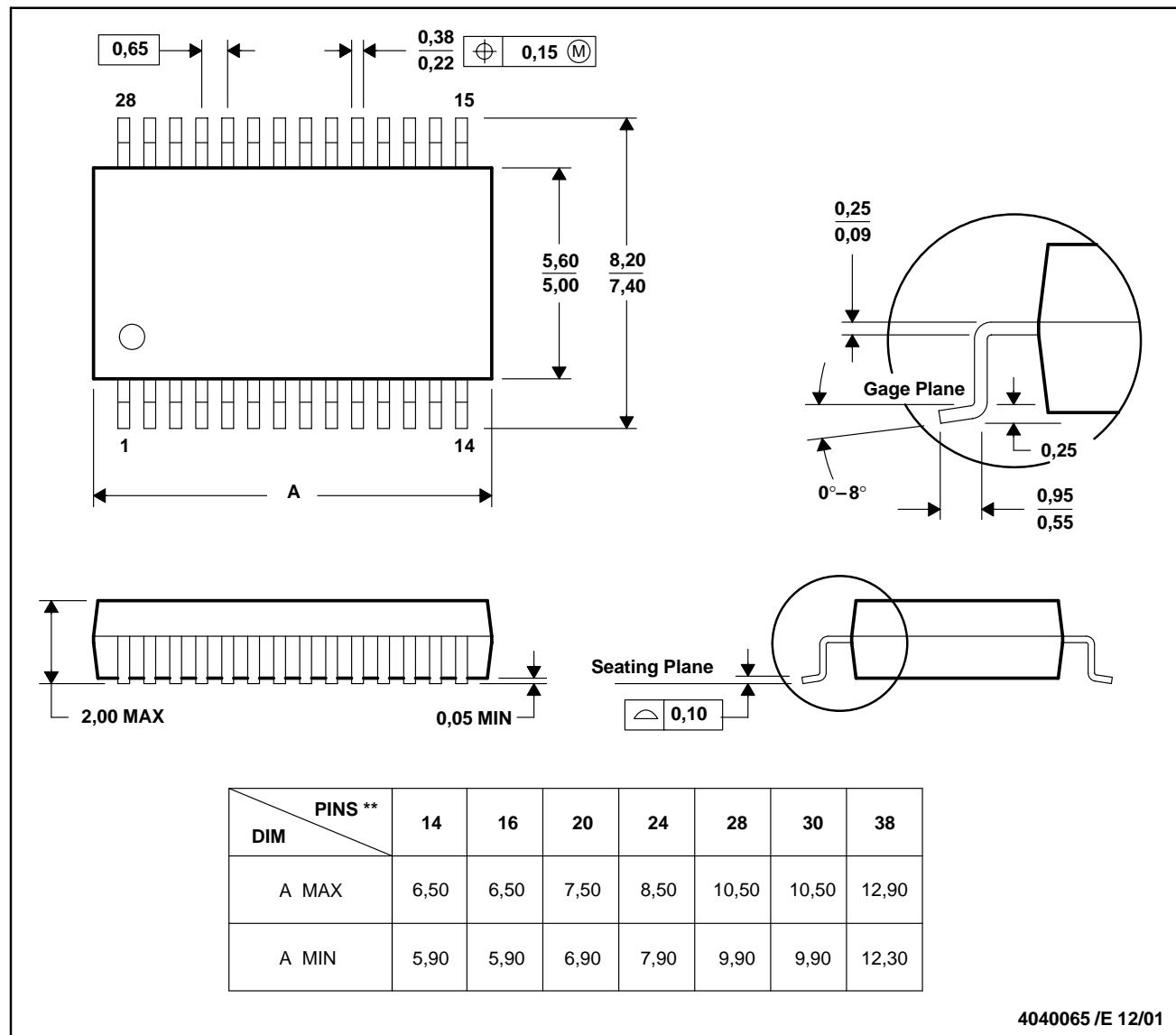
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MSS002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G\*\*)**

28 PINS SHOWN

**PLASTIC SMALL-OUTLINE**



4040065 /E 12/01

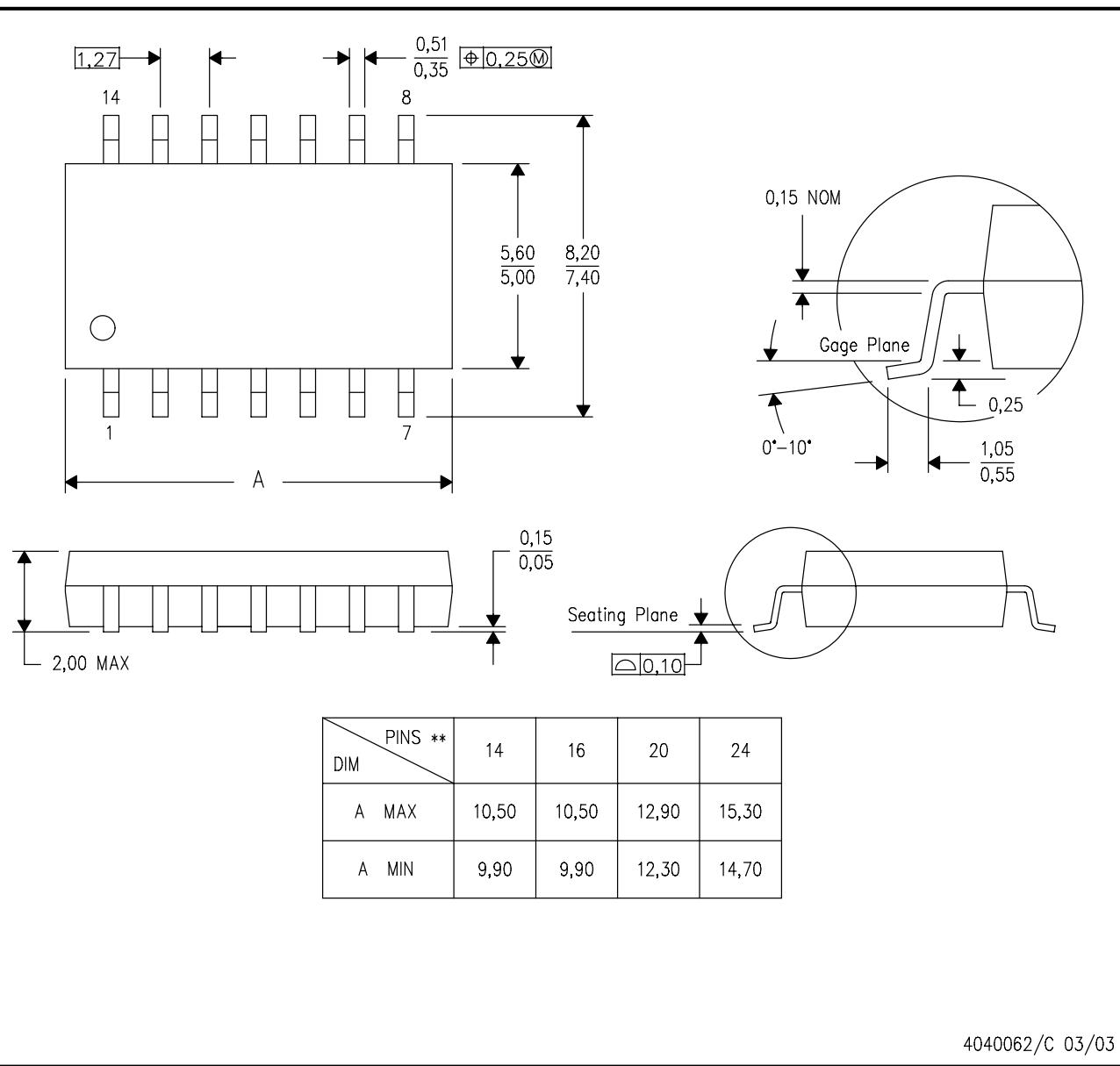
NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
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