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SN54132, SN54LS132, SN54S132, SN74132, SN74LS132, SN74S132 QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

SDLS047 - DECEMBER 1983 - REVISED MARCH 1988

- Operation from Very Slow Edges
- Improved Line-Receiving Characteristics
- High Noise Immunity

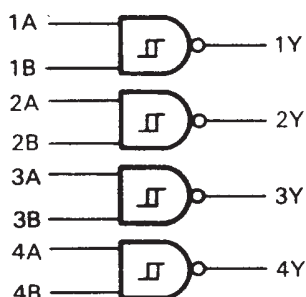
description

Each circuit functions as a 2-input NAND gate, but because of the Schmitt action, it has different input threshold levels for positive (V_{T+}) and for negative going (V_{T-}) signals.

These circuits are temperature-compensated and can be triggered from the slowest of input ramps and still give clear, jitter-free output signals.

The SN54132, SN54LS132, and SN54S132 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74132, SN74LS132, and SN74S132 are characterized for operation from 0°C to 70°C .

logic diagram (positive logic)

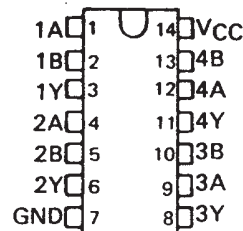


SN54132, SN54LS132, SN54S132 . . . J OR W PACKAGE

SN74132 . . . N PACKAGE

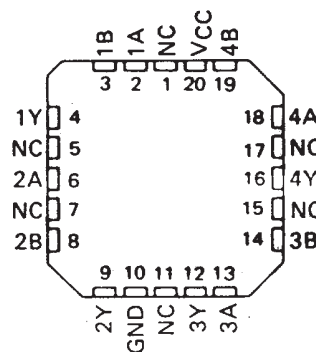
SN74LS132, SN74S132 . . . D OR N PACKAGE

(TOP VIEW)



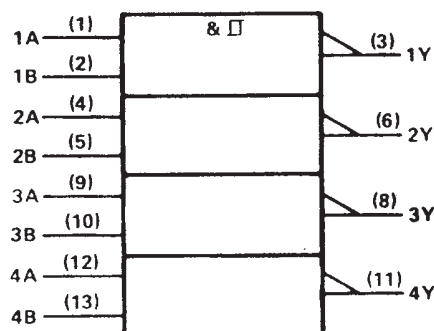
SN54LS132, SN54S132 . . . FK PACKAGE

(TOP VIEW)



NC-No internal connection

logic symbol†



positive logic: $Y = \overline{AB}$ or $Y = \overline{A} + \overline{B}$

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

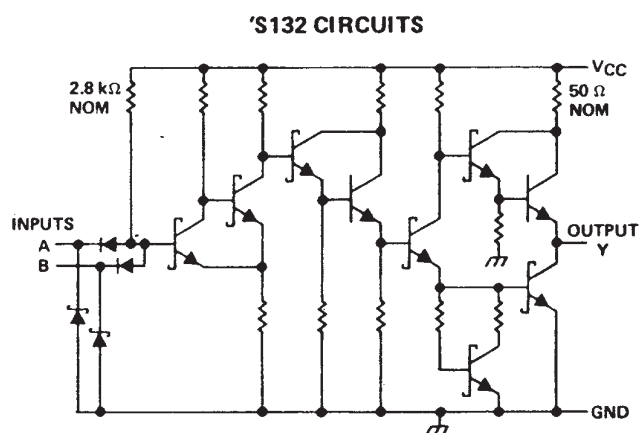
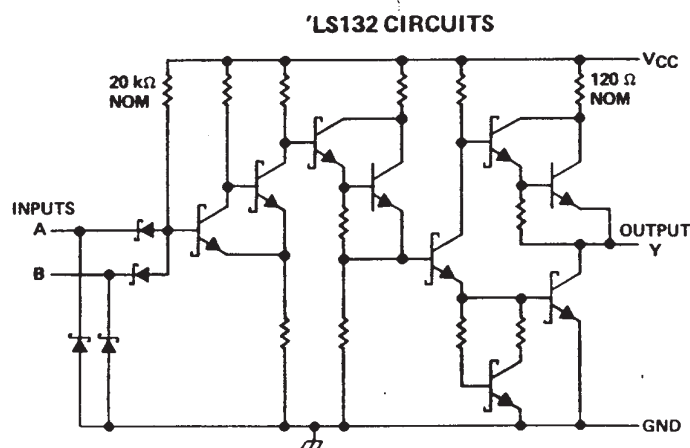
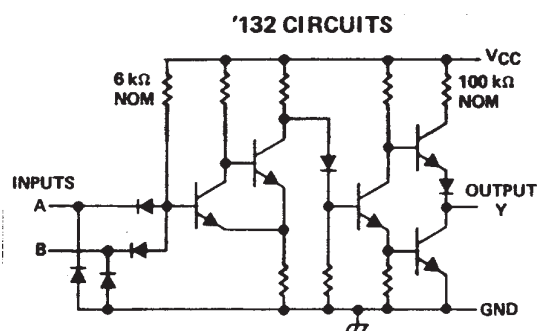
SN54132, SN54LS132, SN54S132,

SN74132, SN74LS132, SN74S132

QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

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schematics



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1).	7 V
Input voltage: '132, 'S132.	5.5 V
'LS132.	7 V
Operating free-air temperature: SN54'.	-55°C to 125°C
SN74'.	0°C to 70°C
Storage temperature range.	-65°C to 150°C

NOTE 1: Voltages values are with respect to network ground terminal.

SN54132, SN74132 QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

SDLS047 - DECEMBER 1983 - REVISED MARCH 1988

recommended operating conditions

	SN54132			SN74132			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH} High-level output current			-0.8			-0.8	mA
I _{OL} Low-level output current			16			16	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{T+}	V _{CC} = 5 V	1.5	1.7	2	V
V _{T-}	V _{CC} = 5 V	0.6	0.9	1.1	V
V _{hys} (V _{T+} - V _{T-})	V _{CC} = 5 V	0.4	0.8		V
V _{IK}	V _{CC} = MIN, I _I = -12 mA			-1.5	V
V _{OH}	V _{CC} = MIN, V _I = 0.6 V, I _{OH} = -0.8 mA	2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _I = 2 V, I _{OL} = 16 mA		0.2	0.4	V
I _{T+}	V _{CC} = 5 V, V _I = V _{T+}	-0.43			mA
I _{T-}	V _{CC} = 5 V, V _I = V _{T-}	-0.56			mA
I _I	V _{CC} = MAX, V _I = 5.5 V			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V			40	μA
I _{IL}	V _{CC} = MAX, V _{IL} = 0.4 V	-0.8		-1.2	mA
I _{OS} §	V _{CC} = MAX	-18		-55	mA
I _{CCH}	V _{CC} = MAX		15	24	mA
I _{CCL}	V _{CC} = MAX		26	40	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Y	R _L = 400 Ω, C _L = 15 pF		15	22	ns
t _{PHL}					15	22	ns



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SN54LS132, SN74LS132 QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

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recommended operating conditions

	SN54LS132			SN74LS132			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH} High-level output current			– 0.4			– 0.4	mA
I _{OL} Low-level output current			4			8	mA
T _A Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS132			SN74LS132			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	$V_{CC} = 5\text{ V}$		1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	$V_{CC} = 5\text{ V}$		0.5	0.8	1	0.5	0.8	1	V
V_{hys} ($V_{T+} - V_{T-}$)	$V_{CC} = 5\text{ V}$		0.4	0.8		0.4	0.8		V
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18\text{ mA}$		-1.5			-1.5			V
V_{OH}	$V_{CC} = \text{MIN}, V_I = 0.5\text{ V}, I_{OH} = -0.4\text{ mA}$		2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_I = 1.9\text{ V}$	$I_{OL} = 4\text{ mA}$	0.25 0.4			0.25 0.4			V
		$I_{OL} = 8\text{ mA}$				0.35 0.5			
I_{T+}	$V_{CC} = 5\text{ V}, V_I = V_{T+}$		-0.14			-0.14			mA
I_{T-}	$V_{CC} = 5\text{ V}, V_I = V_{T-}$		-0.18			-0.18			mA
I_I	$V_{CC} = \text{MAX}, V_I = 7\text{ V}$		0.1			0.1			mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7\text{ V}$		20			20			μA
I_{IL}	$V_{CC} = \text{MAX}, V_{IL} = 0.4\text{ V}$		-0.4			-0.4			mA
$I_{OS} §$	$V_{CC} = \text{MAX}$		-20		-100	-20		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}$		5.9 11			5.9 11			mA
I_{CCL}	$V_{CC} = \text{MAX}$		8.2 14			8.2 14			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25° C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second

switching characteristics, V_{CC} = 5 V, T_A = 25° C (see figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Y	R _L = 2 kΩ, C _L = 15 pF		15	22	ns
t _{PHL}					15	22	ns

SN54S132, SN74S132 QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

SDLS047 - DECEMBER 1983 - REVISED MARCH 1988

recommended operating conditions

	SN54S132			SN74S132			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH} High-level output current			-1			-1	mA
I _{OL} Low-level output current			20			20	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S132			SN74S132			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{T+}	V _{CC} = 5 V	1.6	1.77	1.9	1.6	1.77	1.9	V
V _{T-}	V _{CC} = 5 V	1.1	1.22	1.4	1.1	1.22	1.4	V
V _{hys} (V _{T+} - V _{T-})	V _{CC} = 5 V	0.2	0.55		0.2	0.55		V
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = MIN, V _I = 1.1 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _I = 1.9 V, I _{OL} = 20 mA			0.5			0.5	V
I _{T+}	V _{CC} = 5 V, V _I = V _{T+}		-0.9			-0.9		mA
I _{T-}	V _{CC} = 5 V, V _I = V _{T-}		-1.1			-1.1		mA
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			50			50	μA
I _{IL}	V _{CC} = MAX, V _{IL} = 0.5 V			-2			-2	mA
I _{OS} §	V _{CC} = MAX	-40		-100	-40		-100	mA
I _{CCH}	V _{CC} = MAX		28	44		28	44	mA
I _{CCL}	V _{CC} = MAX		44	68		44	68	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 280 Ω, C _L = 15 pF		7	10.5	ns
t _{PHL}					8.5	13	ns



**TEXAS
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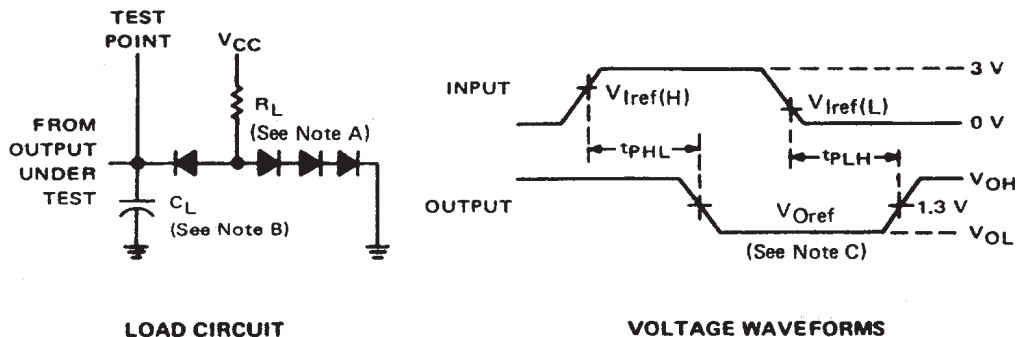
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**SN54132, SN54LS132, SN54S132,
SN74132, SN74LS132, SN74S132**

QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. All diodes are 1N3064 or equivalent.
B. C_L includes probe and jig capacitance.
C. Generator characteristics and reference voltages are:

	Generator Characteristics				Reference Voltages		
	Z_{out}	PRR	t_r	t_f	$V_{I\ ref(H)}$	$V_{I\ ref(L)}$	$V_{O\ ref}$
SN54'/SN74'	50	1 MHz	10 ns	10 ns	1.7 V	0.9 V	1.5 V
SN54LS'/SN74LS'	50	1 MHz	15 ns	6 ns	1.6 V	0.8 V	1.3 V
'S132	50	1 MHz	2.5 ns	2.5 ns	1.8 V	1.2 V	1.5 V

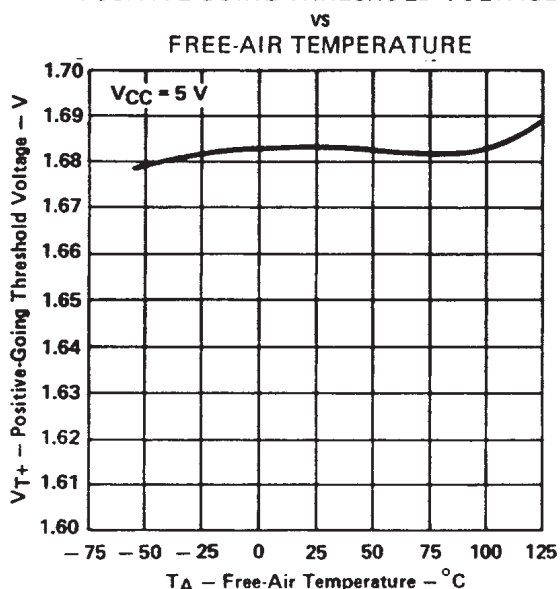
FIGURE 1

SN54132, SN74132
QUADRUPL 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

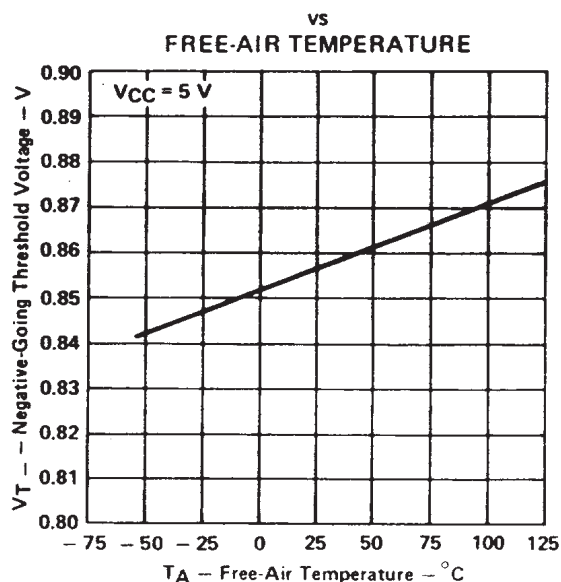
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TYPICAL CHARACTERISTICS OF '132 CIRCUITS

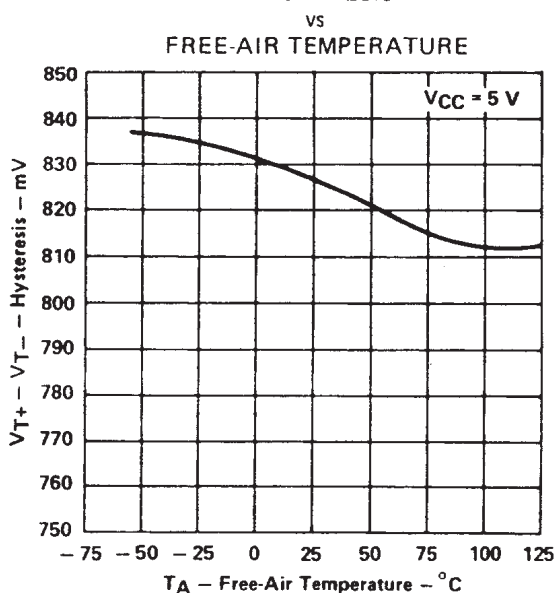
POSITIVE-GOING THRESHOLD VOLTAGE



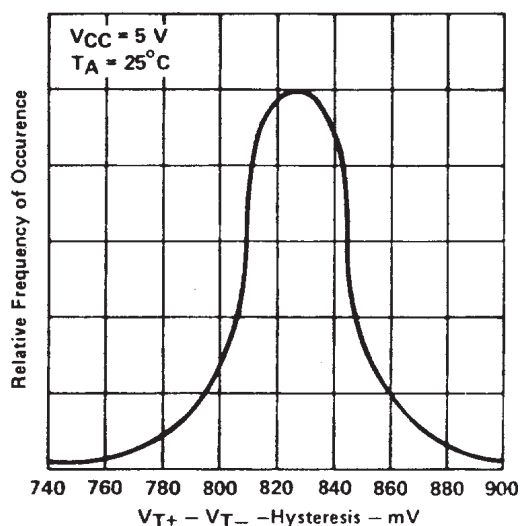
NEGATIVE-GOING THRESHOLD VOLTAGE



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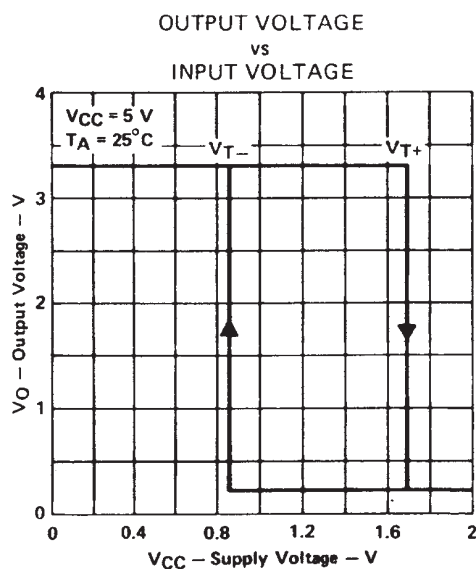
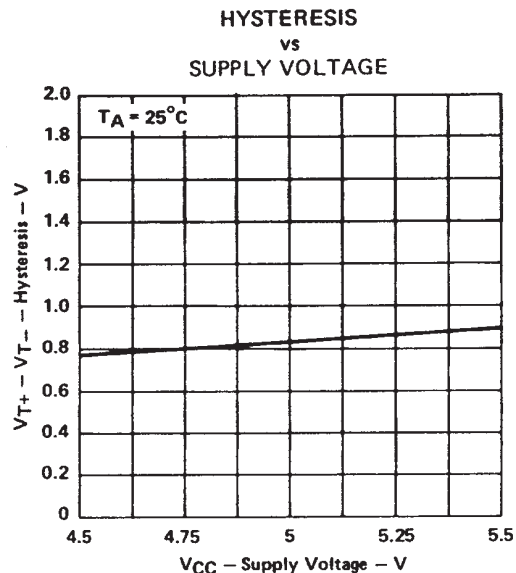
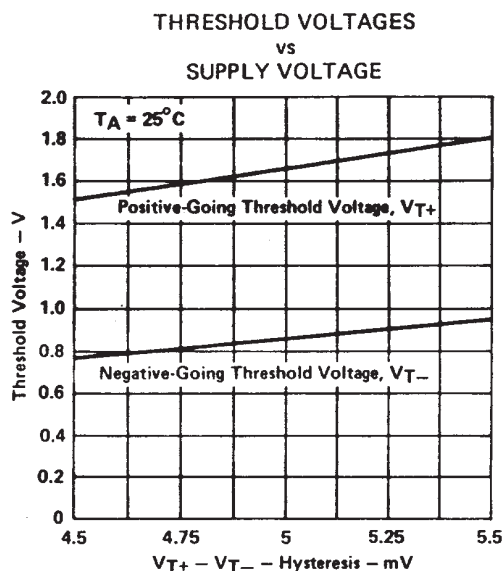
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SN54132, SN74132 QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

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TYPICAL CHARACTERISTICS OF '132 CIRCUITS

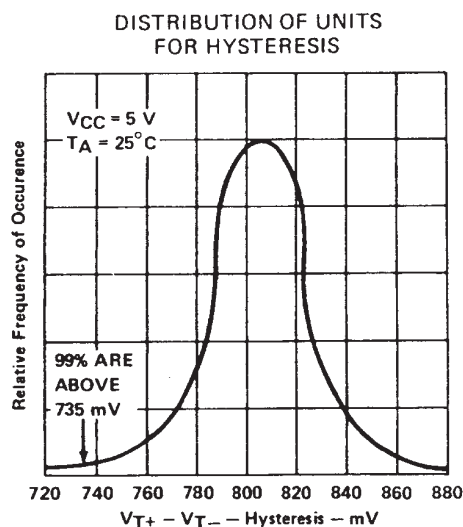
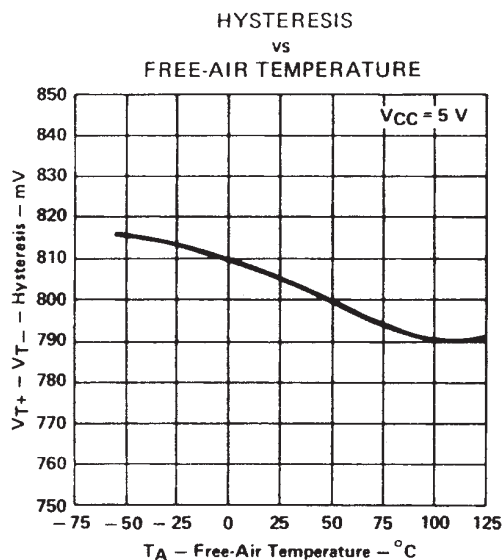
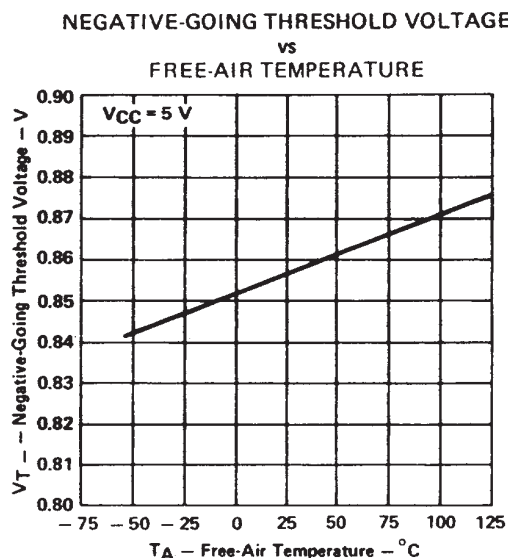
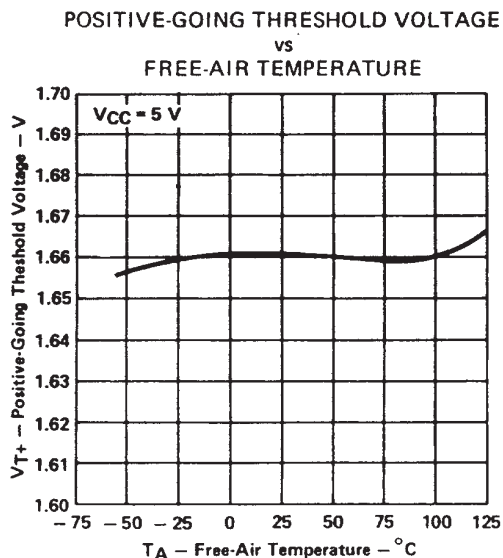


† Data for temperatures below 0°C and 70°C and supply below 4.75 V and above 5.25 V are applicable for SN54132 only.

SN54LS132, SN74LS132 QUADRUPL 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

SDLS047 - DECEMBER 1983 - REVISED MARCH 1988

TYPICAL CHARACTERISTICS OF 'LS132 CIRCUITS



Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS132 only.



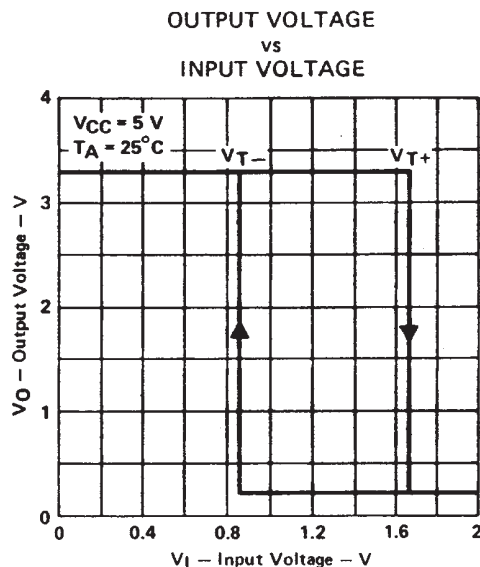
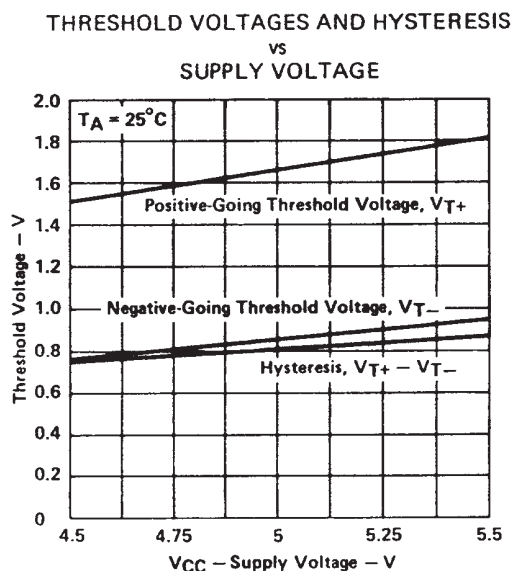
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SDLS047 - DECEMBER 1983 - REVISED MARCH 1988

TYPICAL CHARACTERISTICS OF 'LS132 CIRCUITS



† Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS132 only.

SDLS047 – DECEMBER 1983 – REVISED MARCH 1988

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
7600401CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7600401CA SNJ54LS132J	Samples
7600401DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7600401DA SNJ54LS132W	Samples
7600401DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7600401DA SNJ54LS132W	Samples
JM38510/31303BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31303BCA	Samples
JM38510/31303BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31303BCA	Samples
M38510/31303BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31303BCA	Samples
M38510/31303BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31303BCA	Samples
SN54132J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SN54132J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SN54LS132J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS132J	Samples
SN54LS132J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS132J	Samples
SN54S132J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S132J	Samples
SN54S132J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S132J	Samples
SN74132N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74132N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74132N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74132N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS132D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS132	Samples
SN74LS132D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS132	Samples
SN74LS132DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS132	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS132DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS132	Samples
SN74LS132DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS132	Samples
SN74LS132DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS132	Samples
SN74LS132DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS132	Samples
SN74LS132DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS132	Samples
SN74LS132J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	0 to 70		
SN74LS132J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	0 to 70		
SN74LS132N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS132N	Samples
SN74LS132N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS132N	Samples
SN74LS132N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS132N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS132NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS132N	Samples
SN74LS132NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS132N	Samples
SN74LS132NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS132	Samples
SN74LS132NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS132	Samples
SN74S132N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70	SN74S132N	
SN74S132N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70	SN74S132N	
SN74S132N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74S132N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SNJ54132J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SNJ54132J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SNJ54LS132FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 132FK	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS132FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 132FK	Samples
SNJ54LS132J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7600401CA SNJ54LS132J	Samples
SNJ54LS132J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7600401CA SNJ54LS132J	Samples
SNJ54LS132W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7600401DA SNJ54LS132W	Samples
SNJ54LS132W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7600401DA SNJ54LS132W	Samples
SNJ54S132FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 132FK	Samples
SNJ54S132FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 132FK	Samples
SNJ54S132J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S132J	Samples
SNJ54S132J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S132J	Samples
SNJ54S132W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S132W	Samples
SNJ54S132W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S132W	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)



⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54132, SN54LS132, SN54S132, SN74132, SN74LS132, SN74S132 :

• Catalog: [SN74132](#), [SN74LS132](#), [SN74S132](#)

• Military: [SN54132](#), [SN54LS132](#), [SN54S132](#)

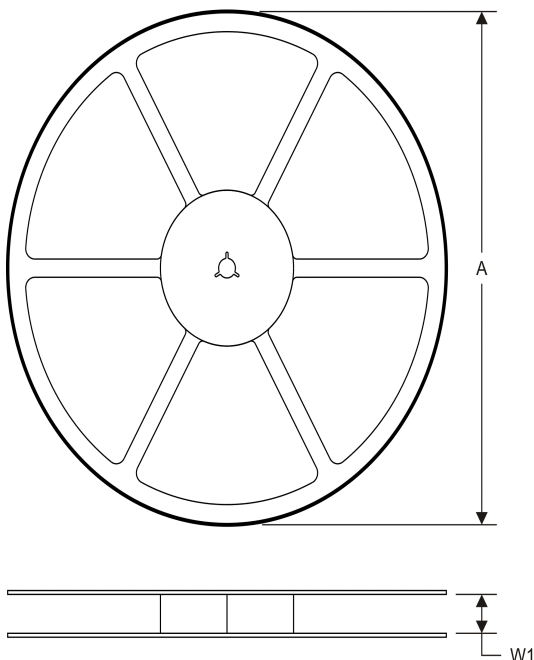
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

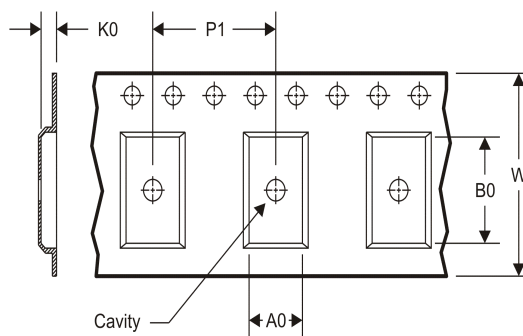
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



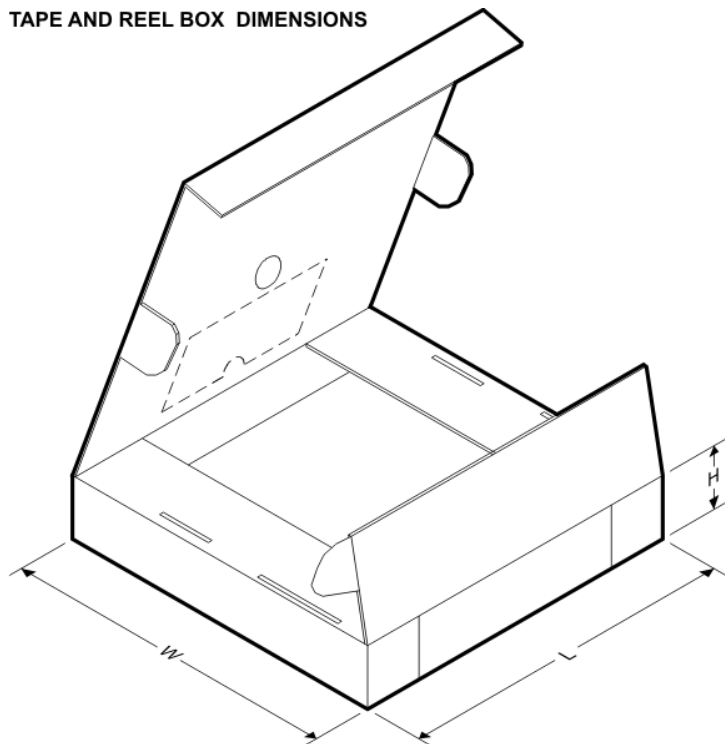
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS132DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS132NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



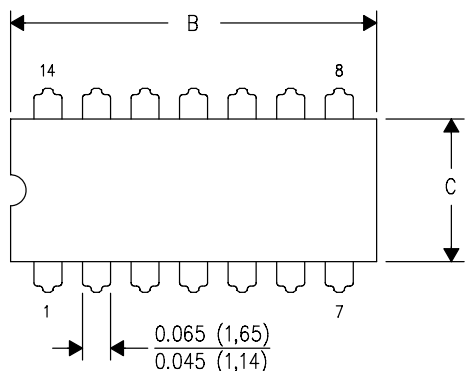
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS132DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LS132NSR	SO	NS	14	2000	367.0	367.0	38.0

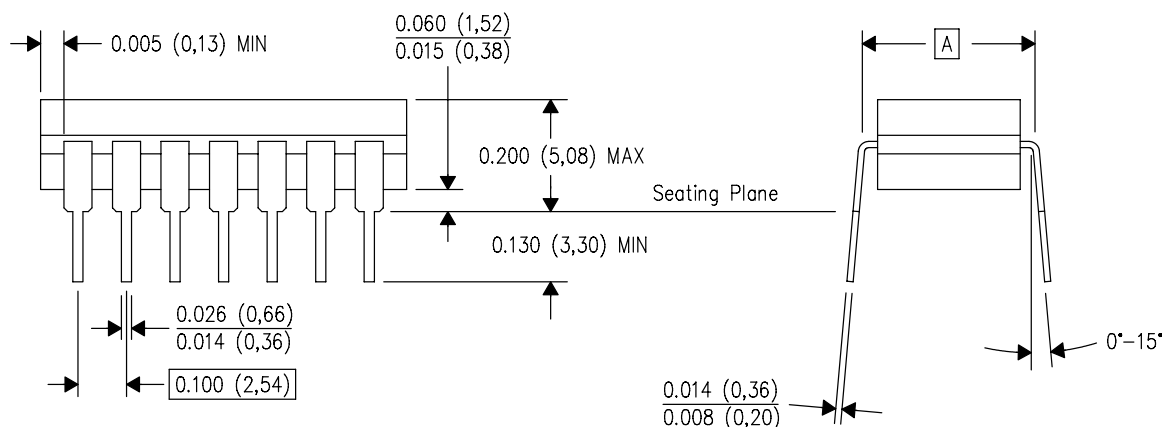
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



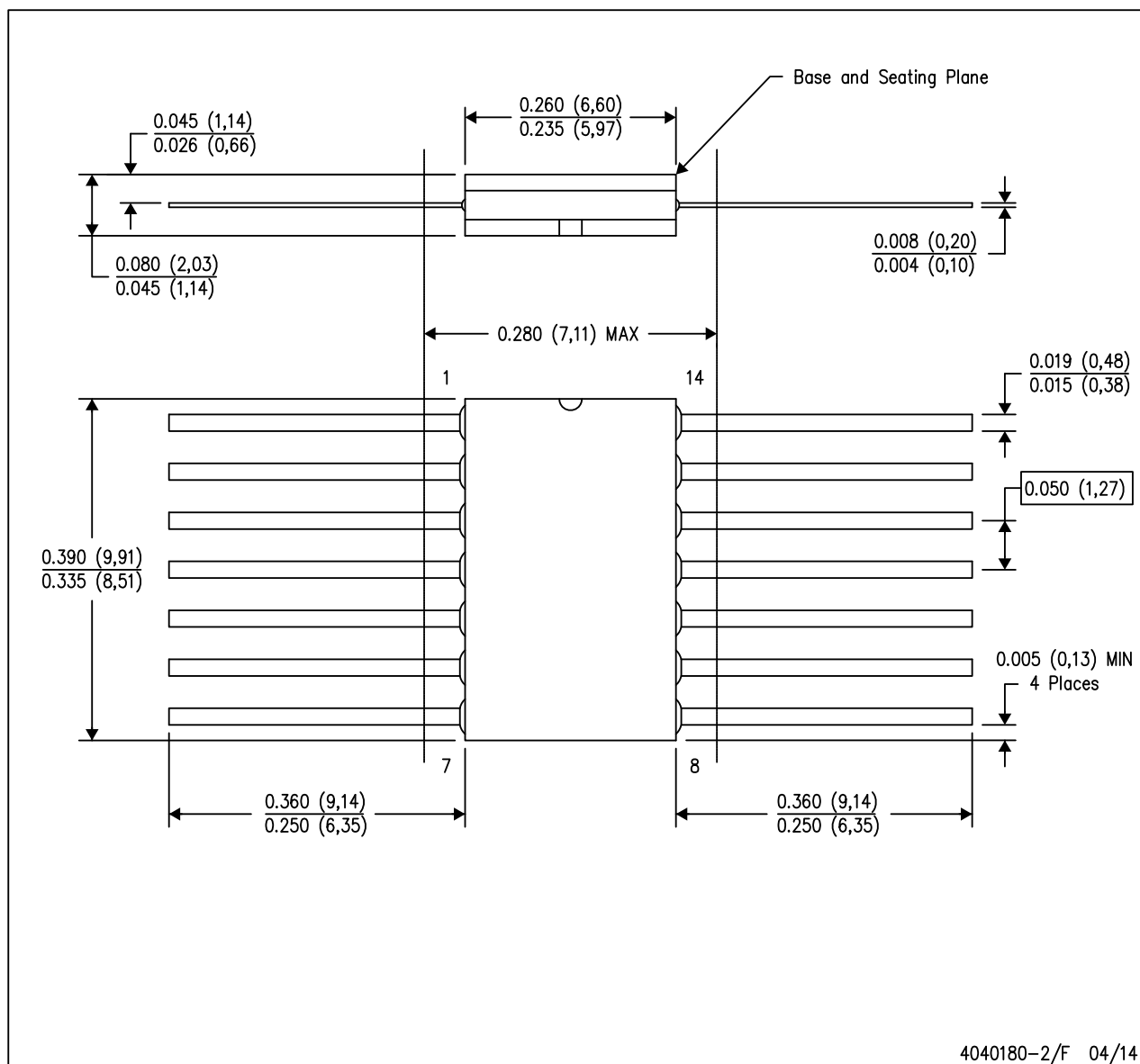
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

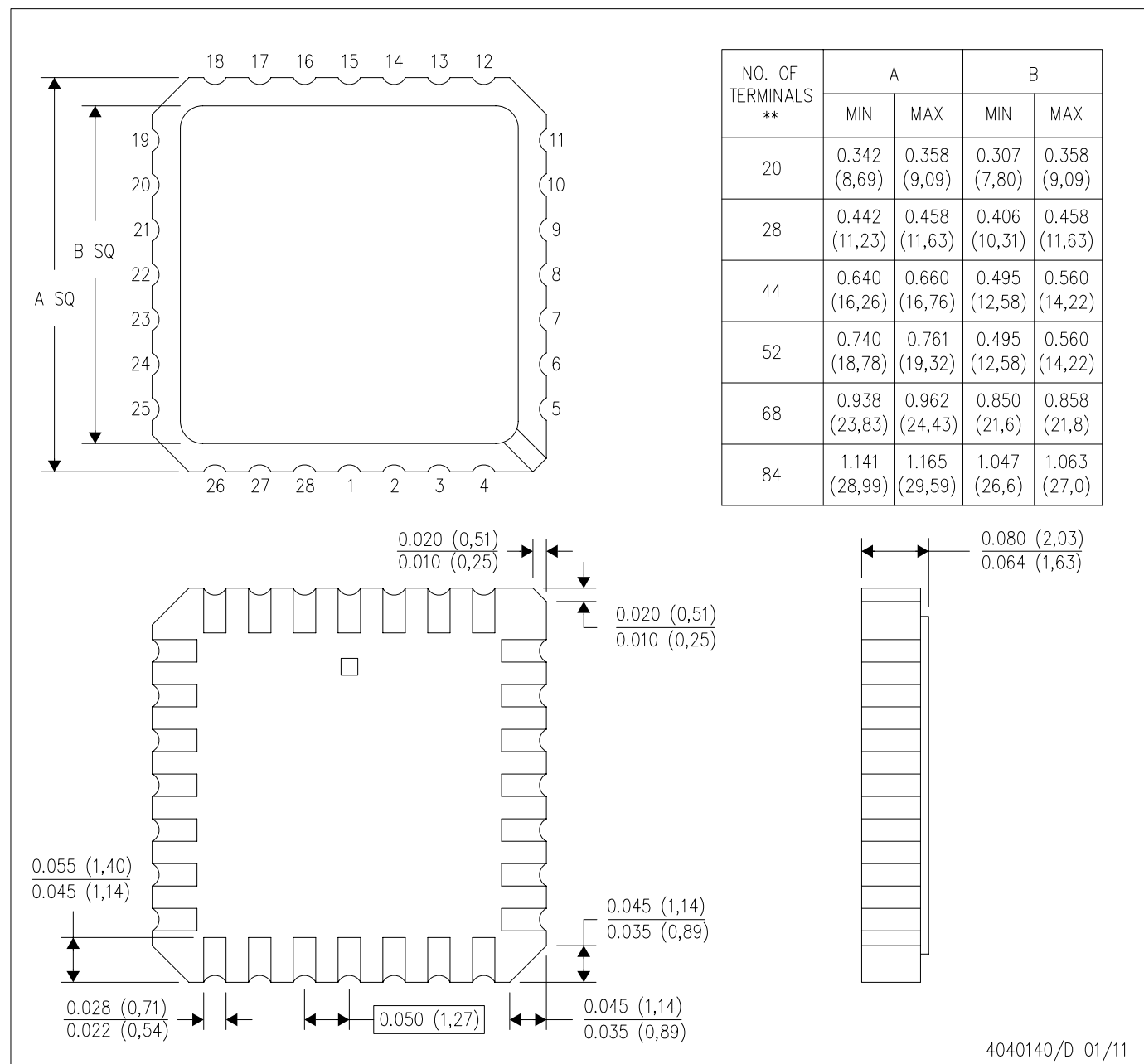


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 01/11

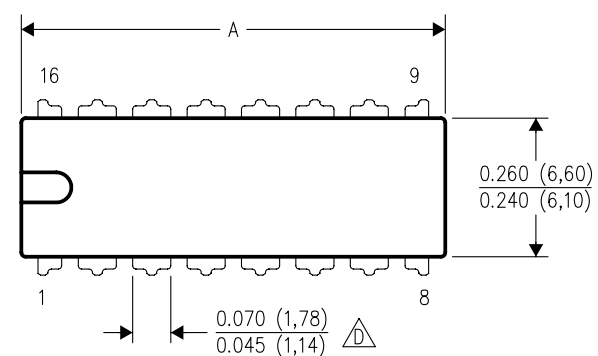
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

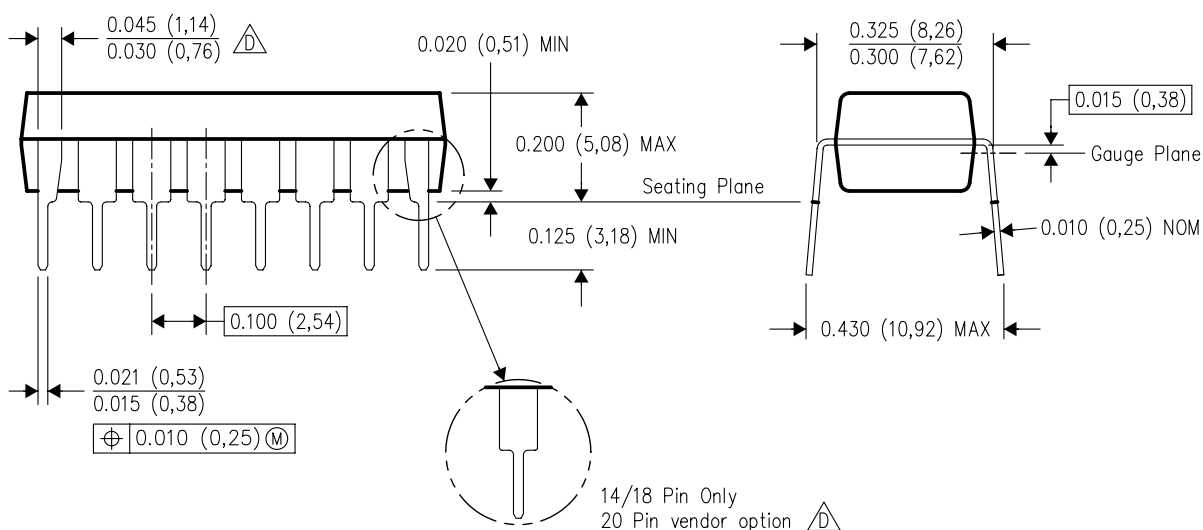
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

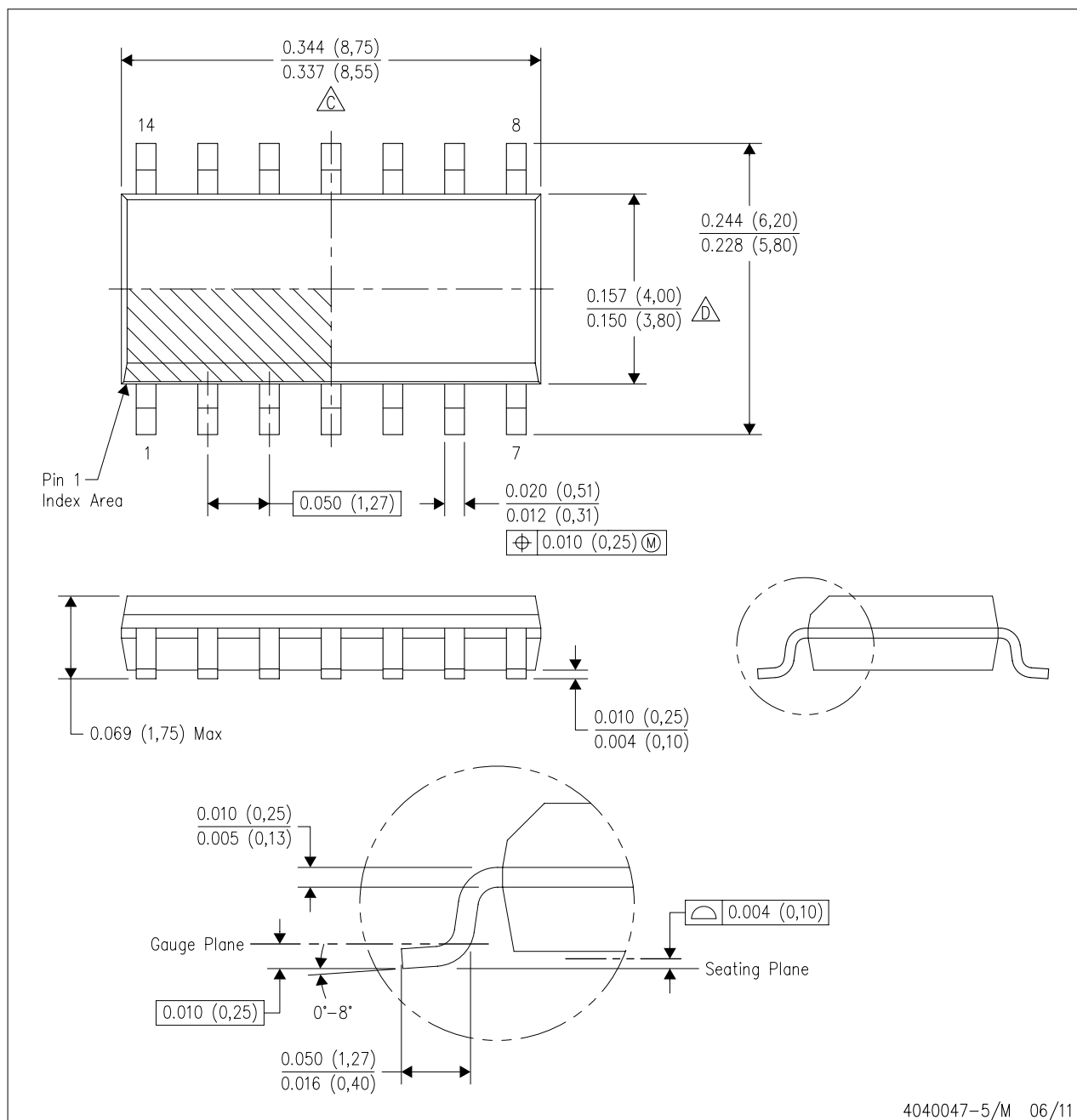
NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

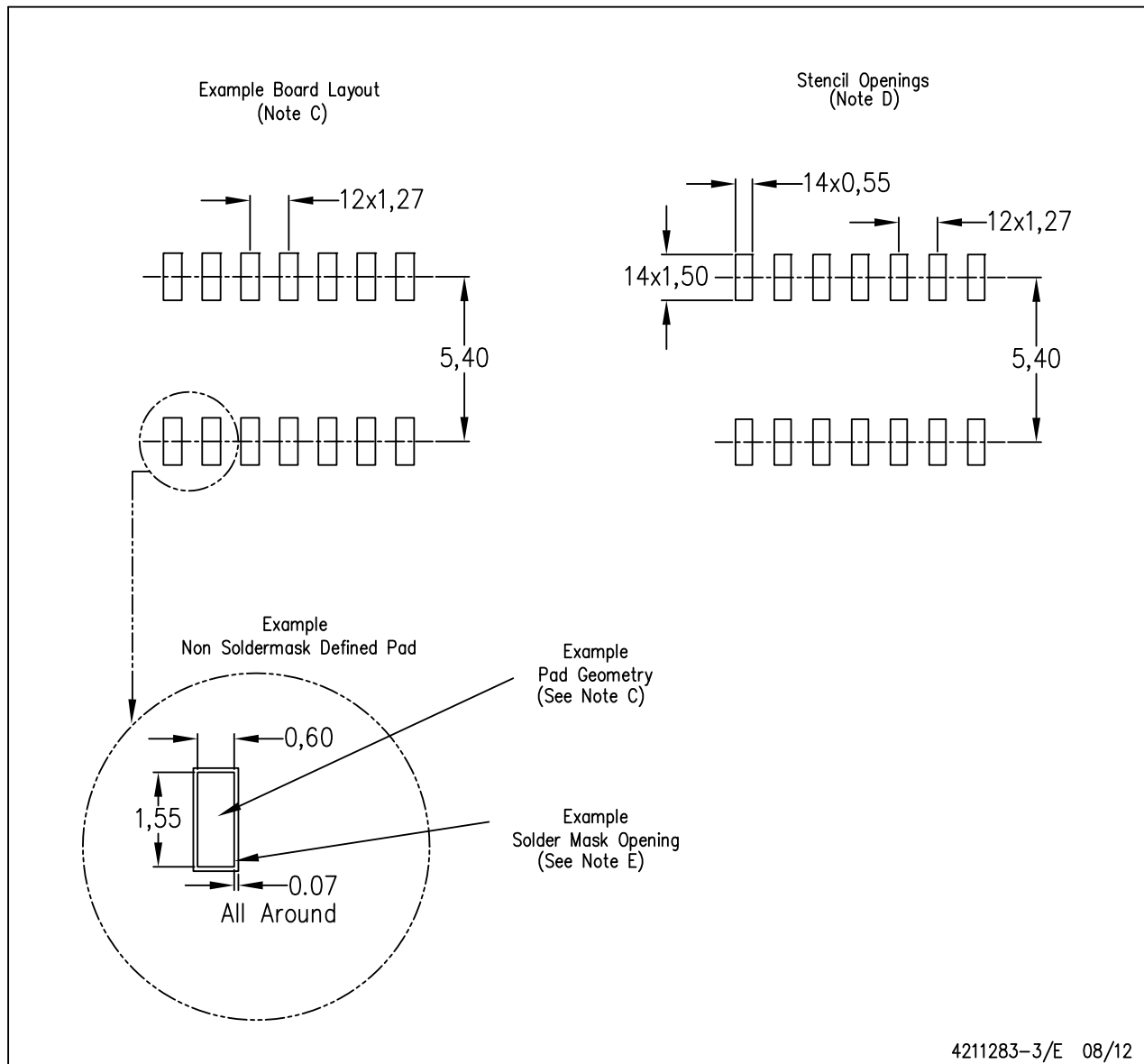


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - Reference JEDEC MS-012 variation AB.

LAND PATTERN DATA

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



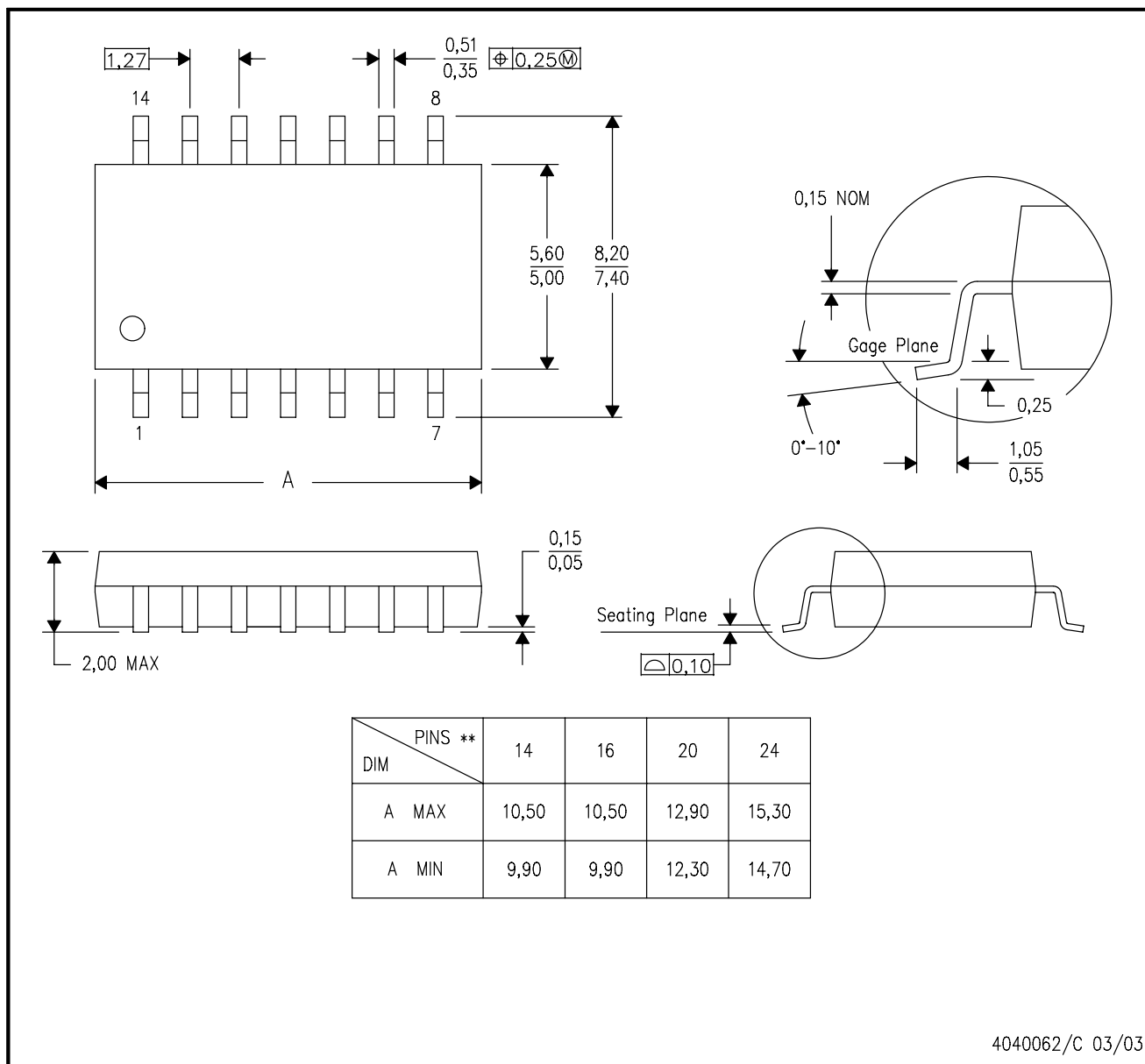
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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