

Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[Fairchild Semiconductor](#)
[FDS4897C](#)

For any questions, you can email us directly:

sales@integrated-circuit.com



November 2005

FDS4897C

Dual N & P-Channel PowerTrench® MOSFET

General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

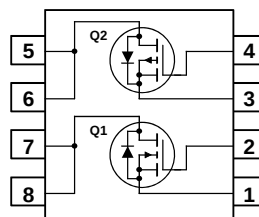
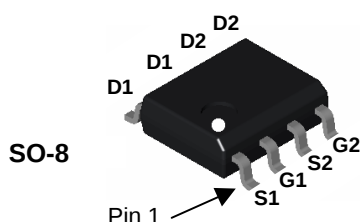
Application

- Inverter
- Power Supplies



Features

- **Q1:** N-Channel
6.2A, 40V $R_{DS(on)} = 29m\Omega @ V_{GS} = 10V$
 $R_{DS(on)} = 36m\Omega @ V_{GS} = 4.5V$
- **Q2:** P-Channel
-4.4A, -40V $R_{DS(on)} = 46m\Omega @ V_{GS} = -10V$
 $R_{DS(on)} = 63m\Omega @ V_{GS} = -4.5V$
- High power handling capability in a widely used surface mount package
- RoHS compliant



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V _{DSS}	Drain-Source Voltage	40	40	V
V _{GSS}	Gate-Source Voltage	±20	±20	V
I _D	Drain Current - Continuous (Note 1a)	6.2	−4.4	A
	- Pulsed	20	−20	
P _D	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1		
	(Note 1c)	0.9		
T _J , T _{STG}	Operating and Storage Junction Temperature Range	−55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS4897C	FDS4897C	13"	12mm	2500 units

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 3)							
E _{AS}	Drain-Source Avalanche Energy (Single Pulse)	V _{DD} = 40 V, I _D = 7.3 A, L = 1 mH	Q1			27	mJ
		V _{DD} = -40 V, I _D = -8.7 A, L = 1 mH	Q2			38	mJ
I _{AS}	Drain-Source Avalanche Current		Q1 Q2		7.3 -8.7		A
Off Characteristics							
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA V _{GS} = 0 V, I _D = -250 μA	Q1 Q2	40 -40			V
ΔBV _{DSS} ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C I _D = -250 μA, Referenced to 25°C	Q1 Q2		34 -40		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 32 V, V _{GS} = 0 V V _{DS} = -32 V, V _{GS} = 0 V	Q1 Q2			1 -1	μA
I _{GSS}	Gate-Body Leakage	V _{GS} = ±20 V, V _{DS} = 0 V	All			±100	nA
On Characteristics (Note 2)							
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA V _{DS} = V _{GS} , I _D = -250 μA	Q1 Q2	1 -1	1.9 -1.7	3 -3	V
ΔV _{GS(th)} ΔT _J	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C I _D = -250 μA, Referenced to 25°C	Q1 Q2		-5 4		mV/°C
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 6.2 A V _{GS} = 4.5 V, I _D = 4.8 A V _{GS} = 10 V, I _D = 6.2 A, T _J = 125°C V _{GS} = -10 V, I _D = -4.4 A V _{GS} = -4.5 V, I _D = -3.8 A V _{GS} = -10 V, I _D = -4.4 A, T _J = 125°C	Q1 Q2		21 26 29 37 50 55	29 36 43 46 63 73	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 6.2 A V _{DS} = -10 V, I _D = -4.4 A	Q1 Q2		21 12		S
Dynamic Characteristics							
C _{iss}	Input Capacitance	Q1 V _{DS} = 20 V, V _{GS} = 0 V, f = 1.0 MHz	Q1 Q2		760 1050		pF
C _{oss}	Output Capacitance	Q2	Q1 Q2		100 140		pF
C _{rss}	Reverse Transfer Capacitance	V _{DS} = -20 V, V _{GS} = 0 V, f = 1.0 MHz	Q1 Q2		60 70		pF
R _G	Gate Resistance	f = 1.0 MHz	Q1 Q2		1.2 9		Ω

Electrical Characteristics (continued)

$T_A = 25^\circ\text{C}$ unless otherwise noted

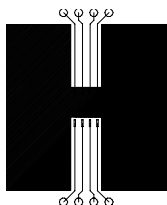
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 20\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$	Q1 Q2		9 12	18 22	ns
t_r	Turn-On Rise Time		Q1 Q2		5 15	10 27	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = -20\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$	Q1 Q2		23 45	37 72	ns
t_f	Turn-Off Fall Time		Q1 Q2		3 18	6 32	ns
Q_g	Total Gate Charge	Q1 $V_{DS} = 20\text{ V}, I_D = 6.2\text{ A}, V_{GS} = 10\text{ V}$	Q1 Q2		14 20	20 28	nC
Q_{gs}	Gate-Source Charge	Q2	Q1 Q2		2.4 3		nC
Q_{gd}	Gate-Drain Charge	$V_{DS} = -20\text{ V}, I_D = -4.4\text{ A}, V_{GS} = -10\text{ V}$	Q1 Q2		2.8 4		nC

Drain-Source Diode Characteristics

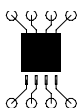
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)	Q1 Q2		0.7 -0.7	1.2 -1.2	V
t_{rr}	Diode Reverse Recovery Time	Q1 $I_F = 6.2\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2		17 24		ns
Q_{rr}	Diode Reverse Recovery Charge	Q2 $I_F = -4.4\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2		7 12		nC

Notes:

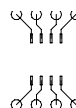
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $78^\circ\text{C}/\text{W}$ when mounted on a 0.5 in^2 pad of 2 oz copper



b) $125^\circ\text{C}/\text{W}$ when mounted on a $.02\text{ in}^2$ pad of 2 oz copper



c) $135^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty Cycle $< 2.0\%$

3. BV(avalanche) Single-Pulse rating is guaranteed by design if device is operated within the UIS SOA boundary of the device.

Typical Characteristics: Q1 (N-Channel)

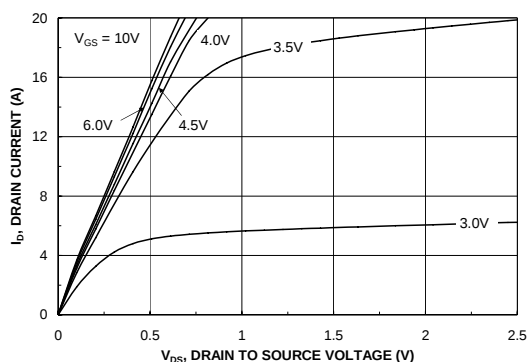


Figure 1. On-Region Characteristics.

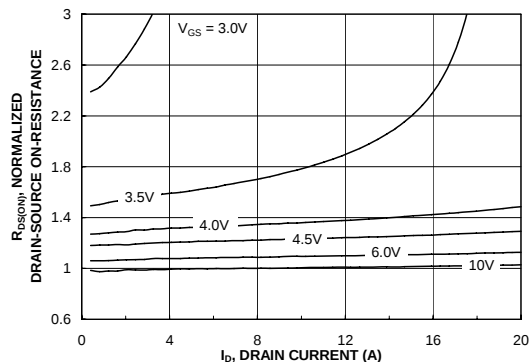


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

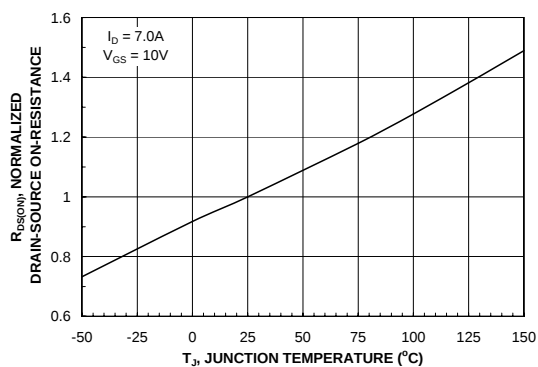


Figure 3. On-Resistance Variation with Temperature.

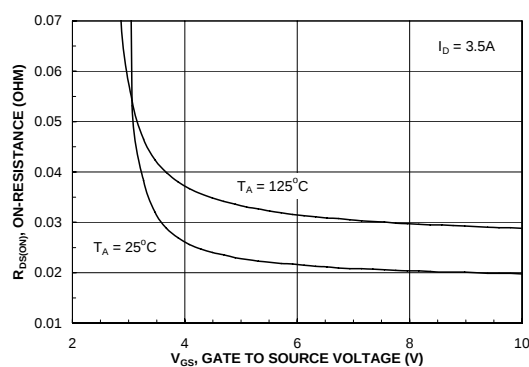


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

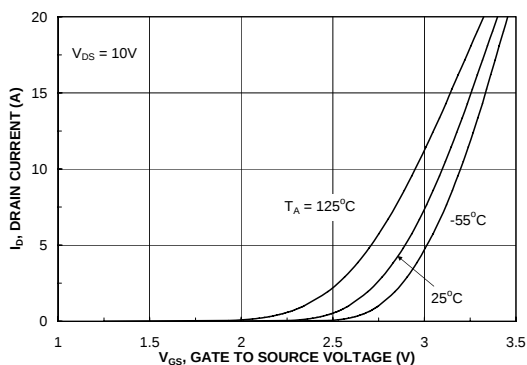


Figure 5. Transfer Characteristics.

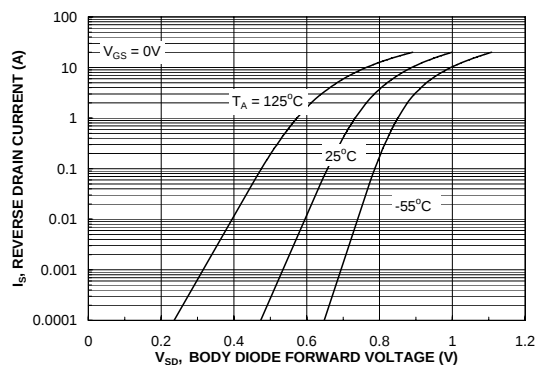


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q1 (N-Channel)

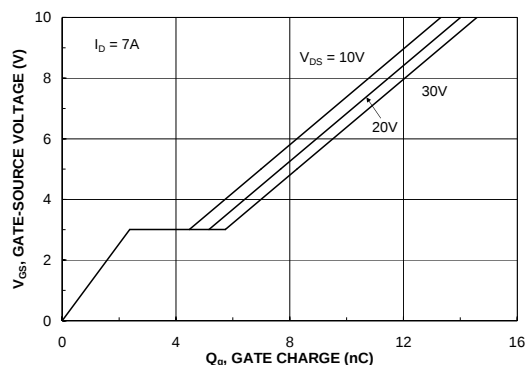


Figure 7. Gate Charge Characteristics.

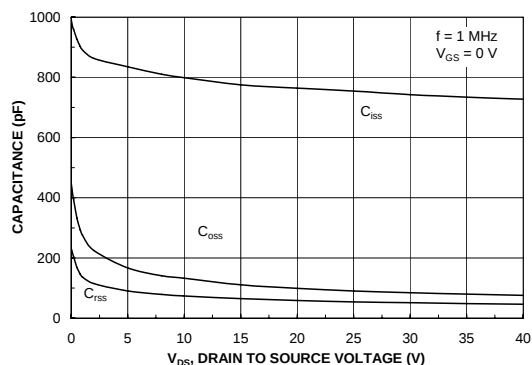


Figure 8. Capacitance Characteristics.

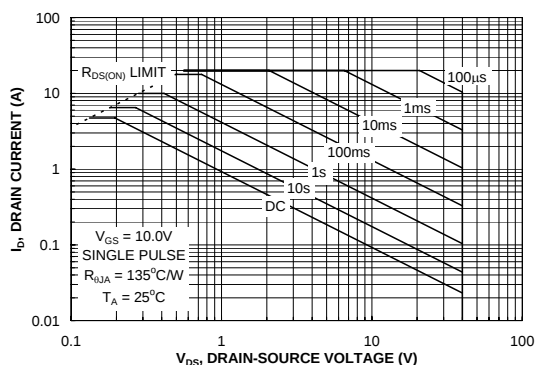


Figure 9. Maximum Safe Operating Area.

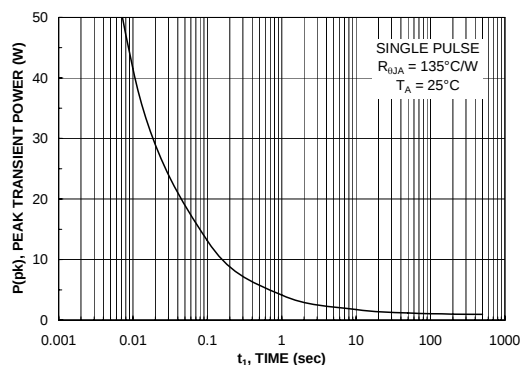


Figure 10. Single Pulse Maximum Power Dissipation.

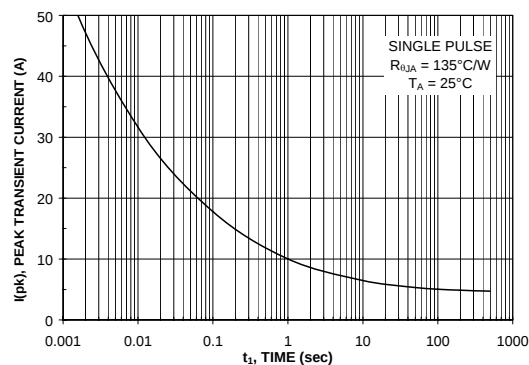


Figure 11. Single Pulse Maximum Peak Current.

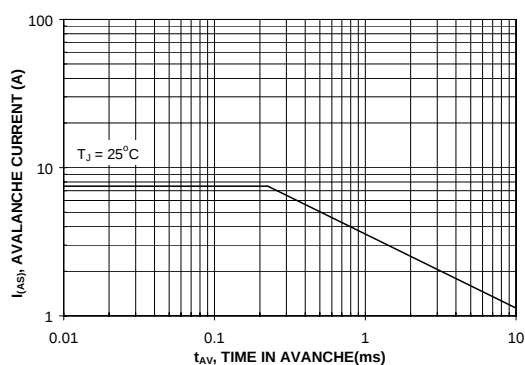


Figure 12. Unclamped Inductive Switching Capability.

Typical Characteristics: Q2 (P-Channel)

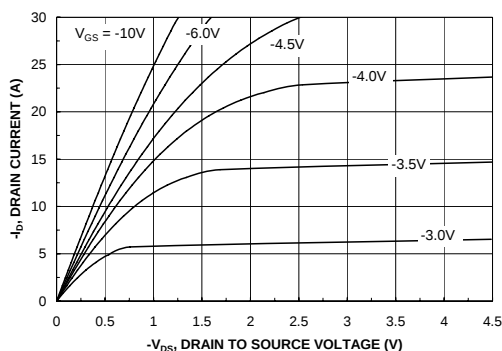


Figure 13. On-Region Characteristics.

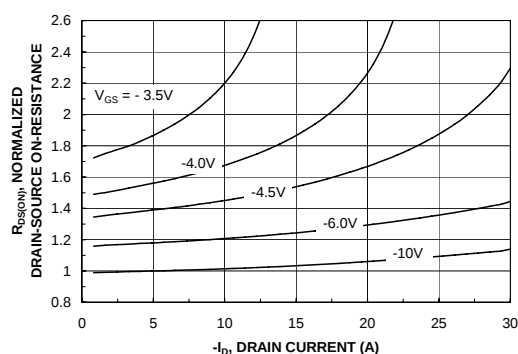


Figure 14. On-Resistance Variation with Drain Current and Gate Voltage.

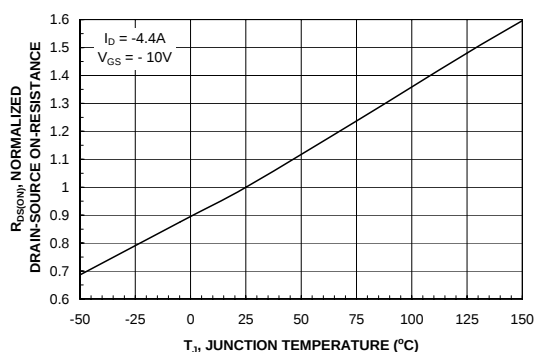


Figure 15. On-Resistance Variation with Temperature.

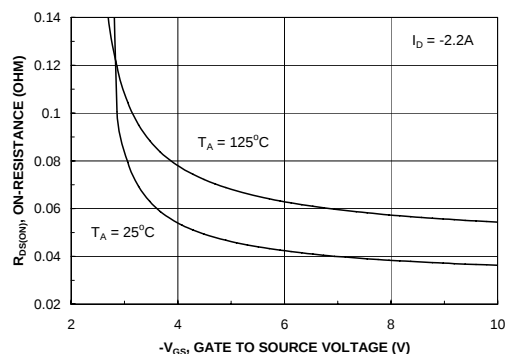


Figure 16. On-Resistance Variation with Gate-to-Source Voltage.

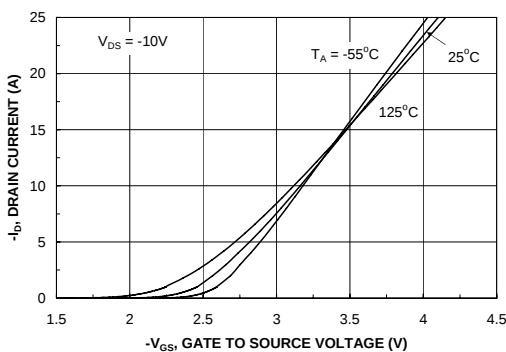


Figure 17. Transfer Characteristics.

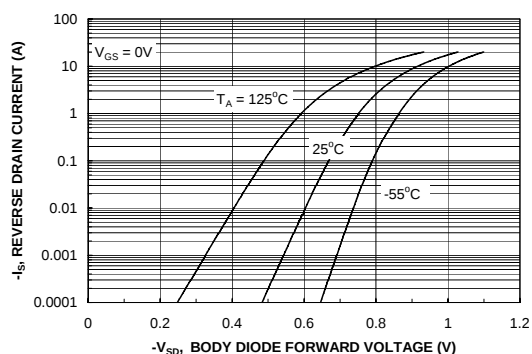


Figure 18. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2 (P-Channel)

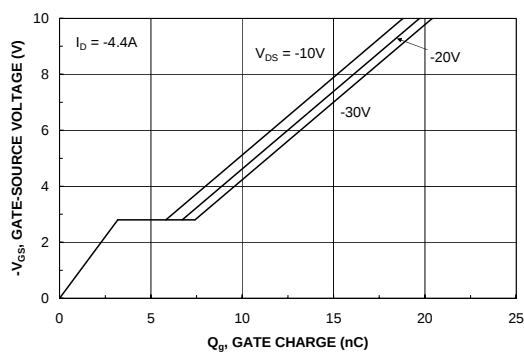


Figure 19. Gate Charge Characteristics.

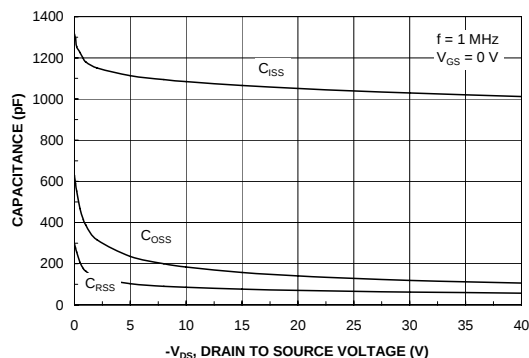


Figure 20. Capacitance Characteristics.

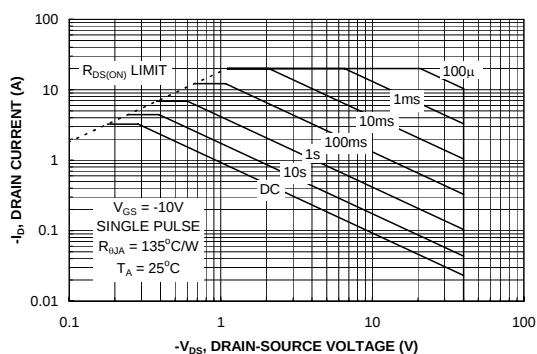


Figure 21. Maximum Safe Operating Area.

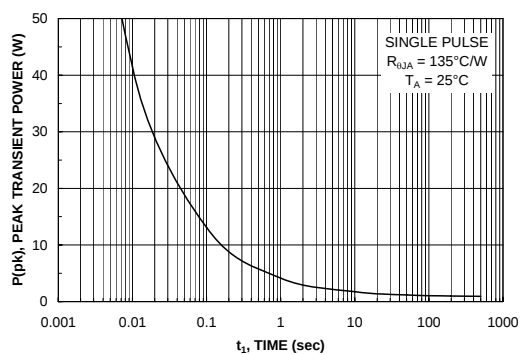


Figure 22. Single Pulse Maximum Power Dissipation.

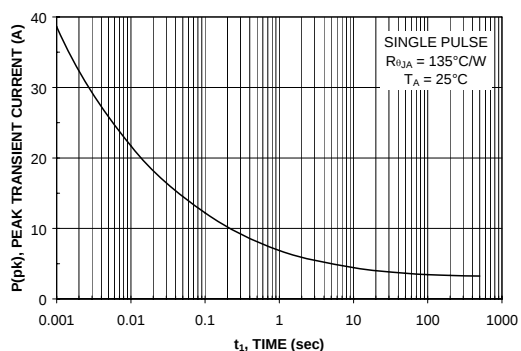


Figure 23. Single Pulse Maximum Peak Current

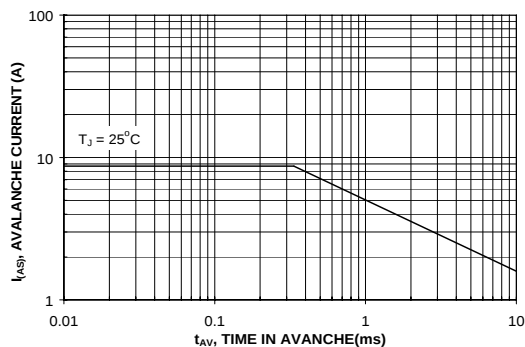


Figure 24. Unclamped Inductive Switching Capability

Typical Characteristics : N and P-Channel

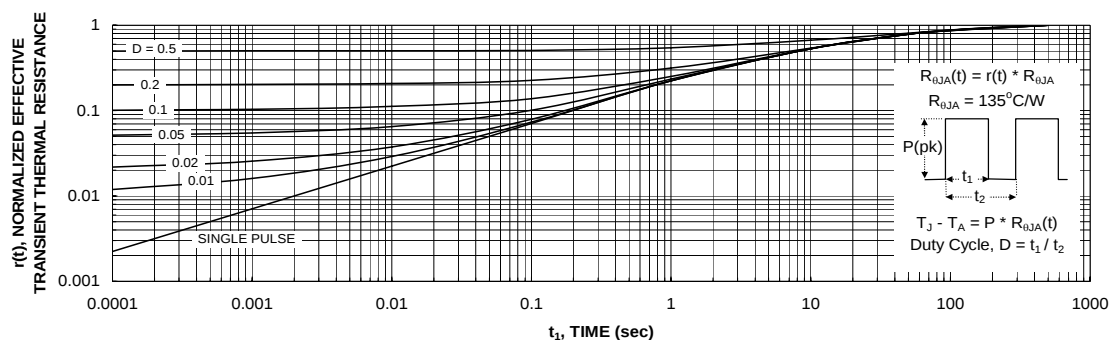


Figure 25. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE [™]	FAST [®]	ISOPLANAR [™]	PowerSaver [™]	SuperSOT [™] -6
ActiveArray [™]	FAST [™]	LittleFET [™]	PowerTrench [®]	SuperSOT [™] -8
Bottomless [™]	FPS [™]	MICROCOUPLER [™]	QFET [®]	SyncFET [™]
Build it Now [™]	FRFET [™]	MicroFET [™]	QS [™]	TinyLogic [®]
CoolFET [™]	GlobalOptoisolator [™]	MicroPak [™]	QT Optoelectronics [™]	TINYOPTO [™]
CROSSVOLT [™]	GTO [™]	MICROWIRE [™]	Quiet Series [™]	TruTranslation [™]
DO [™]	HiSeC [™]	MSX [™]	RapidConfigure [™]	UHC [™]
EcoSPARK [™]	I ² C [™]	MSXPro [™]	RapidConnect [™]	UltraFET [®]
E ² C [™]	i-Lo [™]	OCX [™]	μSerDes [™]	UniFET [™]
EnSigna [™]	ImpliedDisconnect [™]	OCXPro [™]	ScalarPump [™]	VCX [™]
FACT [™]	IntelliMAX [™]	OPTOLOGIC [®]	SILENT SWITCHER [®]	Wire [™]
FACT Quiet Series [™]		OPTOPLANAR [™]	SMART START [™]	
Across the board. Around the world. [™]		PACMAN [™]	SPM [™]	
The Power Franchise [®]		POP [™]	Stealth [™]	
Programmable Active Droop [™]		Power247 [™]	SuperFET [™]	
		PowerEdge [™]	SuperSOT [™] -3	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.