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June 2014

## FCA47N60 / FCA47N60\_F109

### N-Channel SuperFET<sup>®</sup> MOSFET

600 V, 47 A, 70 mΩ

#### Features

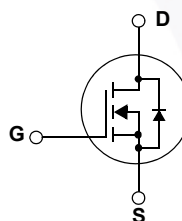
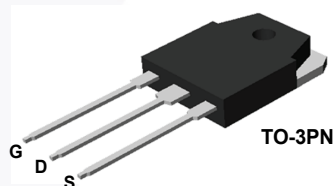
- 650 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 58\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 210\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 420\text{ pF}$ )
- 100% Avalanche Tested

#### Application

- Solar Invertor
- AC-DC Power Supply

#### Description

SuperFET<sup>®</sup> MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance,  $dv/dt$  rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



#### Absolute Maximum Ratings

Symbol	Parameter	FCA47N60	FCA47N60_F109	Unit
$V_{DSS}$	Drain-Source Voltage		600	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	47 29.7		A
$I_{DM}$	Drain Current - Pulsed (Note 1)	141		A
$V_{GSS}$	Gate-Source voltage	$\pm 30$		V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	1800		mJ
$I_{AR}$	Avalanche Current (Note 1)	47		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	41.7		mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	4.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	417 3.33		W W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$

#### Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	--	0.3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	--	41.7	$^\circ\text{C/W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCA47N60	FCA47N60	TO-3PN	-	-	30
FCA47N60	FCA47N60_F109	TO-3PN	-	-	30

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}, T_J = 25^\circ\text{C}$	600	--	--	V
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}, T_J = 150^\circ\text{C}$	--	650	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.6	--	V/ $^\circ\text{C}$
$BV_{DS}$	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 47\text{ A}$	--	700	--	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	--	5.0	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 23.5\text{ A}$	--	0.058	0.07	
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 23.5\text{ A}$	--	40	--	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	--	5.0	

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	--	5900	8000	pF
$C_{oss}$	Output Capacitance		--	3200	4200	pF
$C_{rss}$	Reverse Transfer Capacitance		--	250	--	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	--	160	--	pF
$C_{oss\text{ eff.}}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	--	420	--	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 47\text{ A}$ $R_G = 25\text{ }\Omega$	--	185	430	ns
$t_r$	Turn-On Rise Time		--	210	450	ns
$t_{d(off)}$	Turn-Off Delay Time	(Note 4)	--	520	1100	ns
$t_f$	Turn-Off Fall Time		--	75	160	ns
$Q_g$	Total Gate Charge	$V_{DS} = 480\text{ V}, I_D = 47\text{ A}$ $V_{GS} = 10\text{ V}$	--	210	270	nC
$Q_{gs}$	Gate-Source Charge		--	38	--	nC
$Q_{gd}$	Gate-Drain Charge		--	110	--	nC

### Drain-Source Diode Characteristics

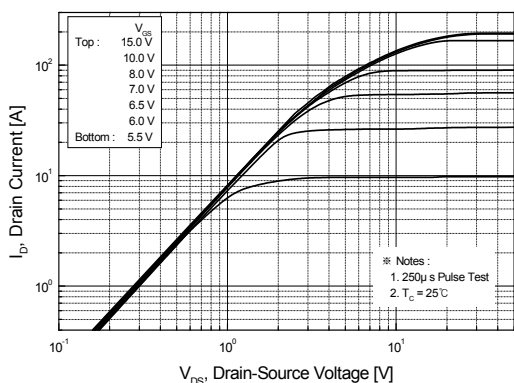
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	47	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	141	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 47 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 47 A	--	590	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di <sub>F</sub> /dt =100 A/μs (Note 4)	--	25	--	μC

#### Notes:

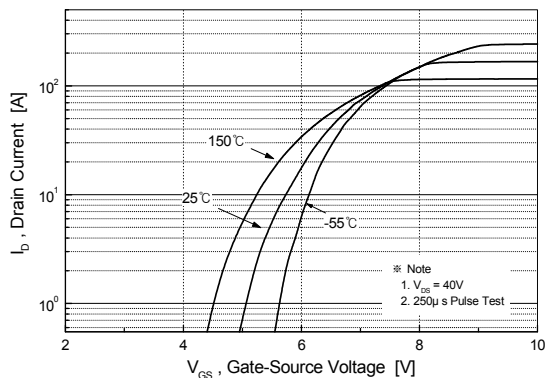
1. Repetitive Rating: Pulse-width limited by maximum junction temperature.
2.  $I_{AS} = 18\text{ A}, R_G = 25\text{ }\Omega$ , starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 47\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} = 380\text{ V}$ , starting  $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature typical characteristics.

## Typical Characteristics

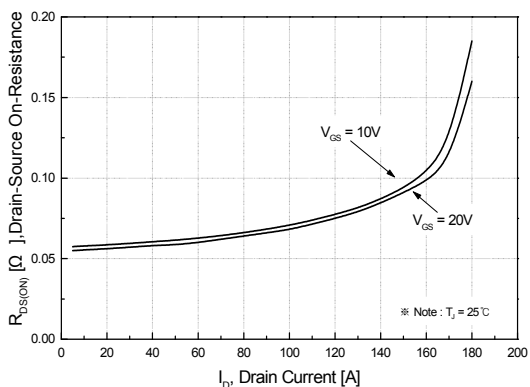
**Figure 1. On-Region Characteristics**



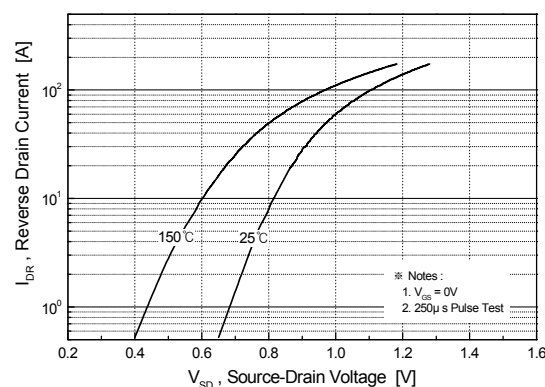
**Figure 2. Transfer Characteristics**



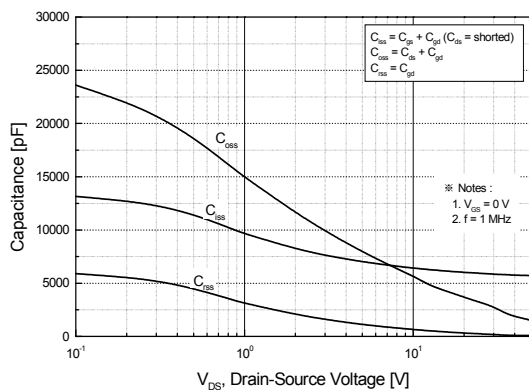
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



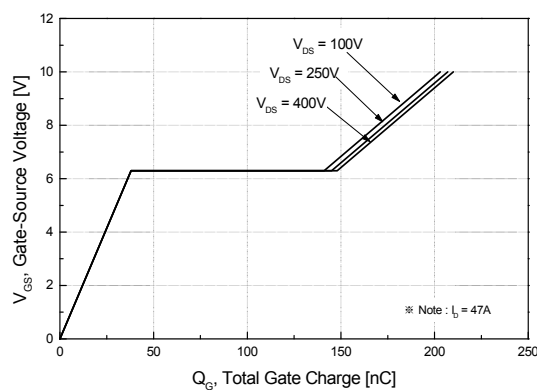
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

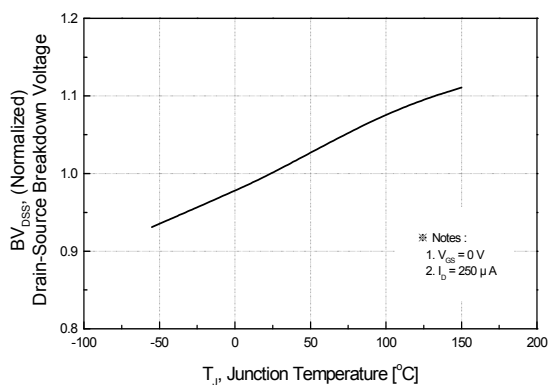


**Figure 6. Gate Charge Characteristics**

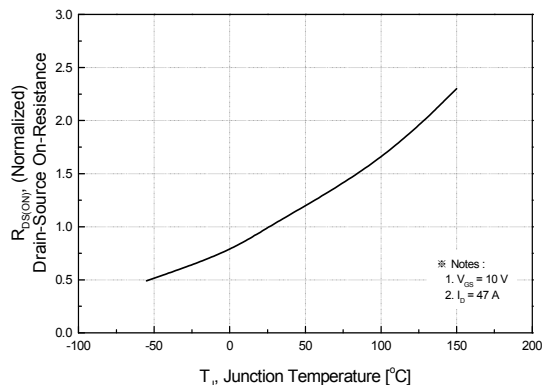


## Typical Characteristics (Continued)

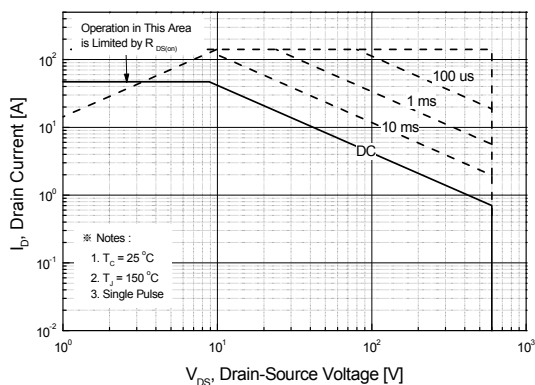
**Figure 7. Breakdown Voltage Variation vs. Temperature**



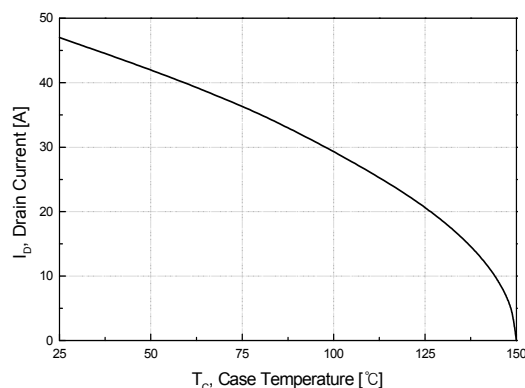
**Figure 8. On-Resistance Variation vs. Temperature**



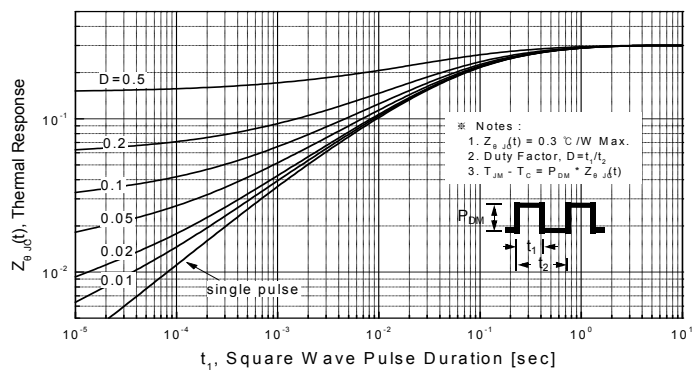
**Figure 9. Safe Operating Area**



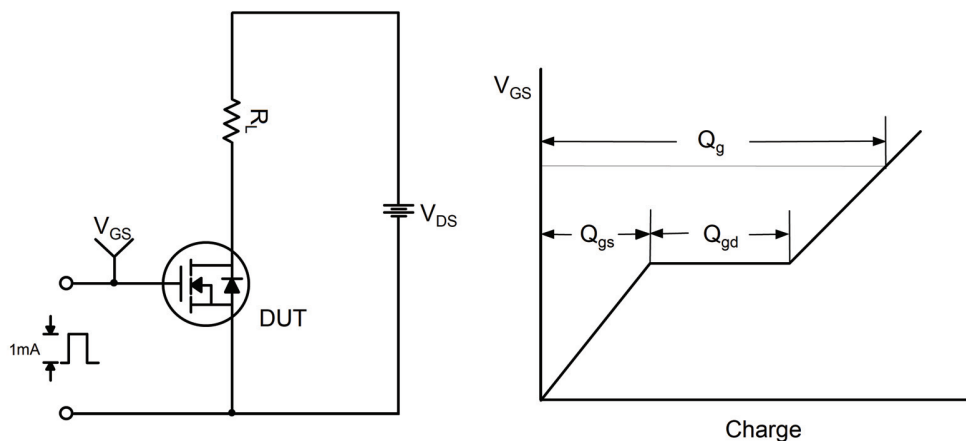
**Figure 10. Maximum Drain Current vs. Case Temperature**



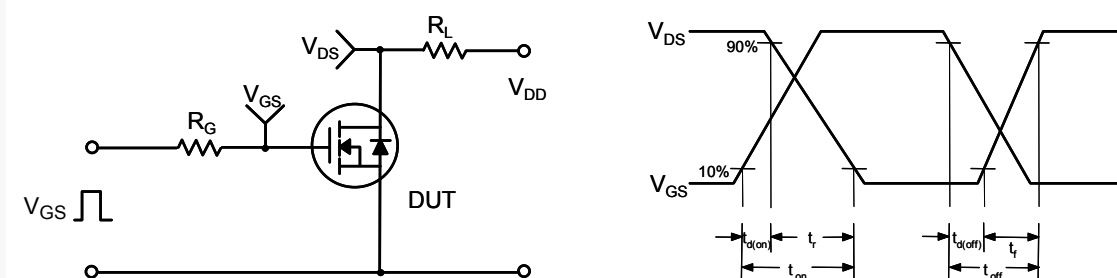
**Figure 11. Transient Thermal Response Curve**



**Figure 12. Gate Charge Test Circuit & Waveform**



**Figure 13. Resistive Switching Test Circuit & Waveforms**



**Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms**

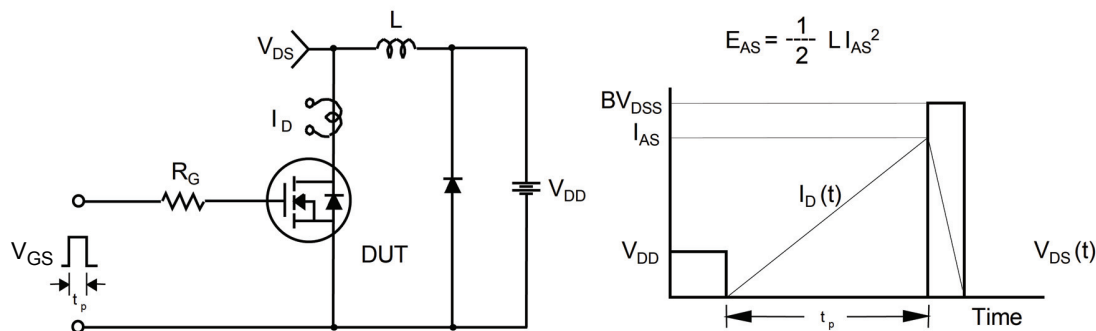
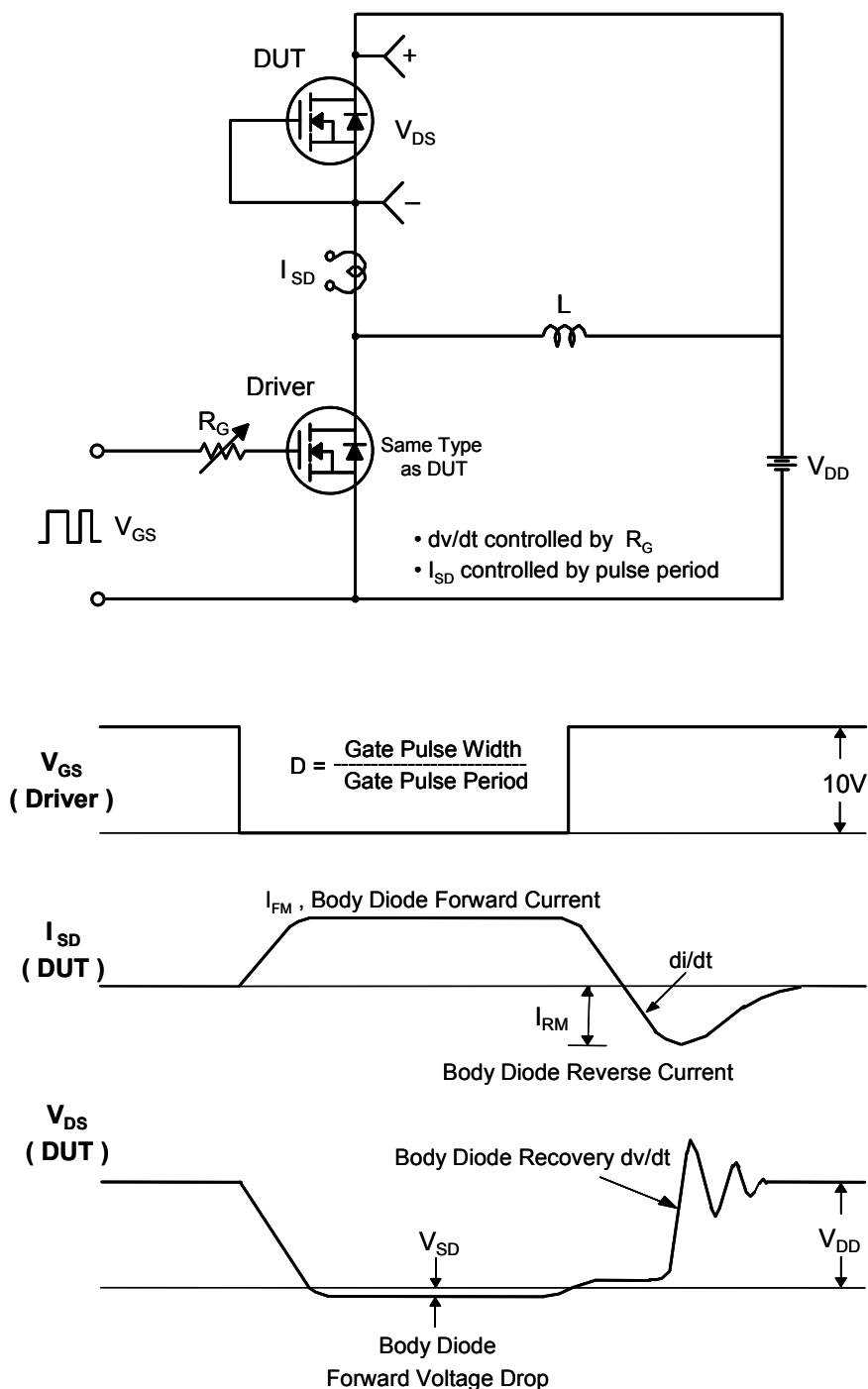


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms









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