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Vishay/Siliconix SUD19P06-60-GE3

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SUD19P06-60

Vishay Siliconix

P-Channel 60 V (D-S) MOSFET

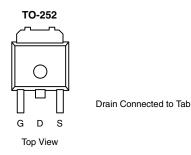
PRODUCT SUMMARY						
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A) ^d	Q _g (Typ)			
- 60	0.060 at V _{GS} = - 10 V	- 19	26			
	0.077 at V _{GS} = - 4.5 V	- 16.8	20			

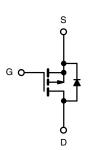
FEATURES

- Halogen-free According to IEC 61249-2-21
 Definition
- TrenchFET[®] Power MOSFET
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- High Side Switch for Full Bridge Converter
- DC/DC Converter for LCD Display





Ordering Information: SUD19P06-60-E3 (Lead (Pb)-free) P-Cha

SUD19P06-60-GE3 (Lead (Pb)-free and Halogen free)

P-Channel MOSFET

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V _{DS}	- 60	v		
Gate-Source Voltage		V _{GS}	± 20	V	
Continuous Drain Current (T _{.1} = 150 °C)	T _C = 25 °C	1-	- 18.3		
	T _C = 125 °C	ID –	- 8.19	А	
Pulsed Drain Current		I _{DM}	- 30		
Avalanche Current, Single Pulse	L = 0.1 mH	I _{AS}	- 22		
Repetitive Avalanche Energy, Single Pulse ^a	L = 0.1 MH	E _{AS}	24.2	mJ	
Power Dissinction	T _C = 25 °C	P _D	38.5 ^c	w	
Power Dissipation	T _A = 25 °C	'D	2.3 ^{b, c}	- ~~	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum lunction to Ambient	t ≤ 10 s	R _{thJA}	17	21		
Maximum Junction-to-Ambient ^o	Steady State	''thJA	45	55	°C/W	
Maximum Junction-to-Case		R _{thJC}	2.7	3.25		

Notes:

a. Duty cycle \leq 1 %.

b. When mounted on 1" square PCB (FR-4 material).

c. See SOA curve for voltage derating.

d. Based up on T_C = 25 °C.

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SPECIFICATIONS ($T_J = 25 \ ^{\circ}C$,	unless otherw	vise note)					
Parameter	Symbol	Test Conditions	Min .	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V_{GS} = 0 V, I_D = - 250 μ A	- 60			V	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$	- 1		- 3	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
		$V_{DS} = -60 \text{ V}, V_{GS} = 0 \text{ V}$			- 1	μΑ	
Zero Gate Voltage Drain Current	I _{DSS}	V_{DS} = - 60 V, V_{GS} = 0 V, T_{J} = 125 °C			- 50		
		V_{DS} = - 60 V, V_{GS} = 0 V, T_{J} = 150 ° C			- 125	1	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = -5 V, V_{GS} = -10 V$	- 30			А	
		V _{GS} = - 10 V, I _D = - 10 A		0.048	0.060		
Durin Courses On Otata Desistance	R _{DS(on)}	V_{GS} = - 10 V, I _D = - 10 A, T _J = 125 °C			0.102		
Drain-Source On-State Resistance ^a	US(on)	V_{GS} = - 10 V, I _D = - 10 A, T _J = 150 °C			0.120	0.120 Ω	
		V _{GS} = - 4.5 V, I _D = - 5 A		0.061	0.077		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 15 V, I _D = - 10 A		22		S	
Dynamic ^b							
Input Capacitance	C _{iss}			1140	1710	pF	
Output Capacitance	C _{oss}	V_{GS} = 0 V, V_{DS} = - 25 V, f = 1 MHz		130			
Reverse Transfer Capacitance	C _{rss}			90			
Total Gate Charge ^c	Qg			26	40	nC	
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = -30$ V, $V_{GS} = -10$ V, $I_{D} = -10$ A		4.5			
Gate-Drain Charge ^c	Q _{gd}]		7		1	
Gate Resistance	Rg	f = 1 MHz		7		Ω	
Turn-On Delay Time ^c	t _{d(on)}			8	15		
Rise Time ^c	t _r	V_{DD} = - 30 V, R _L = 3 Ω		9	15	ns	
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong$ - 19 A, V_{GEN} = - 10 V, R_g = 2.5 Ω		65	100		
Fall Time ^c	t _f	1		30	45		
Drain-Source Body Diode and Characte	eristics (T _C = 2	5 °C) ^b					
Continuous Current	I _S				- 30		
Pulsed Current	I _{SM}				- 30	A	
Forward Voltage ^a	V _{SD}	I _F = - 19 A, V _{GS} = 0 V		- 1	- 1.5	V	
Reverse Recovery Time	t _{rr}	I _F = - 19 A, di/dt = 100 A/μs		41	61	ns	
	1						

Notes:

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

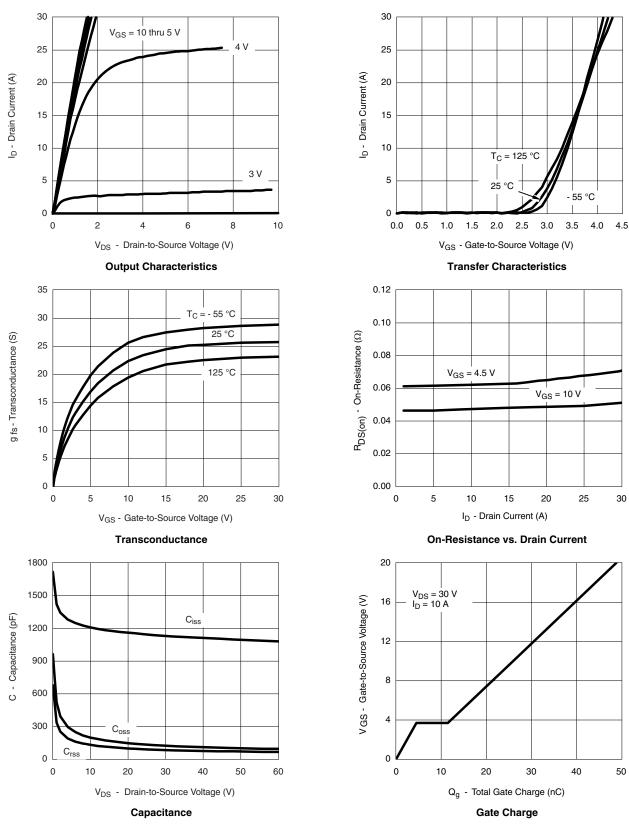
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

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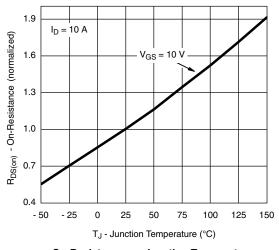


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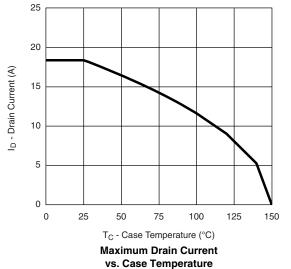
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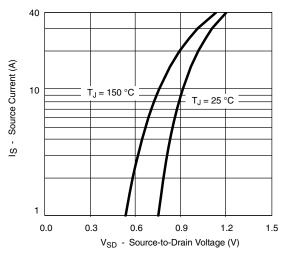
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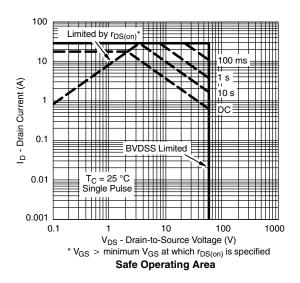


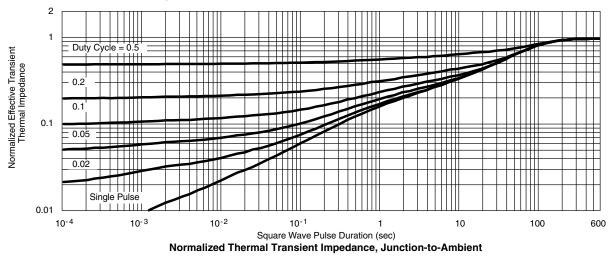






Source-Drain Diode Forward Voltage





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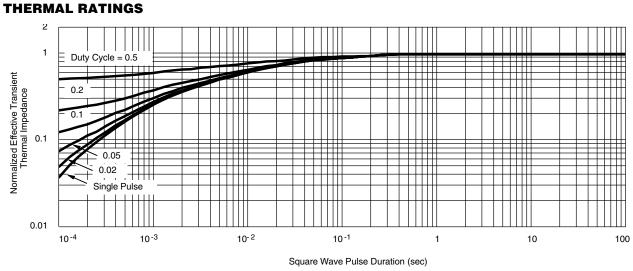
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Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69253.

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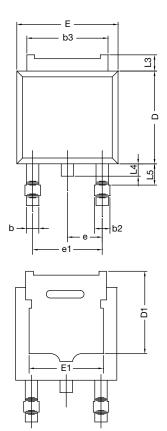




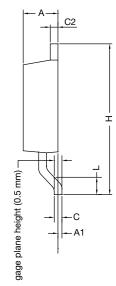
Package Information

Vishay Siliconix

Document Number: 71197



TO-252AA Case Outline



	MILLIN	IETERS	INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
А	2.18	2.38	0.086	0.094	
A1	-	0.127	-	0.005	
b	0.64	0.88	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	
С	0.46	0.61	0.018	0.024	
C2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	
D1	4.10	-	0.161	-	
E	6.35	6.73	0.250	0.265	
E1	4.32	-	0.170	-	
Н	9.40	10.41	0.370	0.410	
е	2.28	BSC	0.090 BSC		
e1	4.56	BSC	0.180 BSC		
L	1.40	1.78	0.055	0.070	
L3	0.89	1.27	0.035	0.050	
L4	-	1.02	-	0.040	
L5	1.01	1.52	0.040	0.060	
ECN: T16- DWG: 534	0236-Rev. P, ⁻ 7	16-May-16			

Notes

• Dimension L3 is for reference only.

Revision: 16-May-16

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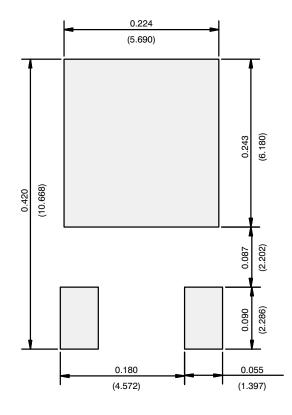




Application Note 826

Vishay Siliconix

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads Dimensions in Inches/(mm)

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