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EM6M1T2R

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Transistors

2.5V Drive Nch+Pch MOSFET

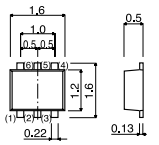
EM6M1

●Structure
Silicon N-channel MOSFET /
Silicon P-channel MOSFET

●Features
1) Nch MOSFET and Pch MOSFET are put in EMT6 package.
2) High-speed switching.
3) Low voltage drive (2.5V drive).
4) Built-in G-S Protection Diode.

●Dimensions (Unit : mm)

EMT6



Each lead has same dimensions

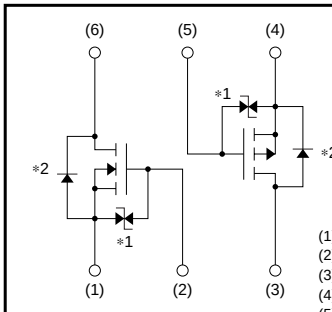
Abbreviated symbol : M01

●Applications
Switching

●Packaging specifications

Type	Package	Taping
	Code	T2R
	Basic ordering unit (pieces)	8000
EM6M1		○

●Inner circuit



∗1 ESD PROTECTION DIODE
∗2 BODY DIODE

(1) Tr1 (Nch) Source
(2) Tr1 (Nch) Gate
(3) Tr2 (Pch) Drain
(4) Tr2 (Pch) Source
(5) Tr2 (Pch) Gate
(6) Tr1 (Nch) Drain

●Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits		Unit
			Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage		V_{DSS}	30	−20	V
Gate-source voltage		V_{GSS}	±20	±12	V
Drain current	Continuous	I_D	±0.1	±0.2	A
	Pulsed	I_{DP} ∗1	±0.4	±0.4	A
Power dissipation		P_D ∗2	150		mW / TOTAL
			120		mW / ELEMENT
Channel temperature		Tch	150		°C
Range of storage temperature		Tstg	−55 to +150		°C

∗1 Pw≦10μs, Duty cycle≦1%
∗2 Mounted on a ceramic board

●Notice
This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

Transistors

N-ch

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±1	μA	V_{GS}= ±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	30	–	–	V	I_D=10μA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	1	μA	V_{DS}=30V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	0.8	–	1.5	V	V_{DS}=3V, I_D=100μA
Static drain-source on-state resistance	$R_{DS\ (on)}$ *	–	5	8	Ω	I_D=10mA, V_{GS}=4V
		–	7	13	Ω	I_D=1mA, V_{GS}=2.5V
Forward transfer admittance	$\|Y_{fs}\|$ *	20	–	–	mS	V_{DS}=3V, I_D=10mA
Input capacitance	C_{iss}	–	13	–	pF	V_{DS}=5V
Output capacitance	C_{oss}	–	9	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	4	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	15	–	ns	V_{DD}≒5V
Rise time	t_r *	–	35	–	ns	I_D=10mA
Turn-off delay time	$t_{d\ (off)}$ *	–	80	–	ns	V_{GS}=5V
Fall time	t_f *	–	80	–	ns	R_L=500Ω R_G=10Ω
Total gate charge	Q_g *	–	0.9	–	nC	V_{DD}≒15V, I_D=0.1A
Gate-source charge	Q_{gs} *	–	0.2	–	nC	V_{GS}=4.5V
Gate-drain charge	Q_{gd} *	–	0.2	–	nC	R_L=150Ω, R_G=10Ω

*Pulsed

P-ch

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±10	μA	V_{GS}= ±12V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	–20	–	–	V	I_D= –1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	V_{DS}= –20V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	–0.7	–	–2.0	V	V_{DS}= –10V, I_D= –1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$ *	–	1.0	1.5	Ω	I_D= –0.2A, V_{GS}= –4.5V
		–	1.1	1.6	Ω	I_D= –0.2A, V_{GS}= –4V
		–	2.0	3.0	Ω	I_D= –0.2A, V_{GS}= –2.5V
Forward transfer admittance	$\|Y_{fs}\|$ *	0.2	–	–	S	V_{DS}= –10V, I_D= –0.15A
Input capacitance	C_{iss}	–	50	–	pF	V_{DS}= –10V
Output capacitance	C_{oss}	–	5	–	pF	V_{GS}= 0V
Reverse transfer capacitance	C_{rss}	–	5	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	9	–	ns	V_{DD}≒ –15V
Rise time	t_r *	–	6	–	ns	I_D= –0.15A
Turn-off delay time	$t_{d\ (off)}$ *	–	35	–	ns	V_{GS}= –4.5V R_L= 100Ω
Fall time	t_f *	–	45	–	ns	R_G= 10Ω
Total gate charge	Q_g *	–	1.2	–	nC	V_{DD}≒ –15V, I_D= –0.2A
Gate-source charge	Q_{gs} *	–	0.2	–	nC	V_{GS}= –4.5V
Gate-drain charge	Q_{gd} *	–	0.2	–	nC	R_L= 75Ω, R_G= 10Ω

*Pulsed

N-ch

●Electrical characteristic curve

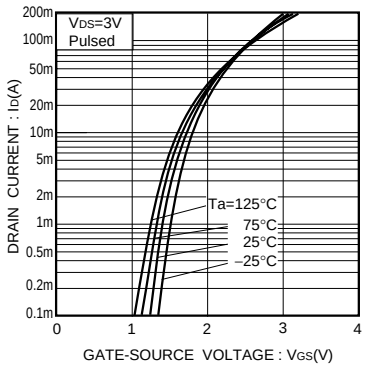


Fig.1 Typical Transfer Characteristics

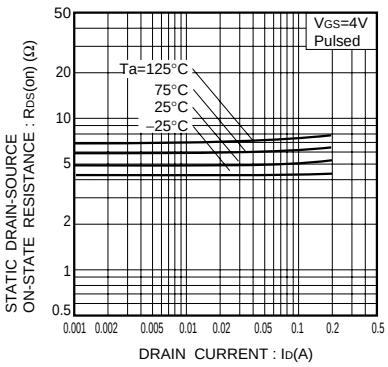


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current (I)

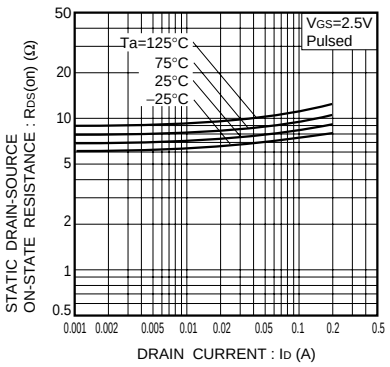


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current (II)

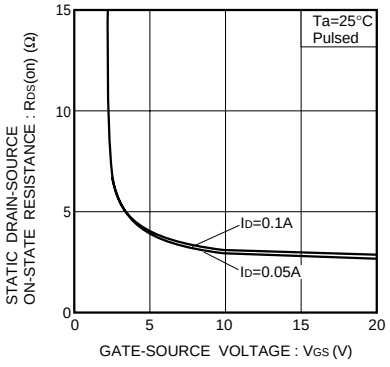


Fig.4 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

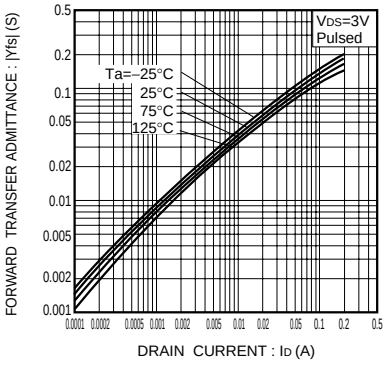


Fig.5 Forward Transfer Admittance vs. Drain Current

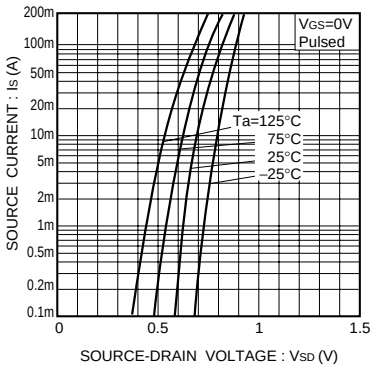


Fig.6 Reverse Drain Current vs. Source-Drain Voltage (I)

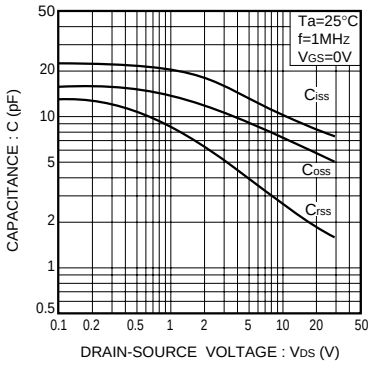


Fig.7 Typical Capacitance vs. Drain-Source Voltage

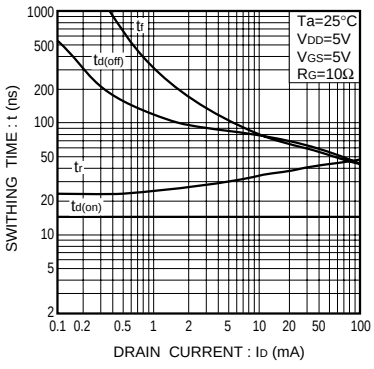


Fig.8 Switching Characteristics

P-ch

●Electrical characteristic curve

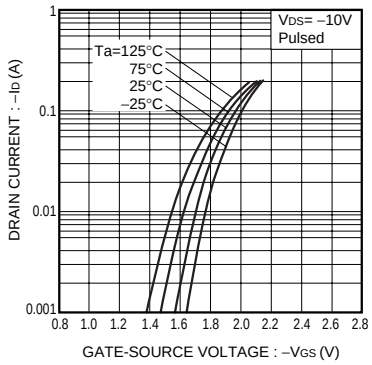


Fig.1 Typical Transfer Characteristics

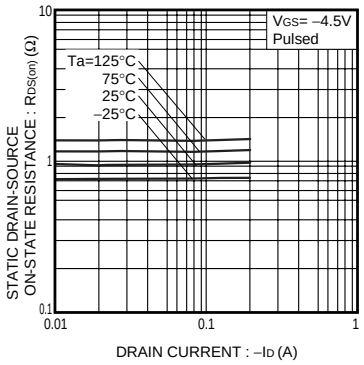


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current (Ⅰ)

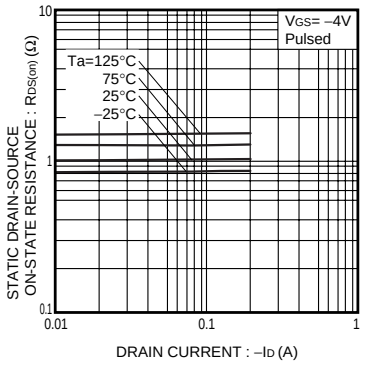


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current (Ⅱ)

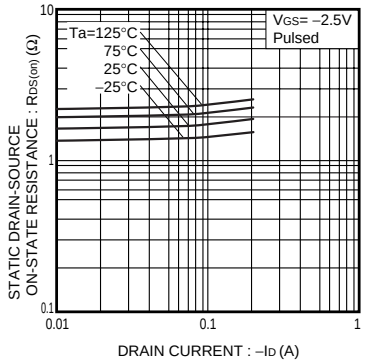


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (Ⅲ)

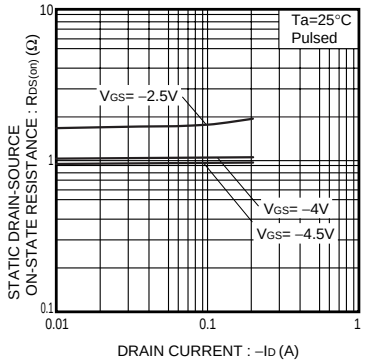


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (Ⅳ)

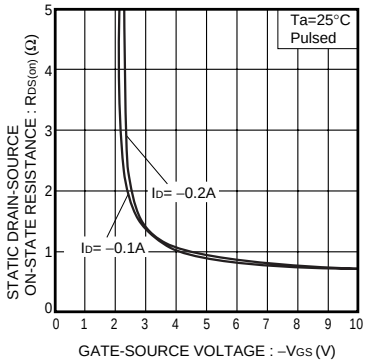


Fig.6 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

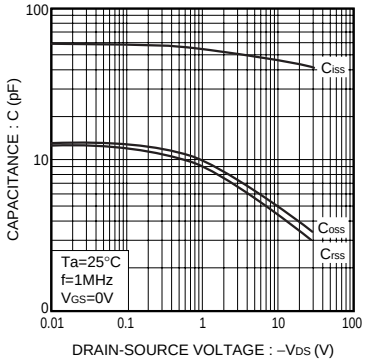


Fig.7 Typical Capacitance vs. Drain-Source Voltage

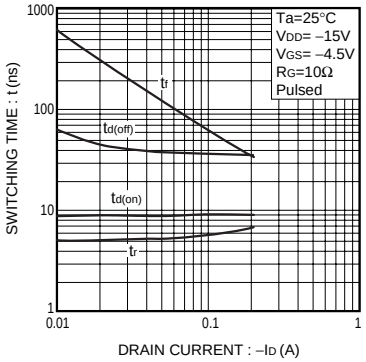


Fig.8 Switching Characteristics

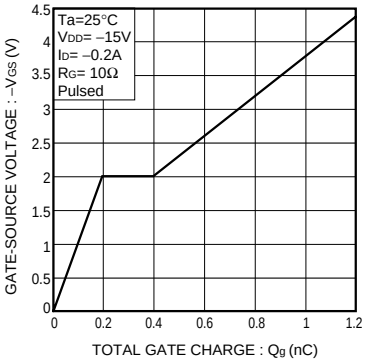


Fig.9 Dynamic Input Characteristics

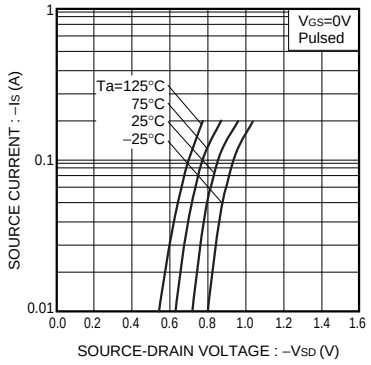


Fig.10 Source Current vs. Source-Drain Voltage

N-ch

●Measurement circuit

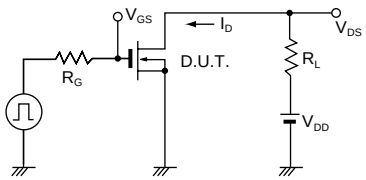


Fig.9 Switching Time Test Circuit

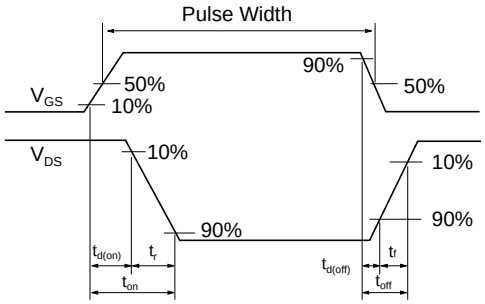


Fig.10 Switching Time Waveforms

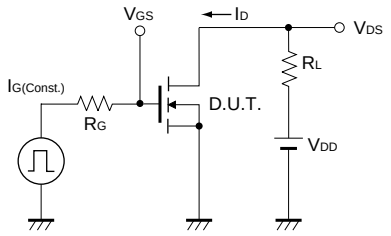


Fig.11 Gate Charge Measurement Circuit

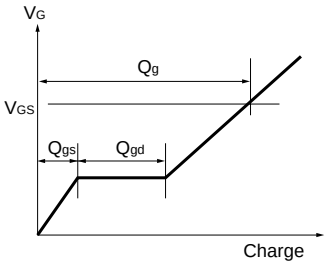


Fig.12 Gate Charge Waveform

P-ch

●Measurement circuit

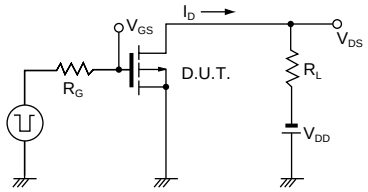


Fig.11 Switching Time Test Circuit

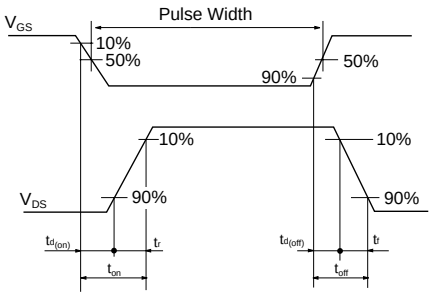


Fig.12 Switching Time Waveforms

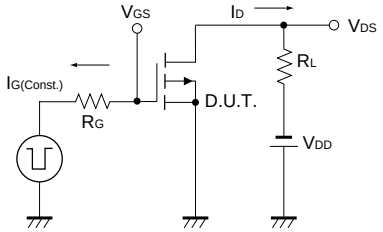


Fig.13 Gate Charge Measurement Circuit

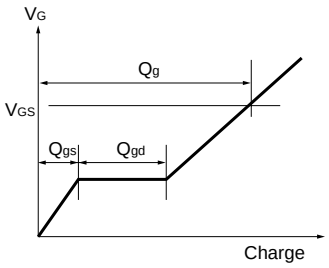


Fig.14 Gate Charge Waveform

Appendix

Notes

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