PRELIMINARY

CRYSTAL-TO-0.7V DIFFERENTIAL HCSL/ LVCMOS FREQUENCY SYNTHESIZER

ICS841S012I

GENERAL DESCRIPTION

The ICS841S012I is an optimized PCIe, sRIO and Gigabit Ethernet Frequency Synthesizer and a member of HiperClocks™family of high performance clock solutions from IDT. The ICS841S012I uses a 25MHz parallel resonant crystal to generate 33.33MHz - 200MHz clock signals, replacing solutions requiring multiple oscillator and fanout buffer solution. The device supports ±0.25% center-spread, and -0.5% down-spread clocking with two spread select pins (SSC[1:0]). The VCO operates at frequency of 2GHz. The device has three output banks: Bank A with two HCSL outputs, 100MHz – 250MHz; Bank B with seven 33.33MHz – 200MHz LVCMOS/ LVTTL outputs; and Bank C with one 33.33MHz – 200MHz LVCMOS/LVTTL output.

All Banks A, B and C have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The low jitter characteristic of the ICS841S012I makes it an ideal clock source for PCIe, sRIO and Gigabit Ethernet applications. Designed for networking and industrial applications, the ICS841S012I can also drive the high-speed clock inputs of communication processors, DSPs, switches and bridges.

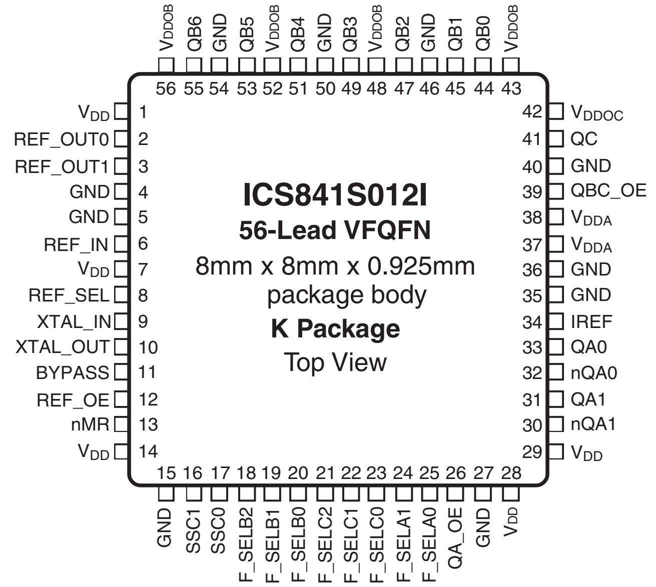
FEATURES

- Two 0.7V differential HCSL outputs (Bank A), configurable for PCIe (100MHz or 250MHz) and sRIO (100MHz or 125MHz) clock signals

  Eight LVCMOS/LVTTL outputs (Banks B/C), 15Ω typical output impedance

  Two REF_OUT LVCMOS/LVTTL clock outputs, 20Ω typical output impedance
- Selectable crystal oscillator interface, 25MHz, 18pF parallel resonant crystal or one LVCMOS/LVTTL single-ended reference clock input
- Supports the following output frequencies:
  HCSL Bank A: 100MHz, 125MHz, 200MHz and 250MHz
  LVCMOS/LVTTL Bank B/C: 33.33MHz, 50MHz, 66.67MHz, 100MHz, 125MHz, 133.33MHz, 166.67MHz and 200MHz
- VCO: 2GHz
- Spread spectrum clock: ±0.25% center-spread and -0.5% down-spread
- PLL bypass and output enable
- RMS period jitter: 15ps (typical), QB outputs
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

PIN ASSIGNMENT



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

BLOCK DIAGRAM

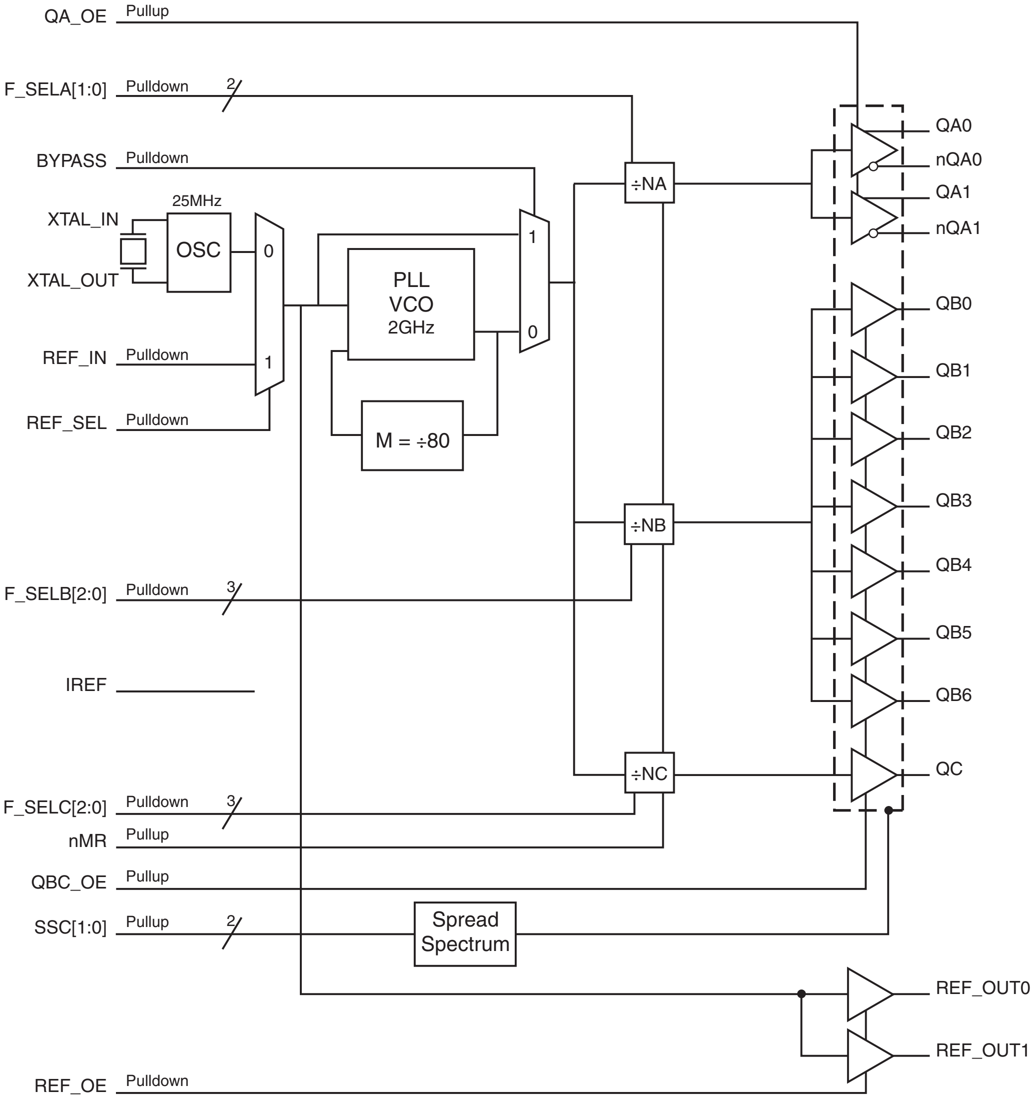


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 7, 14, 28, 29	V_{DD}	Power		Core supply pins.
2, 3	REF_OUT0, REF_OUT1	Output		Single-ended LVCMOS/LVTTL reference clock outputs. 20Ω typical output impedance.
4, 5, 15, 27, 35, 36, 40, 46, 50, 54	GND	Power		Power supply ground.
6	REF_IN	Input	Pulldown	Single-ended LVCMOS/LVTTL reference clock input.
8	REF_SEL	Input	Pulldown	Reference select pin. When HIGH selects REF_IN. When LOW, selects crystal. LVCMOS/LVTTL interface levels. See Table 3E.
9, 10	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.
11	BYPASS	Input	Pulldown	When HIGH bypasses PLL. When LOW, selects N divider. LVCMOS/LVTTL interface levels.
12	REF_OE	Input	Pulldown	Active HIGH REF_OUT enables/disables pin. LVCMOS/LVTTL interface levels. See Table 3H.
13	nMR	Input	Pullup	Active LOW Master Reset. When logic LOW, the internal dividers are reset and the outputs are in high impedance (HI-Z). When logic HIGH, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
16, 17	SSC1, SSC0	Input	Pullup	SSC control pin. LVCMOS/LVTTL interface levels. See Table 3D.
18, 19, 20	F_SELB2, F_SELB1, F_SELB0	Input	Pulldown	Frequency select pins for QBx outputs. See Table 3B. LVCMOS/LVTTL interface levels.
21, 22, 23	F_SELC2, F_SELC1, F_SELC0	Input	Pulldown	Frequency select pins for QC output. See Table 3C. LVCMOS/LVTTL interface levels.
24, 25	F_SELA1, F_SELA0	Input	Pulldown	Frequency select pins for QAx/nQAx outputs. See Table 3A. LVCMOS/LVTTL interface levels.
26	QA_OE	Input	Pullup	Output enable pin for Bank A outputs. LVCMOS/LVTTL interface levels. See Table 3F.
30, 31 32, 33	nQA1, QA1 nQA0, QA	Output		Differential Bank A clock outputs. HCSL interface levels.
34	IREF	Output		External fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode QAx/nQAx clock outputs.
37, 38	V_{DDA}	Power		Analog supply pin.
39	QBC_OE	Input	Pullup	Output enable pin for Bank B and Bank C outputs. LVCMOS/LVTTL Interface levels. See Table 3G.
41	QC	Output		Single-ended Bank C clock output. LVCMOS/LVTTL interface levels. 15Ω typical output impedance.
42	V_{DDOC}	Power		Output supply pin for QC LVCMOS output.
43, 48, 52, 56	V_{DDOB}	Power		Output supply pins for QBx LVCMOS outputs.
44, 45, 47, 49, 51, 53, 55	QB0, QB1, QB2, QB3, QB4, QB5, QB6	Output		Single-ended Bank B clock outputs. LVCMOS/LVTTL interface levels. 15Ω typical output impedance.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
C_{PD}	Power Dissipation Capacitance	QB[0:6], QC	V_{DD}, V_{DDOB}, V_{DDOC} = 3.465V		9		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	QB[0:6], QC			15		Ω
		REF_OUT[1:0]			20		Ω

TABLE 3A. F_SELA FREQUENCY SELECT FUNCTION TABLE

Inputs				Output Frequency (25MHz Ref.)
F_SELA1	F_SELA0	M Divider Value	NA Divider Value	QA[0:1]/nQA[0:1] (MHz)
L	L	80	20	100
L	H	80	16	125
H	L	80	10	200
H	H	80	8	250

TABLE 3B. F_SELB FREQUENCY SELECT FUNCTION TABLE

Inputs					Output Frequency (25MHz Ref.)
F_SELB2	F_SELB1	F_SELB0	M Divider Value	NB Divider Value	QB[0:6] (MHz)
L	L	L	80	60	33.33
L	L	H	80	40	50
L	H	L	80	30	66.67
L	H	H	80	20	100
H	L	L	80	16	125
H	L	H	80	15	133.33
H	H	L	80	12	166.67
H	H	H	80	10	200

TABLE 3C. F_SELC FREQUENCY SELECT FUNCTION TABLE

Inputs					Output Frequency (25MHz Ref.)
F_SELC2	F_SELC1	F_SELC0	M Divider Value	NC Divider Value	QC (MHz)
L	L	L	80	60	33.33
L	L	H	80	40	50
L	H	L	80	30	66.67
L	H	H	80	20	100
H	L	L	80	16	125
H	L	H	80	15	133.33
H	H	L	80	12	166.67
H	H	H	80	10	200

TABLE 3D. SSC FUNCTION TABLE

Input		
SSC1	SSC0	Mode
0	0	0 to -0.5% Down-spread
0	1	±0.25% Center-spread
1	0	±0.25% Center-spread
1	1	SSC Off (default)

TABLE 3E. REF_SEL FUNCTION TABLE

Input	
REF_SEL	Input Reference
0	XTAL
1	REF_IN

TABLE 3F. QA_OE FUNCTION TABLE

Input	
QA_OE	Function
0	QA[0:1]/nQA[0:1] disabled (Hi-Z)
1	QA[0:1]/nQA[0:1] enabled

TABLE 3G. QBC_OE FUNCTION TABLE

Input	
QBC_OE	Function
0	QB[0:6] and QC disabled (Hi-Z)
1	QB[0:6] and QC enabled

TABLE 3H. REF_OE FUNCTION TABLE

Input	
REF_OE	Function
0	REF_OUT[0:1] disabled (Hi-Z)
1	REF_OUT[0:1] enabled

TABLE 3I. nMR FUNCTION TABLE

Input	
nMR	Function
0	Device reset, output divider disabled (Hi-Z)
1	Output enabled

NOTE: This device requires a reset signal after power-up to function properly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	31.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDOB} = V_{DDOC} = 3.3V\pm5\%$, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.20	3.3	V_{DD}	V
V_{DDOB}, V_{DDOC}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			250		mA
I_{DDA}	Analog Supply Current			20		mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDOB} = V_{DDOC} = 3.3V\pm5\%$, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	QA_OE, QBC_OE, nMR, SSC0, SSC1,	$V_{DD} = V_{IN} = 3.465V$			5	µA
		F_SELA[0:1], F_SELB[0:2]. F_SELC[0:2], REF_OE, BYPASS, REF_IN, REF_SEL	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	QA_OE, QBC_OE, nMR, SSC0, SSC1,	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
		F_SELA[0:1], F_SELB[0:2]. F_SELC[0:2], REF_OE, BYPASS, REF_IN, REF_SEL	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDOB}, V_{DDOC} = 3.3V ± 5%	2.6			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDOB}, V_{DDOC} = 3.3V ± 5%			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDOB,\,C}/2$. See Parameter Measurement Information, Output Load Test Circuit diagram.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				100	µW

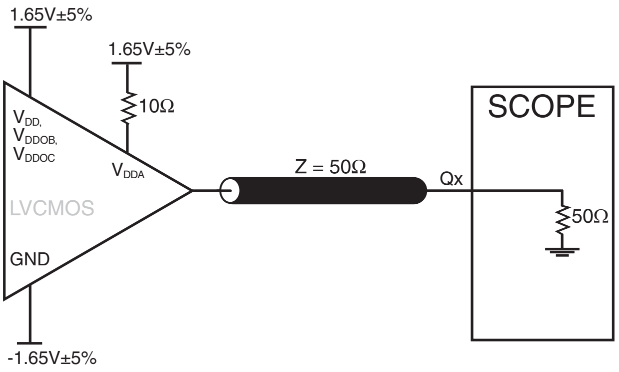
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDOB} = V_{DDOC} = 3.3V \pm 5\%$, TA = -40°C TO 85°C

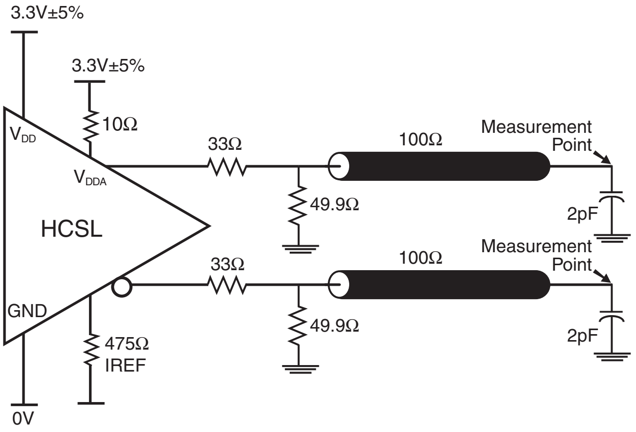
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QB[0:6]		33.33		200	MHz
		QA[0:1]/nQA[0:1]		100		250	MHz
		QC		33.33		200	MHz
*t*sk(o)	Output Skew; NOTE 1, 2	QB[0:6]			35		ps
		QA[0:1]/nQA[0:1]			10		ps
*t*sk(b)	Bank Skew; NOTE 2, 3		across Banks B and C		50		ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 2	QA[0:1]/nQA[0:1]			45		ps
		QB[0:6]			55		ps
		QC			50		ps
*t*jit(per)	RMS Period Jitter	QA[0:1]/nQA[0:1]			7		ps
		QB[0:6], QC			15		ps
F_M	SSC Modulation Frequency	Banks A, B, C		29		33.33	kHz
V_{HIGH}	Voltage High			660		850	mV
V_{LOW}	Voltage Low			-150			mV
V_{CROSS}	Absolute Crossing Voltage			250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges					140	mV
t_R / t_F	Output Rise/Fall Time	Bank A	measured between 0.175V to 0.525V	175		700	ps
		Banks B, C	20% - 80%		350		ps
odc	Output Duty Cycle	Bank A		45		55	%
		Banks B, C			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDOB,\,C}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

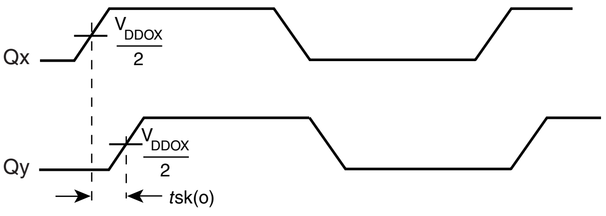
PARAMETER MEASUREMENT INFORMATION



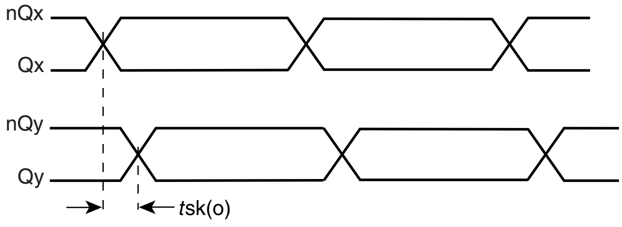
3.3V CORE/3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



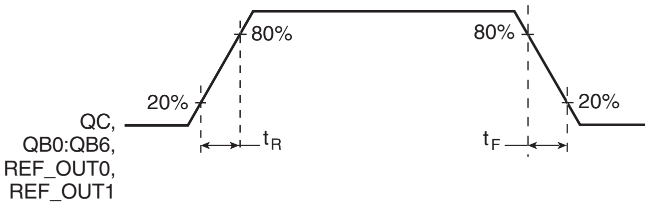
3.3V CORE/3.3V HCSL OUTPUT LOAD AC TEST CIRCUIT



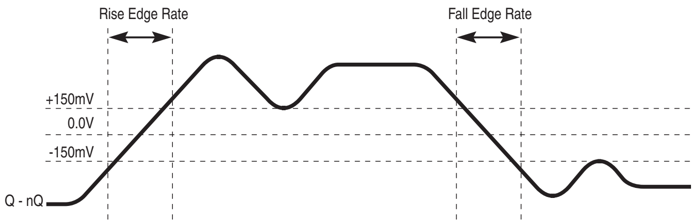
LVCMOS OUTPUT SKEW



HCSL OUTPUT SKEW

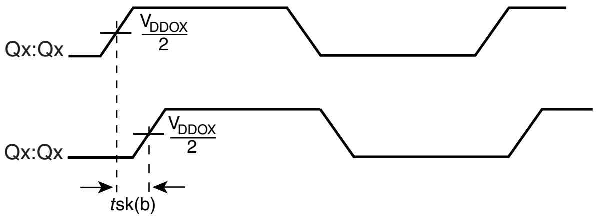


LVCMOS OUTPUT RISE/FALL TIME



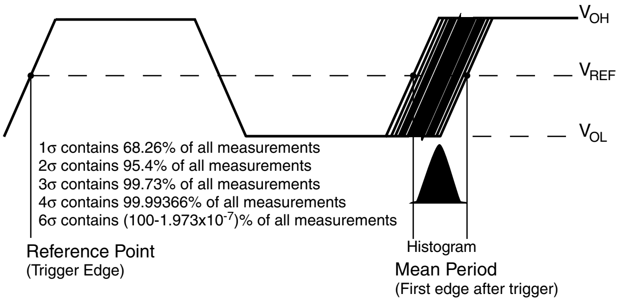
DIFFERENTIAL MEASUREMENT POINTS FOR RISE/FALL TIME

PARAMETER MEASUREMENT INFORMATION, CONTINUED

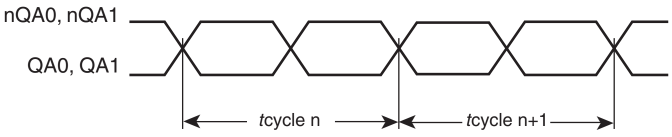


(where X = Bank A or Bank B)

BANK SKEW

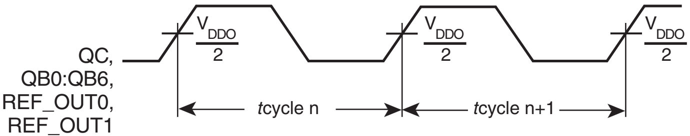


RMS PERIOD JITTER



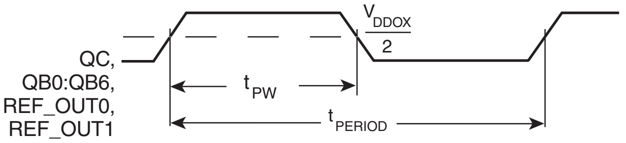
tjit(cc) = tcycle n – tcycle n+1
1000 Cycles

DIFFERENTIAL CYCLE-TO-CYCLE JITTER



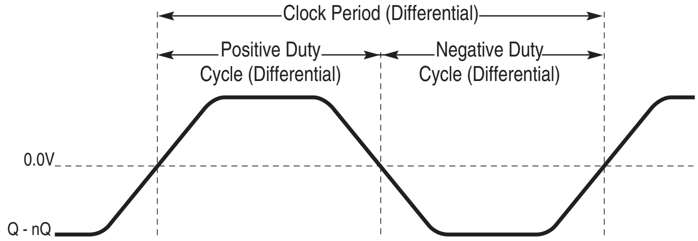
tjit(cc) = tcycle n – tcycle n+1
1000 Cycles

LVCMOS CYCLE-TO-CYCLE JITTER



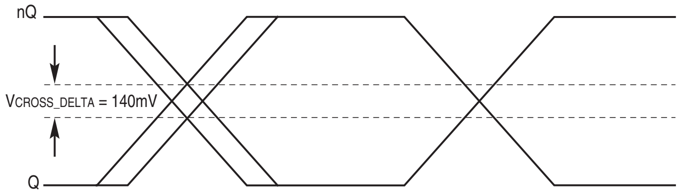
$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



DIFFERENTIAL MEASUREMENT POINTS FOR DUTY CYCLE/PERIOD

PARAMETER MEASUREMENT INFORMATION, CONTINUED



SE MEASUREMENT POINTS FOR DELTA CROSS POINT

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS841S012I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, V_{DDOB}, and V_{DDOC} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

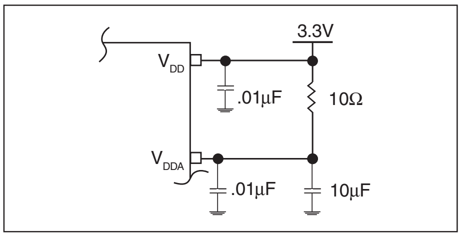


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_IN INPUT

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_IN to ground.

LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUTS

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

DIFFERENTIAL OUTPUT

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

CRYSTAL INPUT INTERFACE

The ICS841S012I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

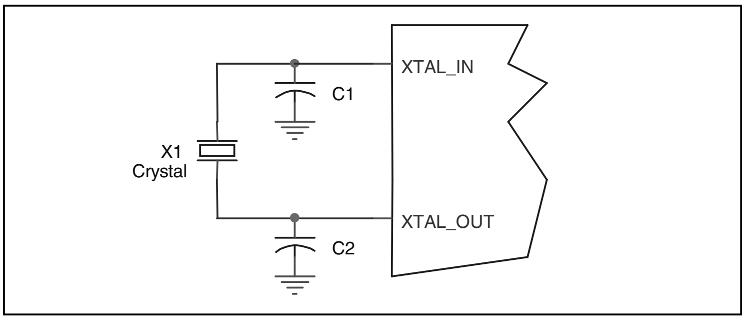


FIGURE 2. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

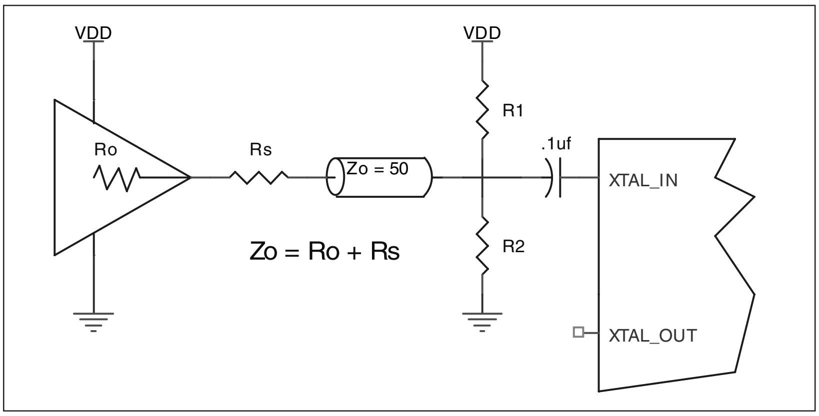


FIGURE 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

VFQFN EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

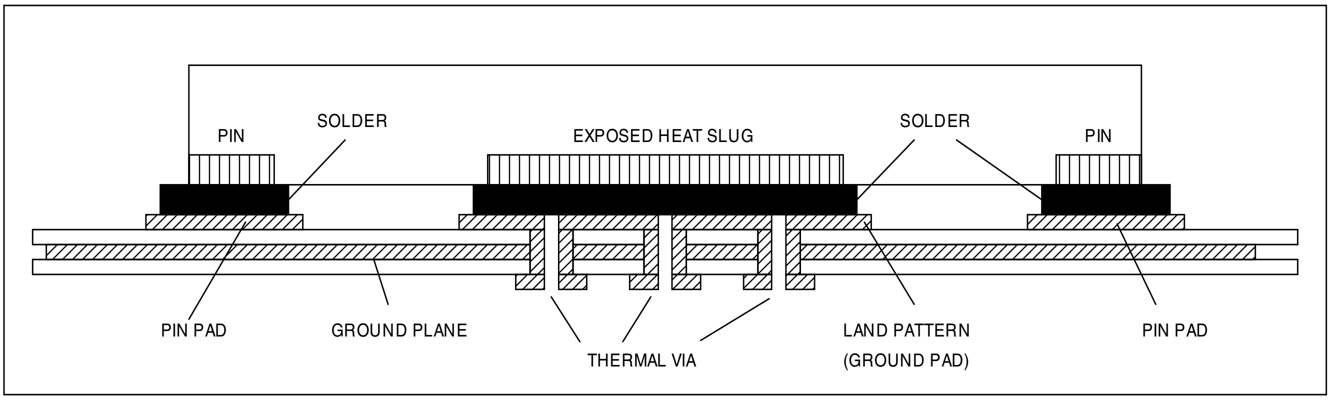


FIGURE 4. P.C.ASSEMBLY FOR EXPOSED PAD THERMAL RELEASE PATH –SIDE VIEW (DRAWING NOT TO SCALE)

RECOMMENDED TERMINATION

Figure 5A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ù impedance.

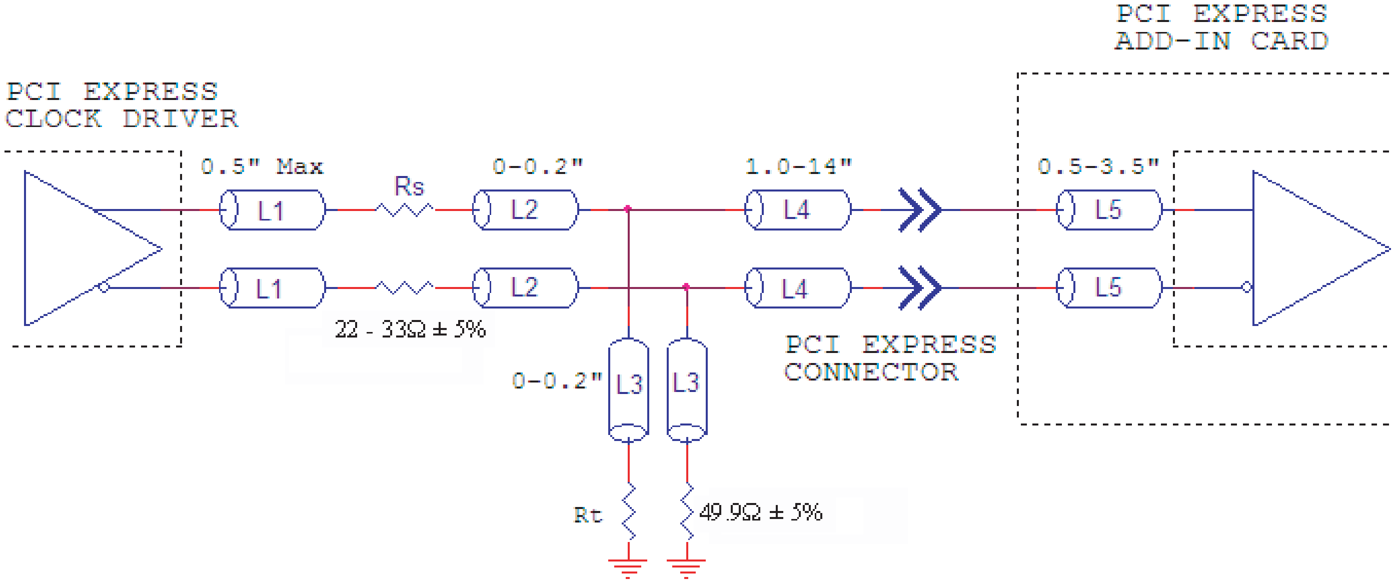


FIGURE 5A. RECOMMENDED TERMINATION

Figure 5B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ù impedance.

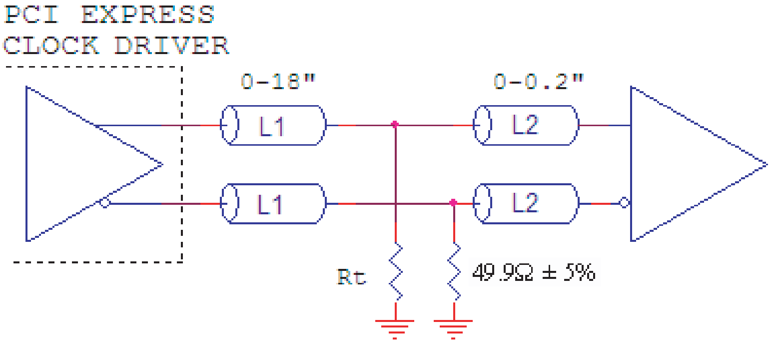


FIGURE 5B. RECOMMENDED TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS841S012I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS841S012I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

Core and HCSL Output Power Dissipation

- Power (core) = $V_{DD\_MAX} * (I_{DD} + I_{DDA}) = 3.465V * (250mA + 20mA) =$ **935.6mW**
  Power (HCSL) = **44.5mW/Load Output Pair**
  If all outputs are loaded, the total power is 2 * 44.5mW = **89mW**

LVCMOS Output Power Dissipation, $R_{OUT} = 15\Omega$

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DDO}/2$
  Output Current $I_{OUT} = V_{DDO\_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465V / [2 * (50\Omega + 15\Omega)] =$ **26.7mA**

- Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 15\Omega * (26.7mA)^2 =$ **10.7mW per output**

- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT} = 15Ω) = 10.7mW * 7 = **74.9mW**

- Dynamic Power Dissipation at 200MHz
  Power (200MHz) = $C_{PD} * \text{Frequency} * (V_{DDO})^2 = 9pF * 200MHz * (3.465V)^2 =$ **21.6mW per output**
  Total Power (200MHz) = **21.6mW * 7 = 151.2mW**

LVCMOS Output Power Dissipation, $R_{OUT} = 20\Omega$

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DDO}/2$
  Output Current $I_{OUT} = V_{DDO\_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465V / [2 * (50\Omega + 20\Omega)] =$ **24.75mA**

- Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 20\Omega * (24.75mA)^2 =$ **12.3mW per output**

- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT} = 20Ω) = 12.3mW * 2 = **24.6mW**

- Dynamic Power Dissipation at 25MHz
  Power (25MHz) = $C_{PD} * \text{Frequency} * (V_{DDO})^2 = 9pF * 25MHz * (3.465V)^2 =$ **2.7mW per output**
  Total Power (25MHz) = **2.7mW * 2 = 5.4mW**

Total Power Dissipation

- **Total Power**
  = Power (core) + Power (HCSL) + Total Power (R_{OUT}= 15Ω) + Total Power (200MHz) + Total Power (R_{OUT}= 20Ω) + Total Power (25MHz)
  = 935.6mW + 89mW + 74.9mW + 151.2mW + 24.6mW + 5.4mW
  = 1280.7mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming 1 meter per second air flow and a multi-layer board, the appropriate value is 27.5°C/W per Table 7.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.281W * 27.5°C/W = 120.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 56 LEAD VFQFN, FORCED CONVECTION

θ_{JA} by Velocity (Meters per second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	31.4°C/W	27.5°C/W	24.6°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 6.*

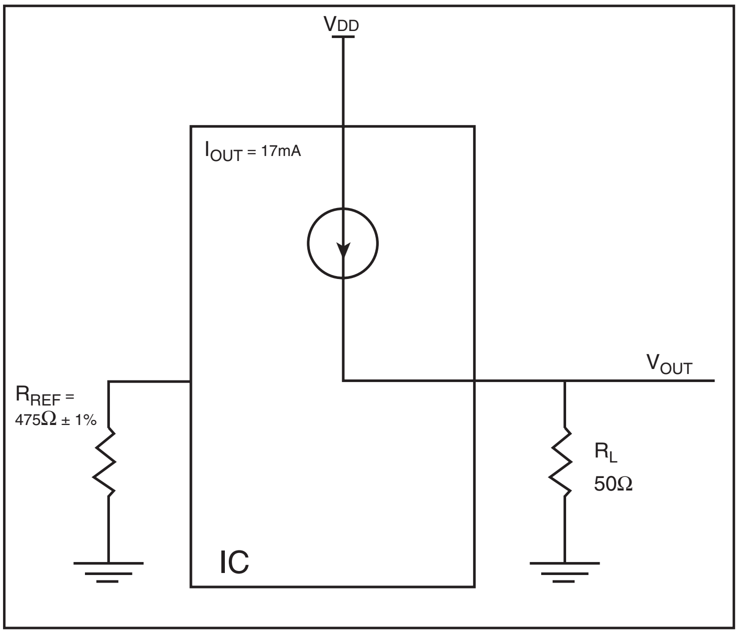


FIGURE 6. HCSL DRIVER CIRCUIT AND TERMINATION

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs at maximum V_{DD}.

Power $= (V_{DD\_MAX} – V_{OUT}) * I_{OUT}$, since $V_{OUT} = I_{OUT} * R_L$

$= (V_{DD\_MAX} – I_{OUT} * R_L) * I_{OUT}$

$= (3.465V – 17mA * 50\Omega) * 17mA$

Total Power Dissipation per output pair = **44.5mW**

RELIABILITY INFORMATION

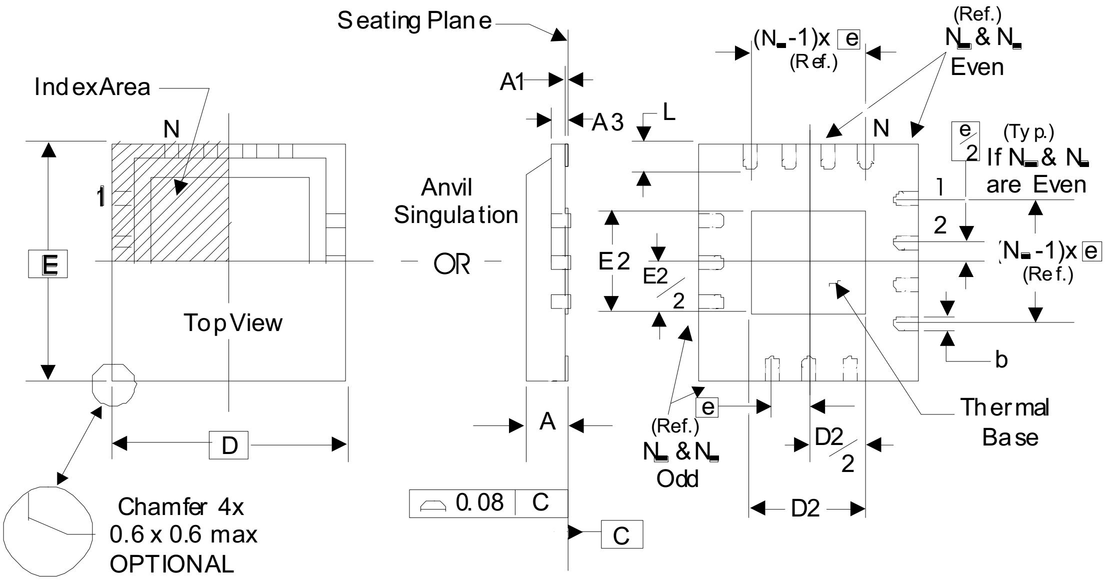
TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 56 LEAD VFQFN

θ_{JA} by Velocity (Meters per second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	31.4°C/W	27.5°C/W	24.6°C/W

TRANSISTOR COUNT

The transistor count for ICS841S012I is: 11,537

PACKAGE OUTLINE - K SUFFIX FOR 56 LEAD VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

TABLE 9. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	56	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	14	
N_E	14	
D	8.0	
D2	4.35	4.65
E	8.0	
E2	5.05	5.35
L	0.3	0.55

Reference Document: JEDEC Publication 95, MO-220

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
841S012BKI	TBD	56 lead VFQFN	tray	-40°C to 85°C
841S012BKIT	TBD	56 lead VFQFN	1000 tape & reel	-40°C to 85°C
841S012BKILF	ICS841S012BIL	56 lead "Lead-Free" VFQFN	tray	-40°C to 85°C
841S012BKILFT	ICS841S012BIL	56 lead "Lead-Free" VFQFN	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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