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PRELIMINARY

FEMTOCLOCKS™ CRYSTAL-TO-3.3V LVPECL FREQUENCY SYNTHESIZER

ICS843206I

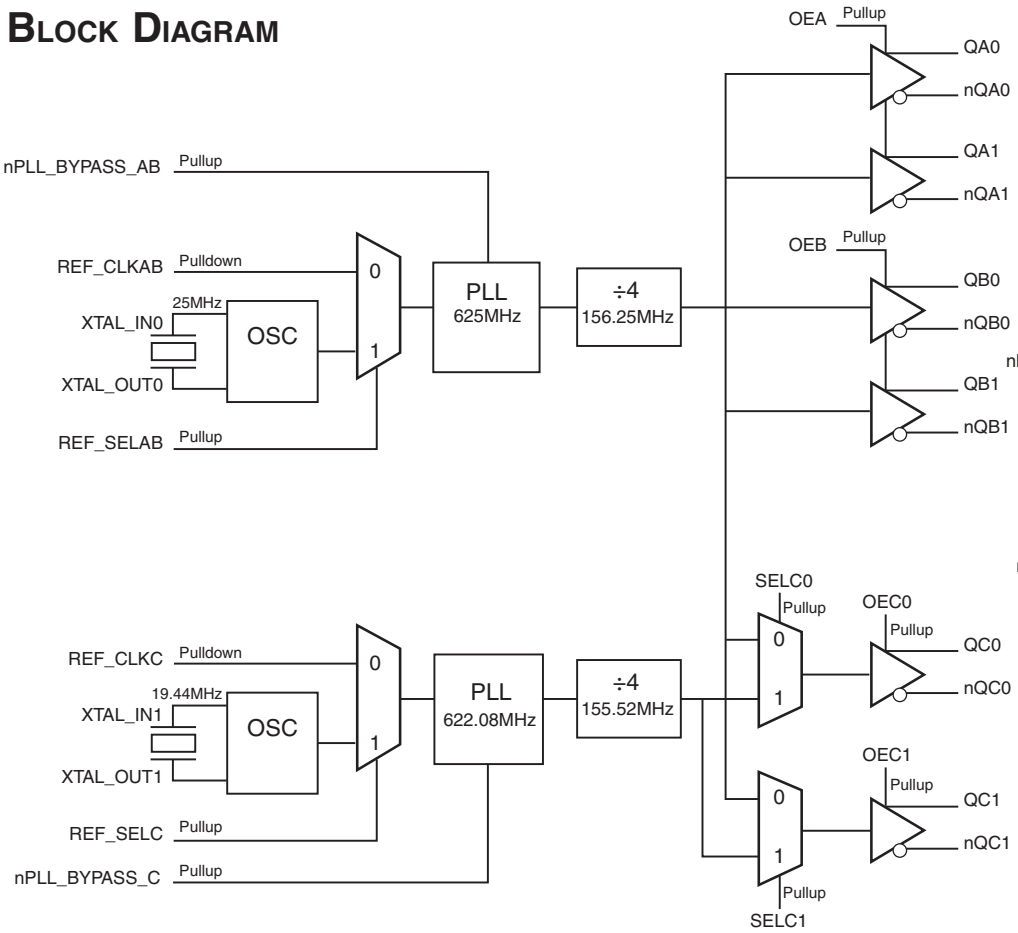
General Description

The ICS843206I is a 6 output LVPECL Synthesizer optimized to generate Gigabit Ethernet and SONET reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. Using a 19.44MHz and 25MHz, 18pF parallel resonant crystal, 155.52MHz and 156.25MHz frequencies can be generated. The ICS843206I uses IDT's FemtoClock™ low phase noise VCO technology and can achieve 1ps or lower typical RMS phase jitter. The ICS843206I is packaged in a 48-pin TSSOP package.

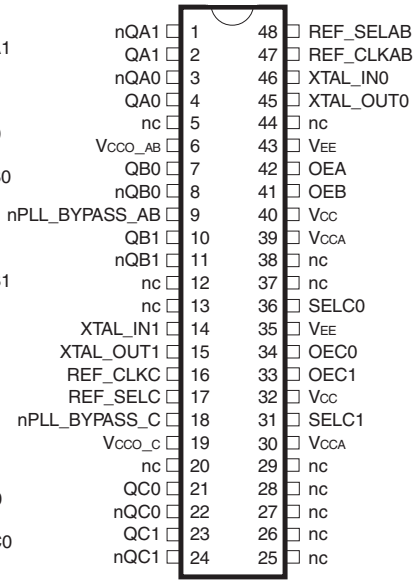
Features

- Six 3.3V differential LVPECL output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following output frequencies: 155.52MHz and 156.25MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 155.52MHz, using a 19.44MHz crystal (12kHz – 1.3MHz): 1.08ps (typical)
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.5ps (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS843206I
48 Lead TSSOP
6.1mm x 12.5mm x 0.93mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	nQA1, QA1	Output		Differential output pair. LVPECL interface levels.
3, 4	nQA0, QA0	Output		Differential output pair. LVPECL interface levels.
5, 12, 13, 20, 25, 26, 27, 28, 29, 37, 38, 44	nc	Unused		No connect.
6	V_{CCO_AB}	Power		Output supply pin for Bank A and Bank B outputs.
7, 8	nQB0, QB0	Output		Differential output pair. LVPECL interface levels.
9	nPLL_BYPASS_AB	Input	Pullup	When LOW, PLL is bypassed. When HIGH, PLL output is active. LVCMOS/LVTTL interface levels.
10, 11	nQB1, QB1	Output		Differential output pair. LVPECL interface levels.
14, 15	XTAL_IN1, XTAL_OUT1	Input		Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.
16	REF_CLKC	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
17	REF_SELC	Input	Pullup	Select pin. When HIGH, selects XTAL1 inputs. When LOW, selects REF_CLKC input. LVCMOS/LVTTL interface levels.
18	nPLL_BYPASS_C	Input	Pullup	When LOW, PLL is bypassed. When HIGH, PLL output is active. LVCMOS/LVTTL interface levels.
19	V_{CCO_C}	Power		Output supply pin for Bank C outputs.
21, 22	QC0, nQC0	Output		Differential output pair. LVPECL interface levels.
23, 24	QC1, nQC1	Output		Differential output pair. LVPECL interface levels.
30, 39	V_{CCA}	Power		Analog supply pins.
31	SELC1	Input	Pullup	Select pin. When HIGH, selects QC1/nQC1 at 155.52MHz. When LOW, selects QC1/nQC1 at 156.25MHz. LVCMOS/LVTTL interface levels.
32, 40	V_{CC}	Power		Core supply pins.
33	OEC1	Input	Pullup	Output enable pin. QC1/nQC1 outputs are enable. LVCMOS/LVTTL interface levels.
34	OEC0	Input	Pullup	Output enable pin. QC0/nQC0 outputs are enabled. LVCMOS/LVTTL interface levels.
35, 43	V_{EE}	Power		Negative supply pins.
36	SELC0	Input	Pullup	Select pin. When HIGH, selects QC0/nQC0 at 155.52MHz. When LOW, selects QC0/nQC0 at 156.25MHz. LVCMOS/LVTTL interface levels.
41	OEB	Input	Pullup	Output enable pin. QB0/nQB0, QB1/nQB1outputs are enabled. LVCMOS/LVTTL interface levels.
42	OEA	Input	Pullup	Output enable pin. QA0/nQA0, QA1/nQA1 outputs are enabled. LVCMOS/LVTTL interface levels.
45, 46	XTAL_OUT0, XTAL_IN0	Input		Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.
47	REF_CLKAB	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
48	REF_SELAB	Input	Pullup	Select pin. When HIGH, selects XTAL0 inputs. When LOW, selects REF_CLKAB input. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	59.6°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, $V_{CC} = V_{CCO\_AB} = V_{CCO\_C}$ = 3.3V±10%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.97	3.3	3.63	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.18	3.3	V_{CC}	V
V_{CCO_AB}, V_{CCO_C}	Output Supply Voltage		2.97	3.3	3.63	V
I_{EE}	Power Supply Current			120		mA
I_{CCA}	Analog Supply Current			18		mA

Table 3B. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCO\_AB} = V_{CCO\_BC}$ = 3.3V±10%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_CLKAB, REF_CLKC	$V_{CC} = V_{IN}$ = 3.63V			150	µA
		SELC0, SELC1, nPLL_BYPASS_AB, nPLL_BYPASS_C, OEA, OEB, OEC0, OEC1, REF_SELAB, REF_SELC	$V_{CC} = V_{IN}$ = 3.63V			5	µA
I_{IL}	Input Low Current	REF_CLKAB, REF_CLKC	V_{CC} = 3.63V, V_{IN} = 0V	-5			µA
		SELC0, SELC1, nPLL_BYPASS_AB, nPLL_BYPASS_C, OEA, OEB, OEC0, OEC1, REF_SELAB, REF_SELC	V_{CC} = 3.63V, V_{IN} = 0V	-150			µA

TABLE 3C. LVPECL DC CHARACTERISTICS, V_{CC} = V_{CCO_AB} = V_{CCO_C} = 3.3V±10%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			19.44		MHz
			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

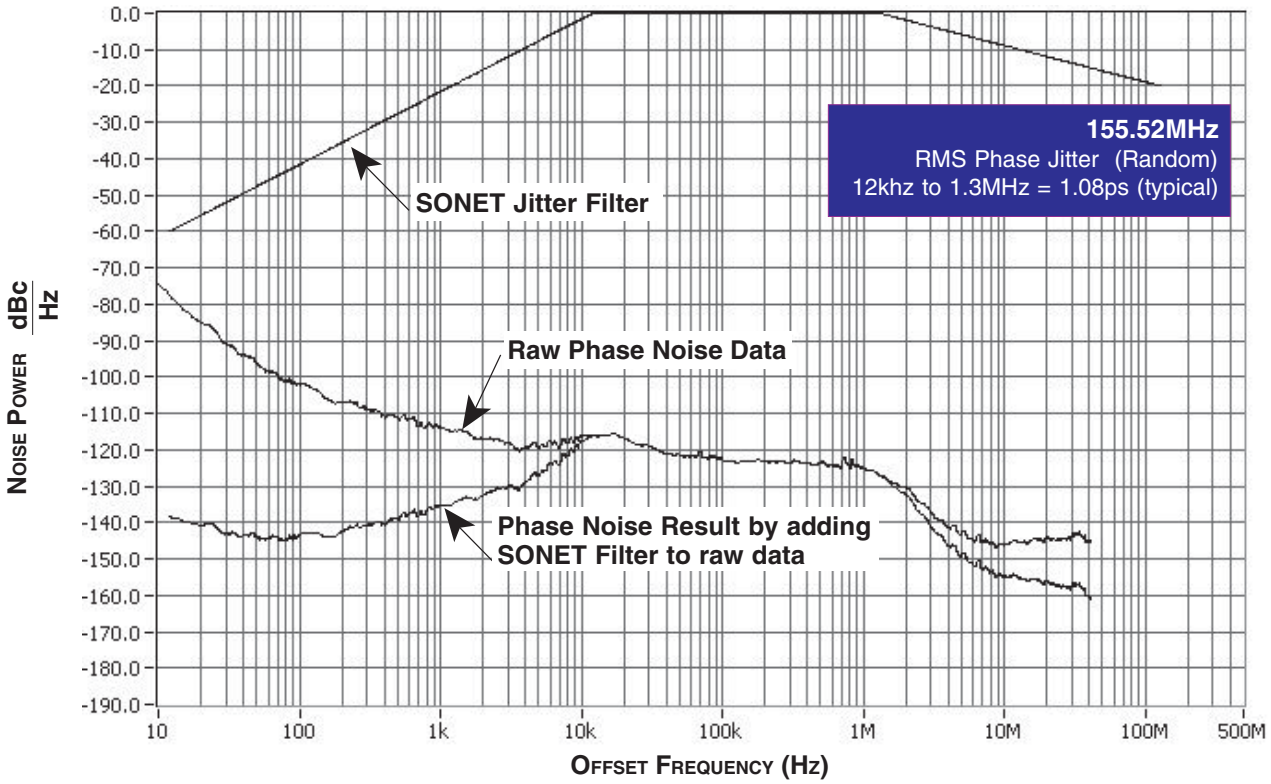
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5. AC CHARACTERISTICS, V_{CC} = V_{CCO_AB} = V_{CCO_C} = 3.3V±10%, T_A = -40°C TO 85°C

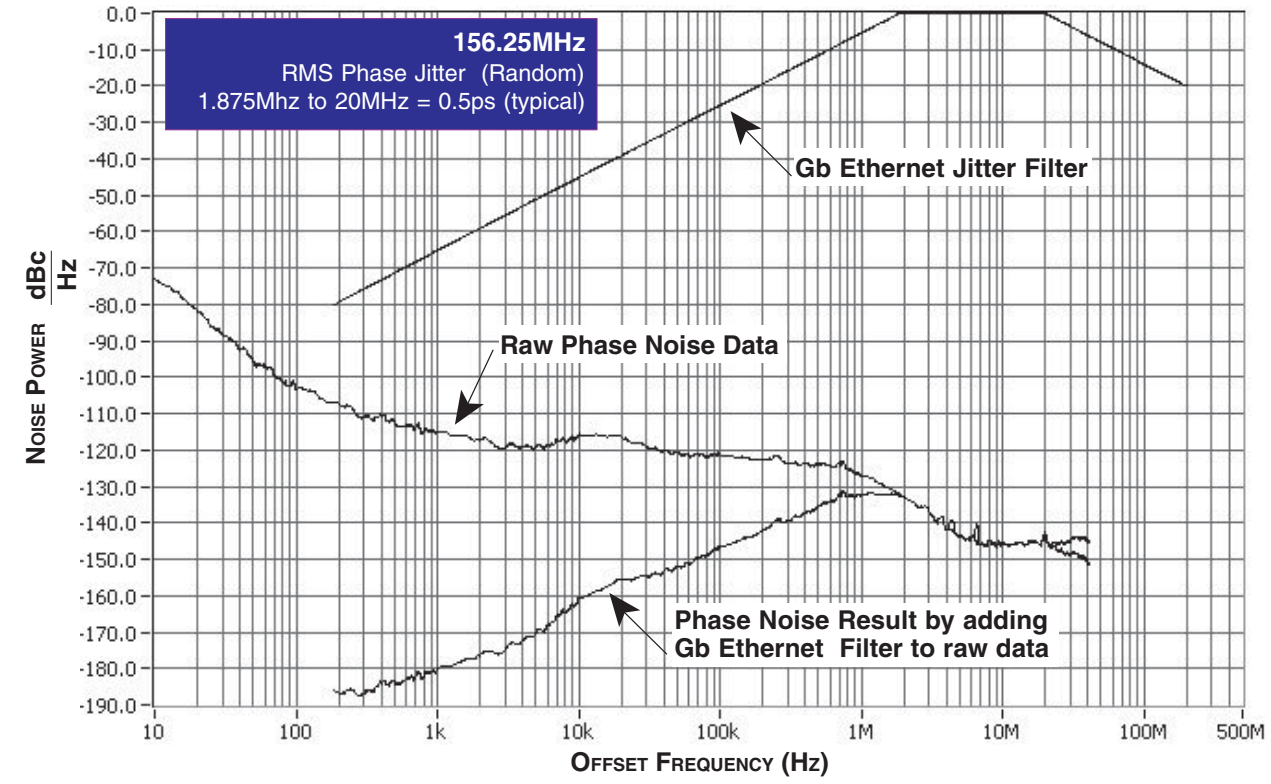
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QA[0:1]/nQA[0:1]			156.25		MHz
		QB[0:1]/nQB[0:1]			156.25		MHz
		QC0/nQC0	SELC0 = 0		156.25		MHz
			SELC0 = 1		155.52		MHz
		QC1/nQC1	SELC1 = 0		156.25		MHz
			SELC1 = 1		155.52		MHz
*t*sk(b)	Bank Skew; NOTE 1, 2				10		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	QA[0:1]/nQA[0:1]	156.25MHz, (1.875MHz - 20MHz)		0.5		ps
		QB[0:1]/nQB[0:1]	156.25MHz, (1.875MHz - 20MHz)		0.5		ps
		QC[0:1]/nQC[0:1]	155.52MHz, (12kHz - 1.3MHz)		1.08		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		450		ps
odc	Output Duty Cycle				50		%

NOTE 1: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions. Measured at the differential outputs.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: See Phase Noise plot.

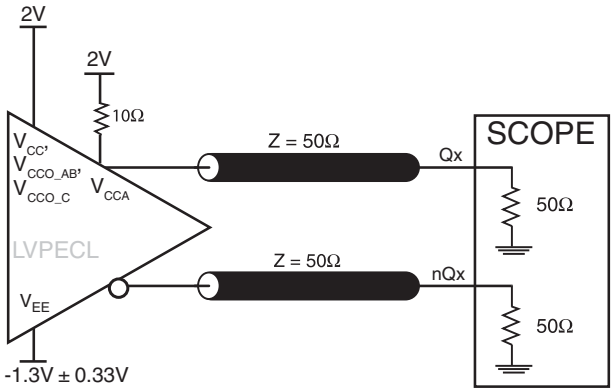
TYPICAL PHASE NOISE AT 155.52MHZ



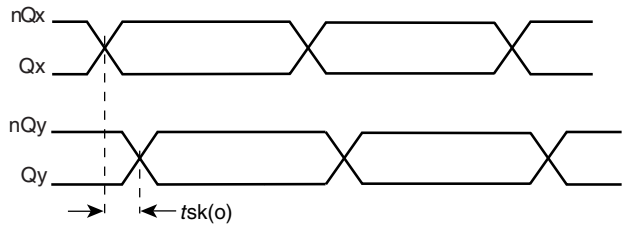
TYPICAL PHASE NOISE AT 156.25MHZ



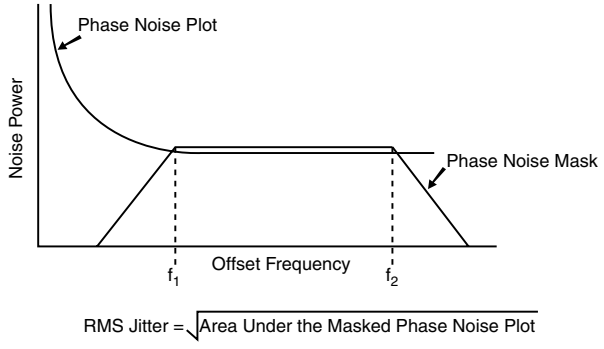
Parameter Measurement Information



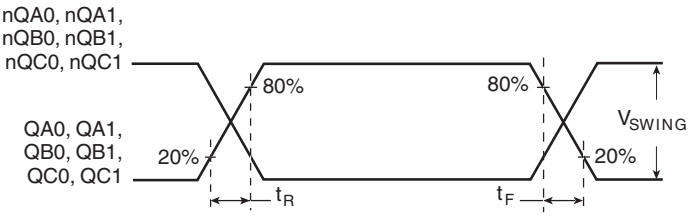
3.3V Core/3.3V Output Load AC Test Circuit



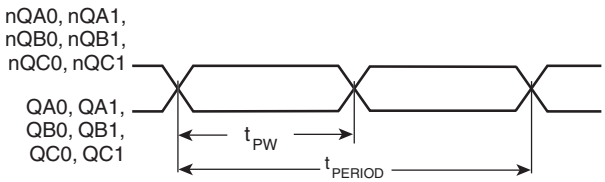
Output Skew



RMS Phase Jitter



Output Rise/Fall Time



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843206I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO_x} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

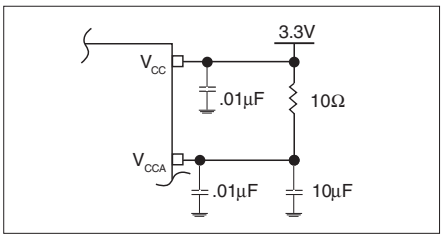


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Inputs

For applications not requiring the use of a reference clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLKx input to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The ICS843206I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

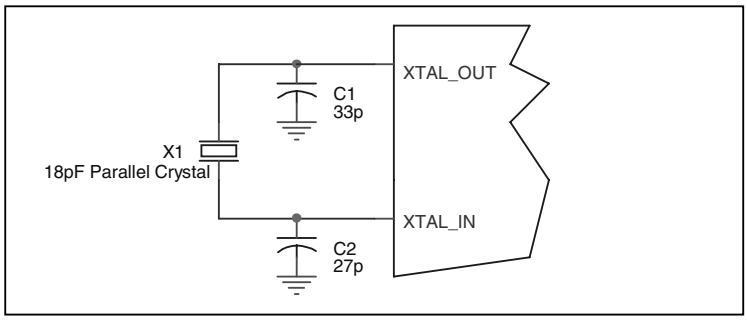


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

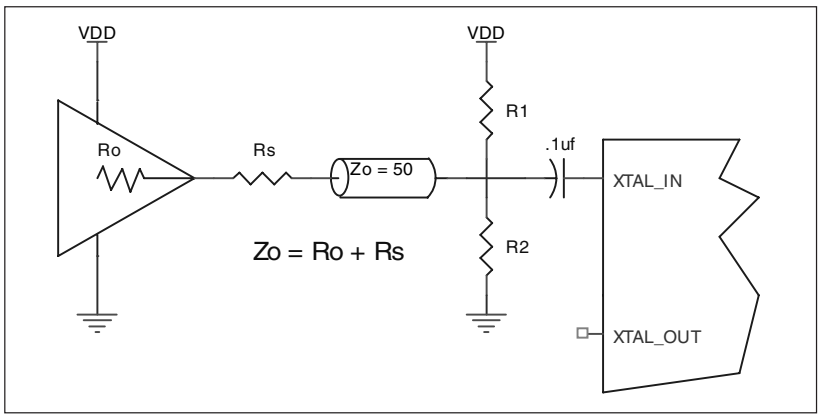


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

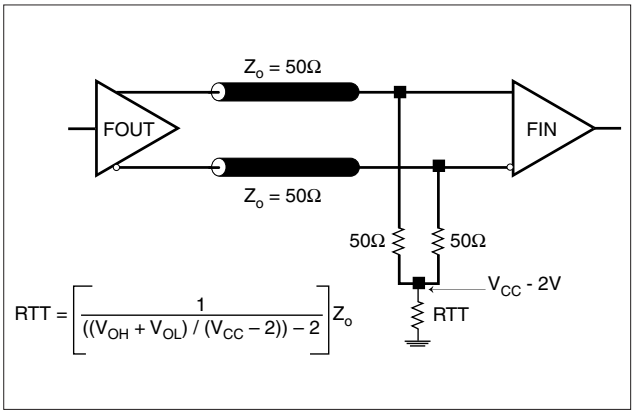


FIGURE 4A. LVPECL OUTPUT TERMINATION

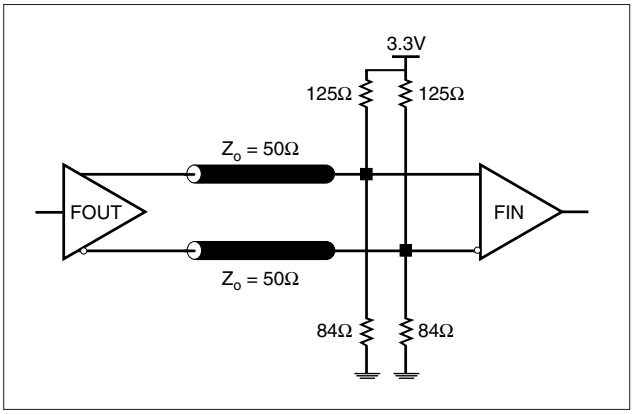


FIGURE 4B. LVPECL OUTPUT TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843206I.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS843206I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 10% = 3.63V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.63V * 120mA = **415.08mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 6 * 30mW = **180mW**

Total Power $_{MAX}$ (3.63V, with all outputs switching) = 415.08mW + 180mW = **595.08mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 59.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.595W * 59.6°C/W = 120.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 48-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	59.6°C/W	55.6°C/W	53.6°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

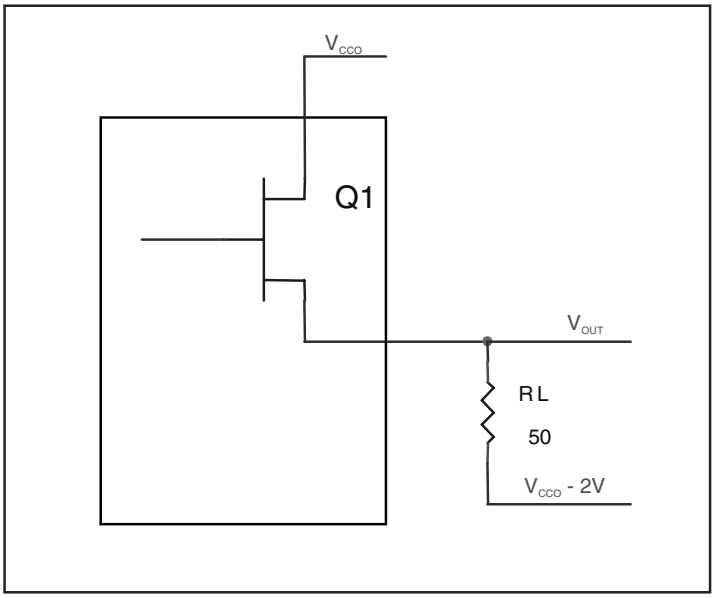


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) =$
$[(2V - 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 48 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	59.6°C/W	55.6°C/W	53.6°C/W

Transistor Count

The transistor count for ICS843206I is: 3957

Package Outline & Dimensions

Package Outline - G Suffix for 48 Lead TSSOP

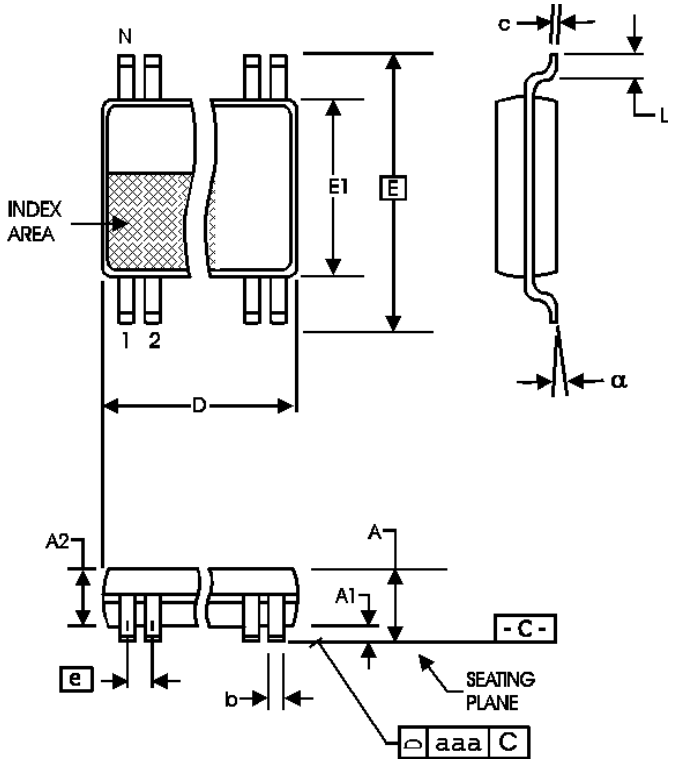


Table 8. Package Dimensions

SYMBOL	Millimeters	
	Minimum	**Maximum**
N	48	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.17	0.27
c	0.09	0.20
D	12.40	12.60
E	8.10 BASIC	
E1	6.00	6.20
e	0.50 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843206AGI	TBD	48 Lead TSSOP	tube	-40°C to 85°C
843206AGIT	TBD	48 Lead TSSOP	1000 tape & reel	-40°C to 85°C
843206AGILF	ICS843206AGILF	48 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
843206AGILFT	ICS843206AGILF	48 Lead "Lead-Free" TSSOP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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