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[ICS9P750CFLF](#)

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9P750CFLF

Category: Zero Delay Buffers

Generic Part: 9P750

Market Group: PC CLOCK

Description: PC BUFFER

Recommended Application: DDR Zero Delay Clock Buffer Product Description/Features: \bullet Low skew, low jitter PLL clock driver \bullet 12 pairs of differential outputs support up to DDR400 \bullet Outputs divided into 3 groups - Group A is reference - Groups B and C have default offsets from Group A, but also have skew programmable in steps relative to Group A - Skew step (unit) set via RSTEP resistor \bullet Static Phase Offset (SPO) of entire device can be programmed - RSPO sets overall SPO (analog delay) - I2C register settings allow fine tuning in steps defined by RSTEP \bullet Spread spectrum tolerant inputs \bullet 2.5 V differential reference clock input Switching Characteristics: \bullet PEAK - PEAK jitter (>100MHz): <75ps \bullet CYCLE - CYCLE jitter (>100MHz): <65ps \bullet OUTPUT - OUTPUT skew: <50ps \bullet DUTY CYCLE: 49% - 51% \bullet Slew rate: 1V/ns - 2V/ns \bullet Input clock duty cycle: 40% - 60%



Parameters

Package	SSOP 48 (PVG48)
Voltage	3.3 V
Package	SSOP 48
Speed	NA
Temperature	C
Status	Active
Sample	Yes
Minimum Order Quantity	90
Factory Order Increment	30

Distributor Inventory

No Pricing information is available from our Distributors at this time.

Documents

Type	Title	Size	Revision Date
Misc	PC Clocks Contact Info	61 KB	05/29/2007

Package

Description	SSOP 300 ML, 48LD
Class	PLASTIC
Moisture Sensitivity Level (MSL)	1
Category	Green
Moisture Exposure Floor Life	Unlimited @ <30°C/85% RH
Peak Reflow Temperature	260°C
Rebake Conditions	N/A
Length	15.9
Mark	PVG
Width	7.5
Pitch	0.64
Thickness	2.3
Status	Active