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AD8271

TABLE OF CONTENTS

Features	1	Circuit Information.....	15
Applications.....	1	Driving the AD8271.....	15
Functional Block Diagram	1	Power Supplies.....	15
General Description	1	Input Voltage Range.....	15
Revision History	2	Applications Information	16
Specifications.....	3	Difference Amplifier Configurations	16
Difference Amplifier Configurations	3	Single-Ended Configurations	17
Absolute Maximum Ratings.....	6	Kelvin Measurement.....	18
Thermal Resistance	6	Instrumentation Amplifier.....	18
Maximum Power Dissipation	6	Driving Cabling.....	19
ESD Caution.....	6	Driving an ADC	19
Pin Configuration and Function Description	7	Outline Dimensions	20
Typical Performance Characteristics	8	Ordering Guide	20
Operational Amplifier Plots.....	14		
Theory of Operation	15		

REVISION HISTORY

1/09—Revision 0: Initial Version

AD8271

SPECIFICATIONS

DIFFERENCE AMPLIFIER CONFIGURATIONS

$V_S = \pm 5$ to ± 15 V, $V_{REF} = 0$ V, $G = 1$, $R_{LOAD} = 2$ k Ω , $T_A = 25^\circ\text{C}$, specifications referred to input (RTI), unless otherwise noted.

Table 2.

Parameter	Conditions	B Grade			A Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
DYNAMIC PERFORMANCE								
Bandwidth		15			15			MHz
Slew Rate		30			30			V/ μ s
Settling Time to 0.01%	$V_S = \pm 15$, 10 V step on output	700	800		700	800		ns
	$V_S = \pm 5$, 5 V step on output	550	650		550	650		ns
Settling Time to 0.001%	$V_S = \pm 15$, 10 V step on output	750	900		750	900		ns
	$V_S = \pm 5$, 5 V step on output	600	750		600	750		ns
NOISE/DISTORTION								
Harmonic Distortion + Noise	$V_S = \pm 15$, $f = 1$ kHz, $V_{OUT} = 10$ V p-p, $R_{LOAD} = 600$ Ω	110			110			dB
	$V_S = \pm 5$, $f = 1$ kHz, $V_{OUT} = 10$ V p-p, $R_{LOAD} = 600$ Ω	141			141			dB
Voltage Noise ¹	$f = 0.1$ Hz to 10 Hz	1.5			1.5			μ V p-p
	$f = 1$ kHz	38			38			nV/ \sqrt Hz
GAIN								
Gain Error	$V_{OUT} = 10$ V p-p		0.02				0.05	%
Gain Drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1	2		1	10		ppm/ $^\circ\text{C}$
Gain Nonlinearity	$V_{OUT} = 10$ V p-p, $R_{LOAD} = 10$ k Ω , 2 k Ω , 600 Ω	1			1			ppm
INPUT CHARACTERISTICS								
Offset ²		300	600		300	1000		μ V
Average Temperature Drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	2			2			μ V/ $^\circ\text{C}$
Common-Mode Rejection Ratio	DC to 1 kHz	80	92		74	92		dB
Power Supply Rejection Ratio		2	10		2	10		μ V/V
Input Voltage Range ³	$-V_S - 0.4$	+ $V_S + 0.4$			$-V_S - 0.4$	+ $V_S + 0.4$		V
Common-Mode Resistance ⁴		10			10			k Ω
Bias Current	Inputs grounded	500			500			nA
OUTPUT CHARACTERISTICS								
Output Swing	$V_S = \pm 15$	-13.8	+13.8		-13.8	+13.8		V
	$V_S = \pm 15$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-13.7	+13.7		-13.7	+13.7		V
	$V_S = \pm 5$	-4	+4		-4	+4		V
	$V_S = \pm 5$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-3.9	+3.9		-3.9	+3.9		V
Short-Circuit Current Limit	Sourcing	100			100			mA
	Sinking	60			60			mA
POWER SUPPLY								
Supply Current		2.3	2.6		2.3	2.6		mA
	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	3.2			3.2			mA

¹ Includes amplifier voltage and current noise, as well as noise of internal resistors.

² Includes input bias and offset errors.

³ At voltages beyond the rails, internal ESD diodes begin to turn on. In some configurations, the input voltage range may be limited by the internal op amp (see the Input Voltage Range section for details).

⁴ Internal resistors, trimmed to be ratio matched, have $\pm 20\%$ absolute accuracy. Common-mode resistance was calculated with both inputs in parallel. The common-mode impedance at only one input is 2x the resistance listed.

AD8271

$V_S = \pm 5$ to ± 15 V, $V_{REF} = 0$ V, $G = 1/2$, $R_{LOAD} = 2$ k Ω , $T_A = 25^\circ\text{C}$, specifications referred to input (RTI), unless otherwise noted.

Table 3.

Parameter	Conditions	B Grade			A Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
DYNAMIC PERFORMANCE								
Bandwidth		20			20			MHz
Slew Rate		30			30			V/ μ s
Settling Time to 0.01%	$V_S = \pm 15$, 10 V step on output	700	800		700	800		ns
	$V_S = \pm 5$, 5 V step on output	550	650		550	650		ns
Settling Time to 0.001%	$V_S = \pm 15$, 10 V step on output	750	900		750	900		ns
	$V_S = \pm 5$, 5 V step on output	600	750		600	750		ns
NOISE/DISTORTION								
Harmonic Distortion + Noise	$V_S = \pm 15$, $f = 1$ kHz, $V_{OUT} = 10$ V p-p, $R_{LOAD} = 600$ Ω	74			74			dB
	$V_S = \pm 5$, $f = 1$ kHz, $V_{OUT} = 10$ V p-p, $R_{LOAD} = 600$ Ω	101			101			dB
Voltage Noise ¹	$f = 0.1$ Hz to 10 Hz	2			2			μ V p-p
	$f = 1$ kHz	52			52			nV/ $\sqrt{\text{Hz}}$
GAIN								
Gain Error	$V_{OUT} = 10$ V p-p		0.04			0.08		%
Gain Drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	0.5	2		1	10		$\mu\text{V}/^\circ\text{C}$
Gain Nonlinearity	$V_{OUT} = 10$ V p-p, $R_{LOAD} = 10$ k Ω , 2 k Ω , 600 Ω	200			200			ppm
INPUT CHARACTERISTICS								
Offset ²		450	1000		450	1500		μ V
Average Temperature Drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	3			3			$\mu\text{V}/^\circ\text{C}$
Common-Mode Rejection Ratio	DC to 1 kHz	74	86		70	86		dB
Power Supply Rejection Ratio		2	10		2	10		$\mu\text{V}/\text{V}$
Input Voltage Range ³	$-V_S - 0.4$	$+V_S + 0.4$			$-V_S - 0.4$	$+V_S + 0.4$		V
Common-Mode Resistance ⁴		7.5			7.5			k Ω
Bias Current	Inputs grounded	500			500			nA
OUTPUT CHARACTERISTICS								
Output Swing	$V_S = \pm 15$	-13.8	+13.8		-13.8	+13.8		V
	$V_S = \pm 15$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-13.7	+13.7		-13.7	+13.7		V
	$V_S = \pm 5$	-4	+4		-4	+4		V
	$V_S = \pm 5$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-3.9	+3.9		-3.9	+3.9		V
Short-Circuit Current Limit	Sourcing	100			100			mA
	Sinking	60			60			mA
POWER SUPPLY								
Supply Current		2.3	2.6		2.3	2.6		mA
			3.2			3.2		mA

¹ Includes amplifier voltage and current noise, as well as noise of internal resistors.

² Includes input bias and offset errors.

³ At voltages beyond the rails, internal ESD diodes begin to turn on. In some configurations, the input voltage range may be limited by the internal op amp (see the Input Voltage Range section for details).

⁴ Internal resistors, trimmed to be ratio matched, have $\pm 20\%$ absolute accuracy. Common-mode resistance was calculated with both inputs in parallel. The common-mode impedance at only one input is $2 \times$ the resistance listed.

AD8271

$V_S = \pm 5$ to ± 15 V, $V_{REF} = 0$ V, $G = 2$, $R_{LOAD} = 2$ k Ω , $T_A = 25^\circ\text{C}$, specifications referred to input (RTI), unless otherwise noted.

Table 4.

Parameter	Conditions	B Grade			A Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
DYNAMIC PERFORMANCE								
Bandwidth			10			10		MHz
Slew Rate			30			30		V/ μ s
Settling Time to 0.01%	$V_S = \pm 15$, 10 V step on output	700	800		700	800		ns
	$V_S = \pm 5$, 5 V step on output	550	650		550	650		ns
Settling Time to 0.001%	$V_S = \pm 15$, 10 V step on output	750	900		750	900		ns
	$V_S = \pm 5$, 5 V step on output	600	750		600	750		ns
NOISE/DISTORTION								
Harmonic Distortion + Noise	$V_S = \pm 15$, $f = 1$ kHz, $V_{OUT} = 10$ V p-p, $R_{LOAD} = 600$ Ω		86			86		dB
	$V_S = \pm 5$, $f = 1$ kHz, $V_{OUT} = 10$ V p-p, $R_{LOAD} = 600$ Ω		112			112		dB
Voltage Noise ¹	$f = 0.1$ Hz to 10 Hz		1			1		μ V p-p
	$f = 1$ kHz		26			26		nV/ $\sqrt{\text{Hz}}$
GAIN								
Gain Error	$V_{OUT} = 10$ V p-p		0.04			0.08		%
Gain Drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	0.5	2		1	10		ppm/ $^\circ\text{C}$
Gain Nonlinearity	$V_{OUT} = 10$ V p-p, $R_{LOAD} = 10$ k Ω , 2 k Ω , 600 Ω	50			50			ppm
INPUT CHARACTERISTICS								
Offset ²		225	500		225	750		μ V
Average Temperature Drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1.5			1.5			μ V/ $^\circ\text{C}$
Common-Mode Rejection Ratio	DC to 1 kHz	84	98	78	98			dB
Power Supply Rejection Ratio		2	10	2	10			μ V/V
Input Voltage Range ³	$-V_S - 0.4$	$+V_S + 0.4$	$-V_S - 0.4$	$+V_S + 0.4$				V
Common-Mode Resistance ⁴		7.5		7.5				k Ω
Bias Current	Inputs grounded		500		500			nA
OUTPUT CHARACTERISTICS								
Output Swing	$V_S = \pm 15$	-13.8	+13.8	-13.8	+13.8			V
	$V_S = \pm 15$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-13.7	+13.7	-13.7	+13.7			V
	$V_S = \pm 5$	-4	+4	-4	+4			V
	$V_S = \pm 5$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-3.9	+3.9	-3.9	+3.9			V
Short-Circuit Current Limit	Sourcing	100		100				mA
	Sinking	60		60				mA
POWER SUPPLY								
Supply Current		2.3	2.6	2.3	2.6			mA
	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		3.2		3.2			mA

¹ Includes amplifier voltage and current noise, as well as noise of internal resistors.

² Includes input bias and offset errors.

³ At voltages beyond the rails, internal ESD diodes begin to turn on. In some configurations, the input voltage range may be limited by the internal op amp (see the Input Voltage Range section for details).

⁴ Internal resistors, trimmed to be ratio matched, have $\pm 20\%$ absolute accuracy. Common-mode resistance was calculated with both inputs in parallel. The common-mode impedance at only one input is 2x the resistance listed.

AD8271

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	± 18 V
Output Short-Circuit Current	See derating curve in Figure 2
Input Voltage Range	$+V_S + 0.4$ V to $-V_S - 0.4$ V
Storage Temperature Range	-65°C to $+130^{\circ}\text{C}$
Specified Temperature Range	-40°C to $+85^{\circ}\text{C}$
Package Glass Transition Temperature (T_g)	150°C
ESD	
Human Body Model	1 kV
Charge Device Model	1 kV
Machine Model	0.1 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
10-Lead MSOP	141.9	43.7	°C/W

The θ_{JA} values in Table 6 assume a 4-layer JEDEC standard board with zero airflow.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the AD8271 is limited by the associated rise in junction temperature (T_j) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a temperature of 150°C for an extended period of time can cause changes in silicon devices, potentially resulting in a loss of functionality.

The AD8271 has built-in short-circuit protection that limits the output current to approximately 100 mA (see Figure 22 for more information). Although the short-circuit condition itself does not damage the part, the heat generated by the condition can cause the part to exceed its maximum junction temperature, with corresponding negative effects on reliability.

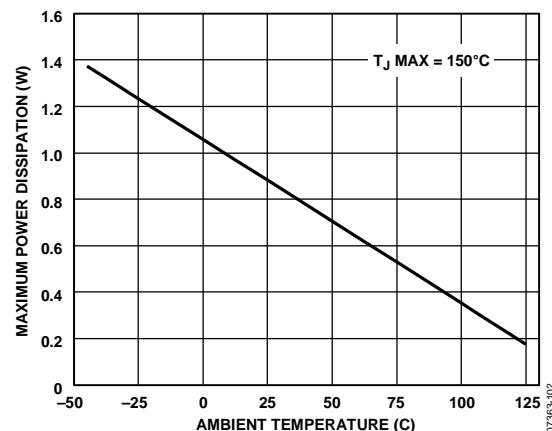


Figure 2. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device.
 Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

AD8271

PIN CONFIGURATION AND FUNCTION DESCRIPTION

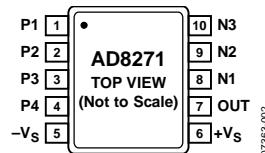


Figure 3.

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	P1	Noninverting Input. A 10 kΩ resistor is connected to the noninverting (+) terminal of the op amp.
2	P2	Noninverting Input. A 10 kΩ resistor is connected to the noninverting (+) terminal of the op amp.
3	P3	Noninverting Input. A 20 kΩ resistor is connected to the noninverting (+) terminal of the op amp. This pin is used as a reference voltage input in many configurations.
4	P4	Noninverting Input. A 20 kΩ resistor is connected to the noninverting (+) terminal of the op amp. This pin is used as a reference voltage input in many configurations.
5	-Vs	Negative Supply.
6	+Vs	Positive Supply.
7	OUT	Output.
8	N1	Inverting Input. A 10 kΩ resistor is connected to the inverting (-) terminal of the op amp.
9	N2	Inverting Input. A 10 kΩ resistor is connected to the inverting (-) terminal of the op amp.
10	N3	Inverting Input. A 10 kΩ resistor is connected to the inverting (-) terminal of the op amp.

AD8271

TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = \pm 15$ V, $T_A = 25^\circ\text{C}$, difference amplifier configuration, unless otherwise noted.

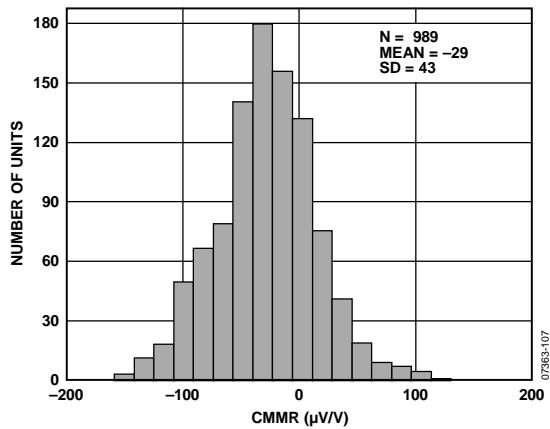


Figure 4. Typical Distribution of CMRR, Gain = 1

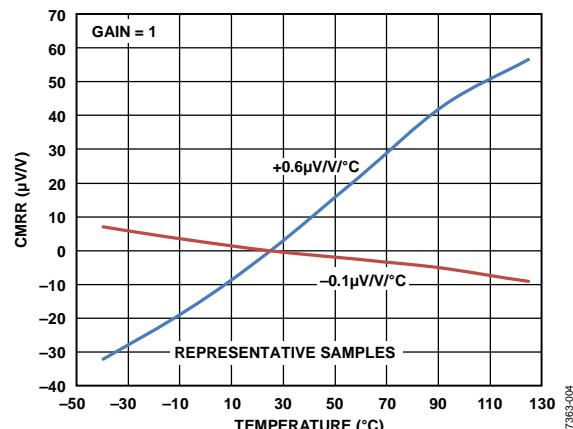


Figure 7. CMRR vs. Temperature, Normalized at 25°C, Gain = 1

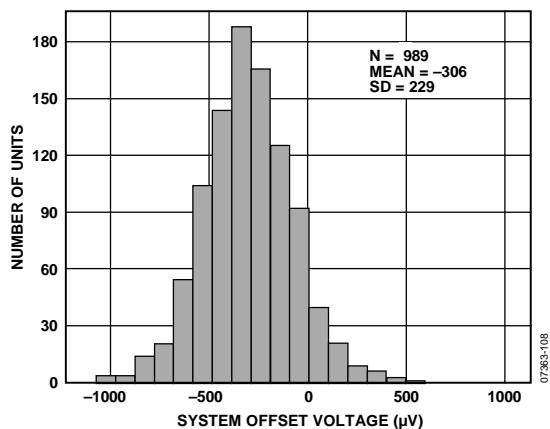


Figure 5. Typical Distribution of System Offset, Gain = 1

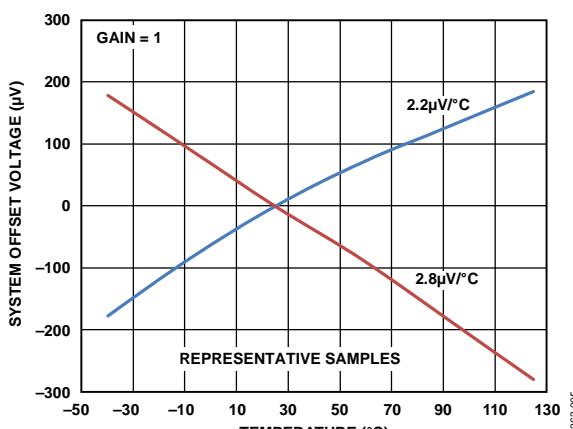


Figure 8. System Offset vs. Temperature, Normalized at 25°C, Referred to Output, Gain = 1

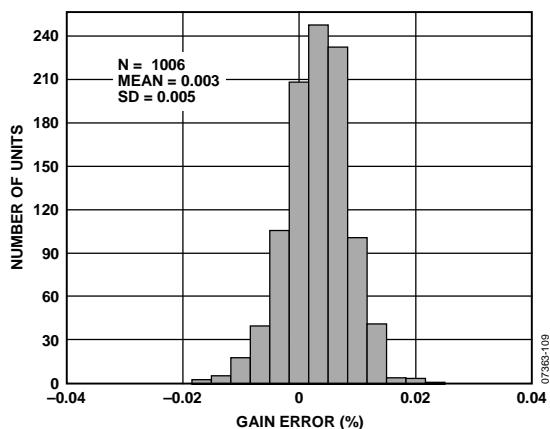


Figure 6. Typical Distribution of Gain Error, Gain = 1

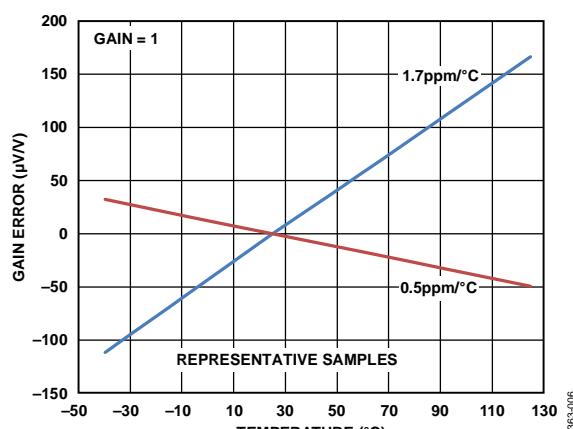


Figure 9. Gain Error vs. Temperature, Normalized at 25°C, Gain = 1

AD8271

$V_S = \pm 15$ V, $T_A = 25^\circ\text{C}$, difference amplifier configuration, unless otherwise noted.

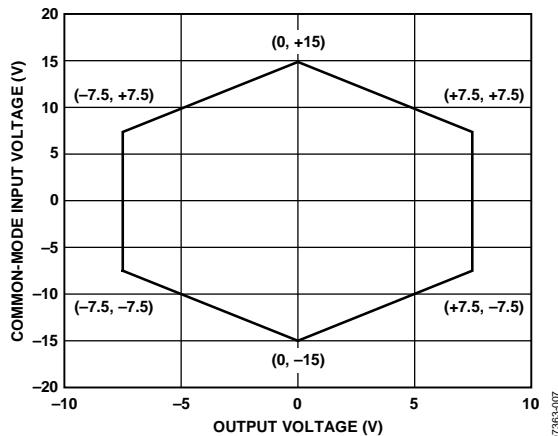


Figure 10. Common-Mode Input Voltage vs. Output Voltage,
Gain = $\frac{1}{2}$, ± 15 V Supplies

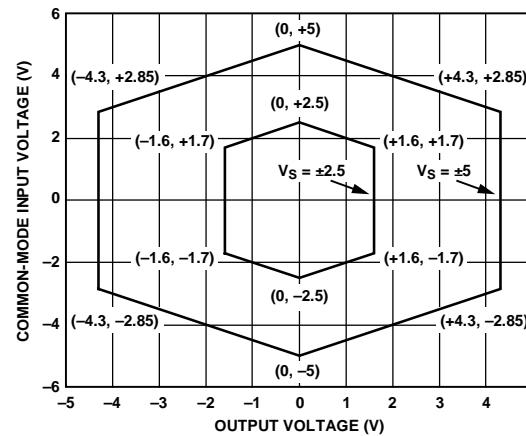


Figure 13. Common-Mode Input Voltage vs. Output Voltage,
Gain = 1, ± 5 V and ± 2.5 V Supplies

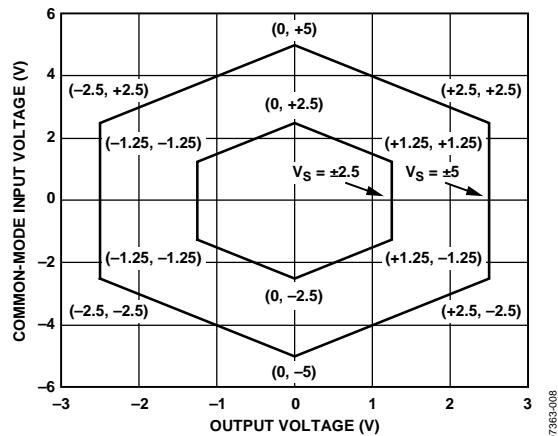


Figure 11. Common-Mode Input Voltage vs. Output Voltage,
Gain = $\frac{1}{2}$, ± 5 V and ± 2.5 V Supplies

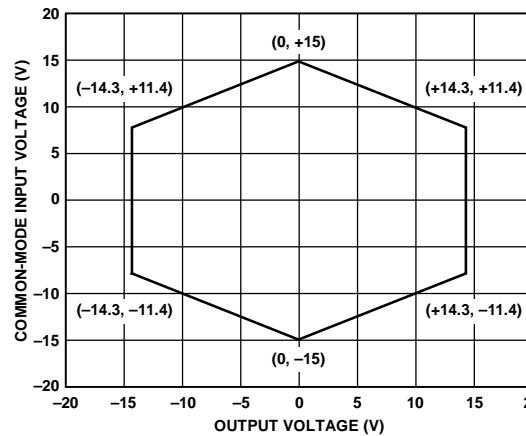


Figure 14. Common-Mode Input Voltage vs. Output Voltage,
Gain = 2, ± 15 V Supplies

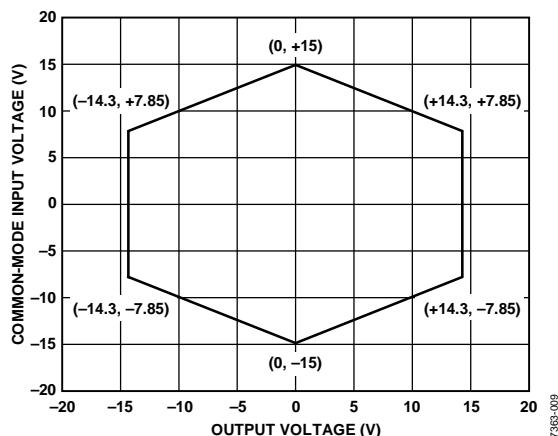


Figure 12. Common-Mode Input Voltage vs. Output Voltage,
Gain = 1, ± 15 V Supplies

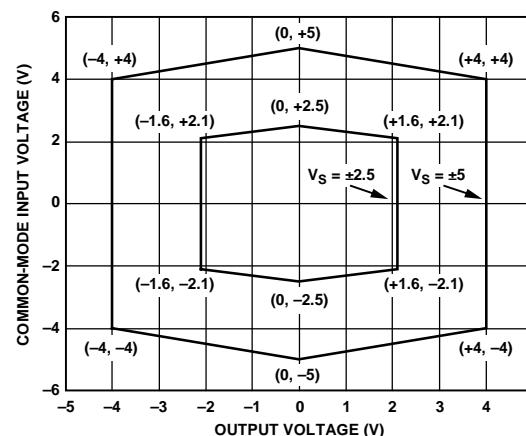


Figure 15. Common-Mode Input Voltage vs. Output Voltage,
Gain = 2, ± 5 V and ± 2.5 V Supplies

AD8271

$V_S = \pm 15$ V, $T_A = 25^\circ\text{C}$, difference amplifier configuration, unless otherwise noted.

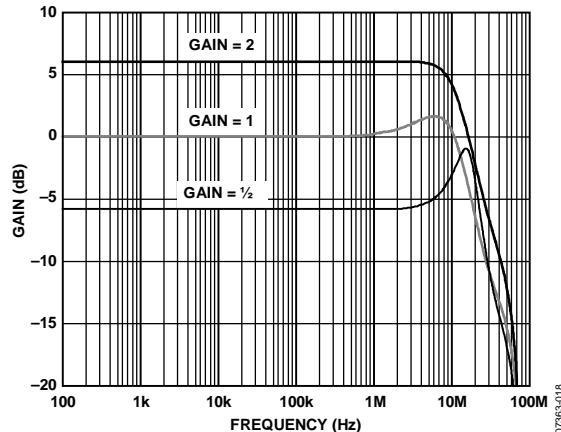


Figure 16. Gain vs. Frequency

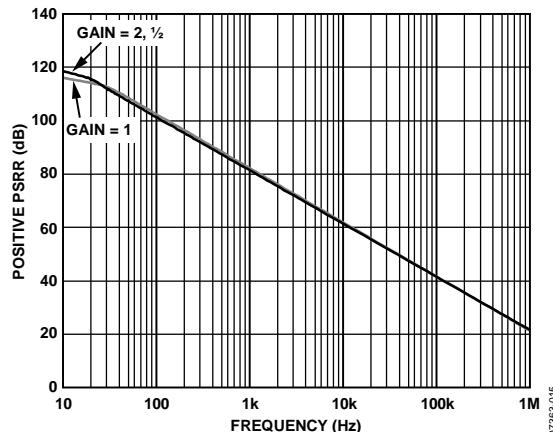


Figure 19. Positive PSRR vs. Frequency

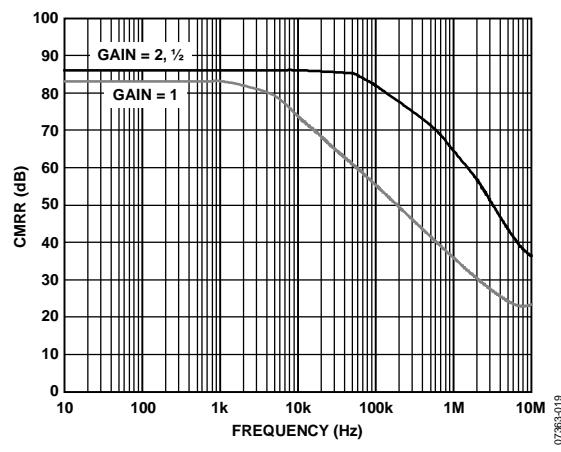


Figure 17. CMRR vs. Frequency

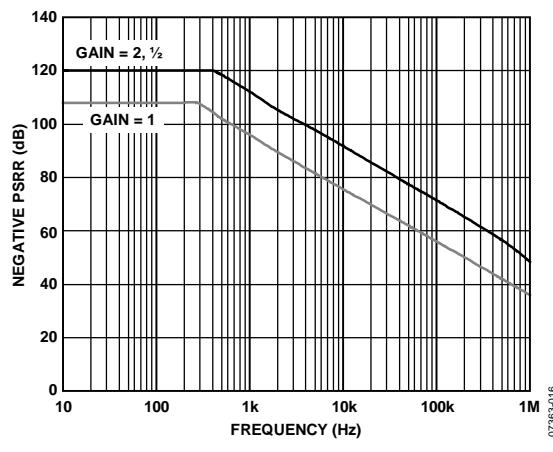


Figure 20. Negative PSRR vs. Frequency

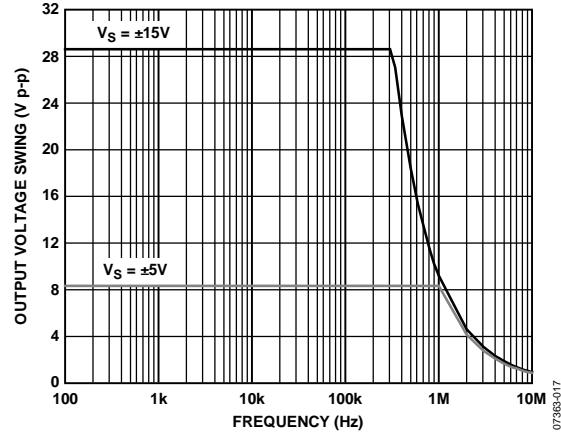


Figure 18. Output Voltage Swing vs. Large-Signal Frequency Response

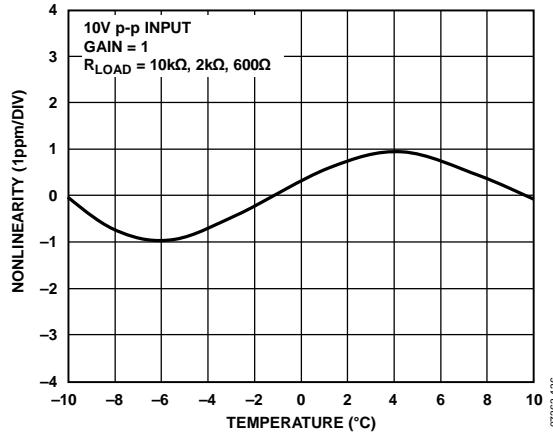


Figure 21. Gain Nonlinearity, Gain = 1

AD8271

$V_S = \pm 15$ V, $T_A = 25^\circ\text{C}$, difference amplifier configuration, unless otherwise noted.

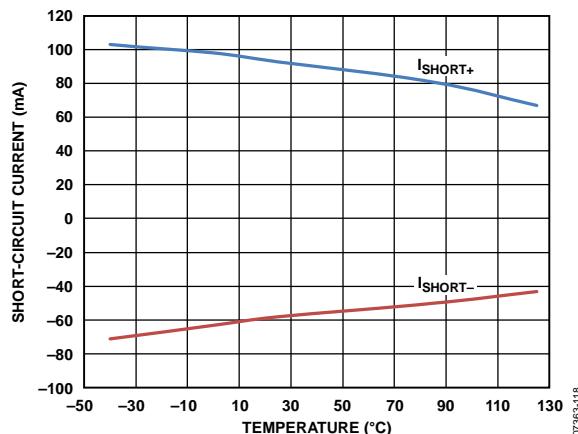


Figure 22. Short-Circuit Current vs. Temperature

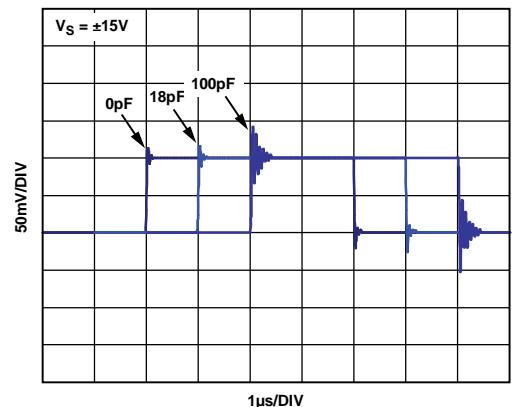


Figure 25. Small-Signal Step Response, Gain = $1/2$

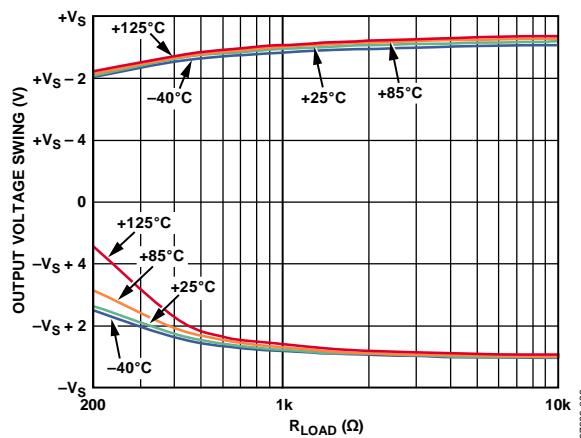


Figure 23. Output Voltage Swing vs. R_{LOAD}

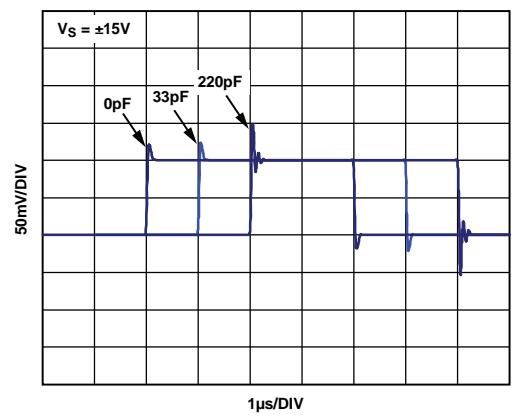


Figure 26. Small-Signal Step Response, Gain = 1

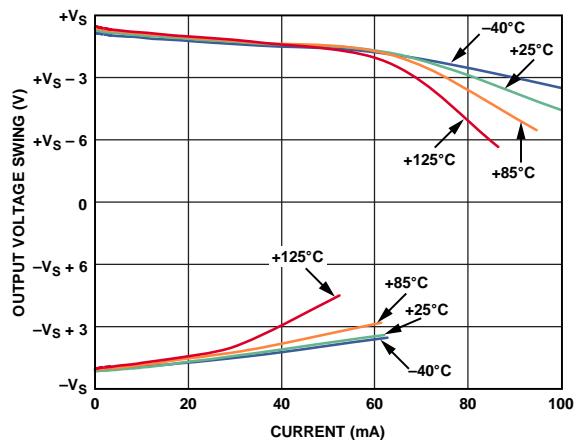


Figure 24. Output Voltage Swing vs. Current (I_{OUT})

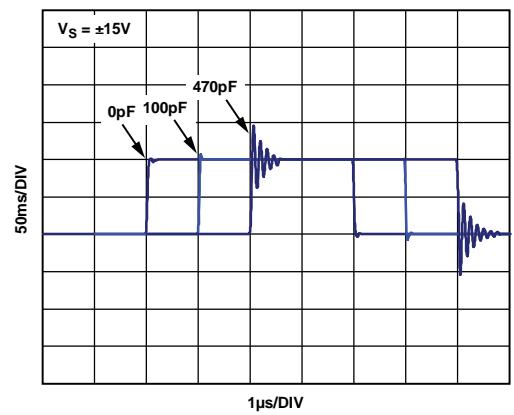


Figure 27. Small-Signal Step Response, Gain = 2

AD8271

$V_S = \pm 15$ V, $T_A = 25^\circ\text{C}$, difference amplifier configuration, unless otherwise noted.

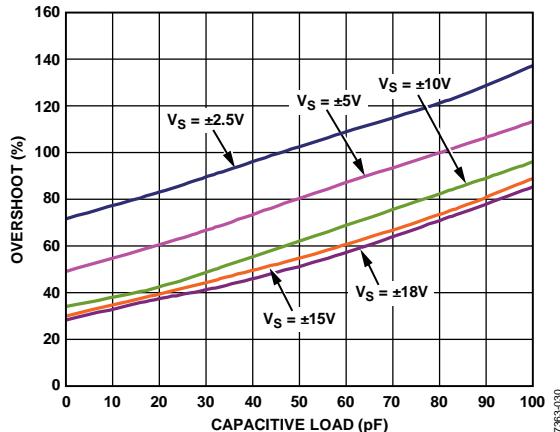


Figure 28. Small-Signal Overshoot vs. Capacitive Load, Gain = $\frac{1}{2}$

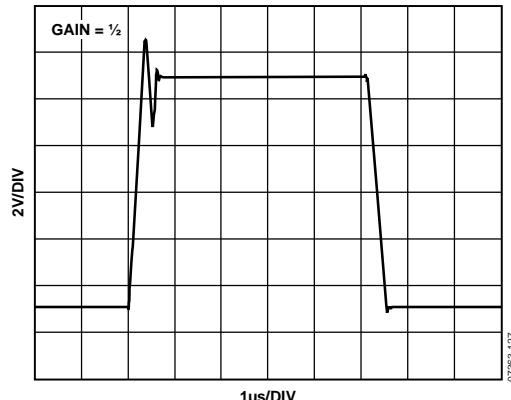


Figure 31. Large-Signal Pulse Response, Gain = $\frac{1}{2}$

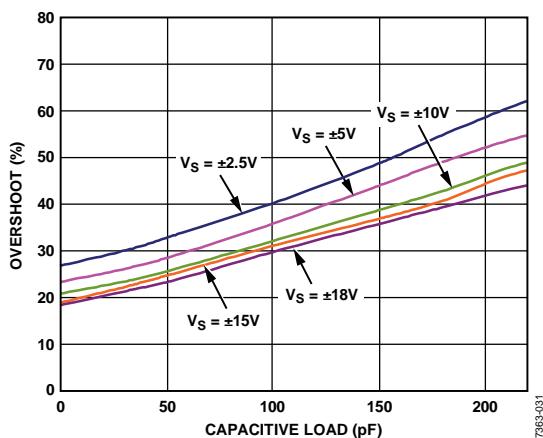


Figure 29. Small-Signal Overshoot vs. Capacitive Load, Gain = 1

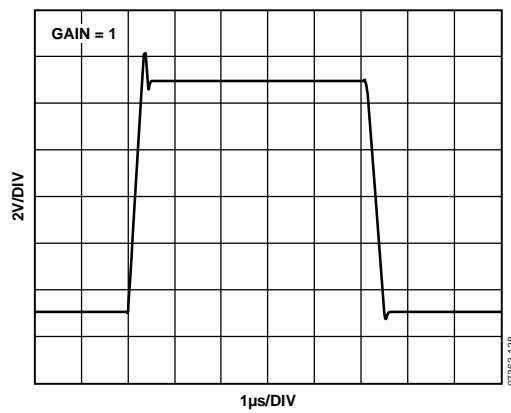


Figure 32. Large-Signal Pulse Response, Gain = 1

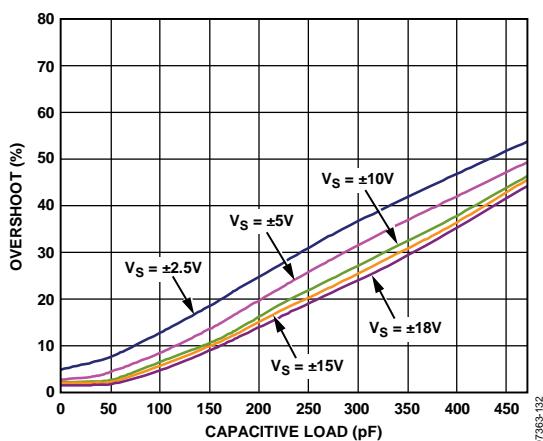


Figure 30. Small-Signal Overshoot vs. Capacitive Load, Gain = 2

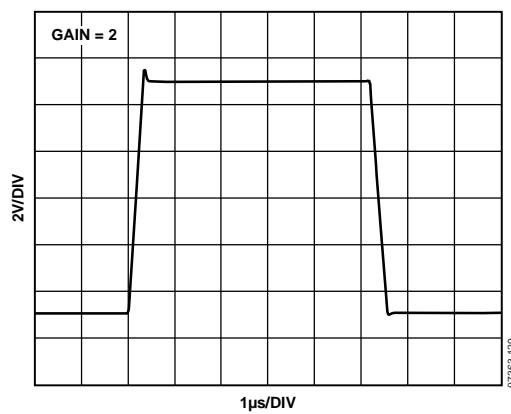


Figure 33. Large-Signal Pulse Response, Gain = 2

AD8271

$V_S = \pm 15$ V, $T_A = 25^\circ\text{C}$, difference amplifier configuration, unless otherwise noted.

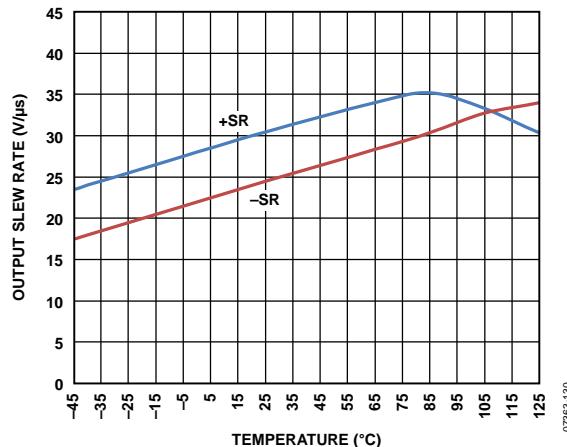


Figure 34. Output Slew Rate vs. Temperature

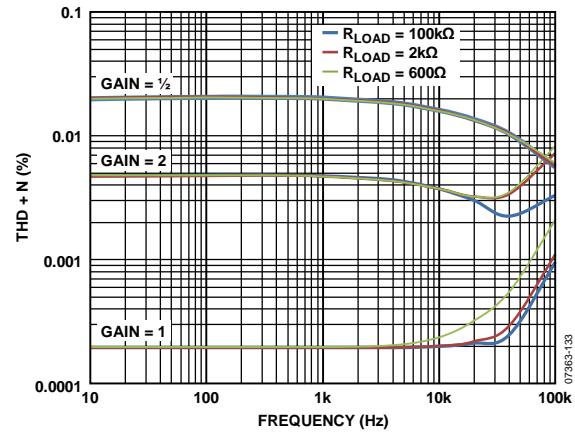


Figure 37. THD + N vs. Frequency

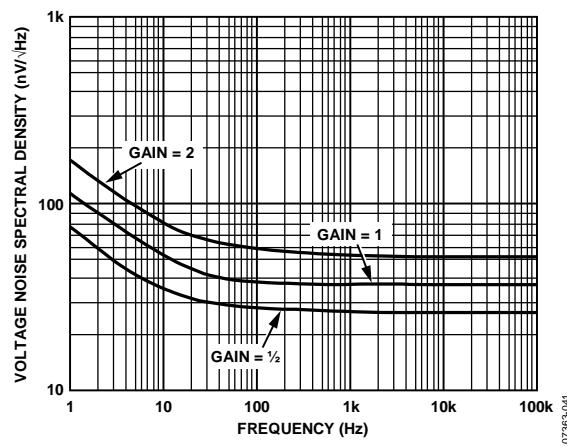


Figure 35. Voltage Noise Spectral Density vs. Frequency, Referred to Output

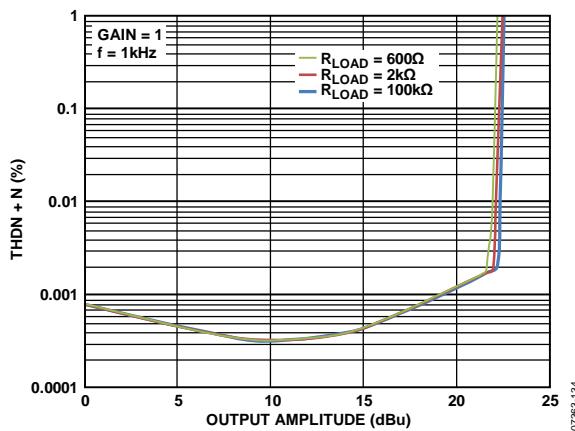


Figure 38. THD + N vs. Output Amplitude, Gain = 1

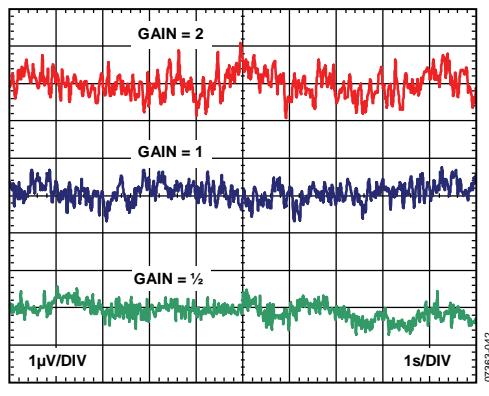


Figure 36. 0.1 Hz to 10 Hz Voltage Noise, Referred to Output

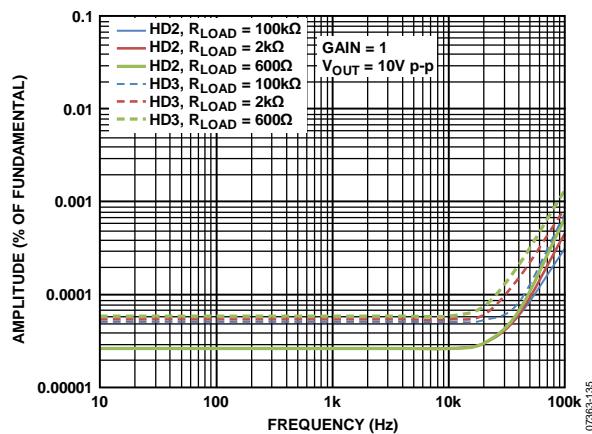


Figure 39. Harmonic Distortion Products vs. Frequency, Gain = 1

AD8271

OPERATIONAL AMPLIFIER PLOTS

$V_S = \pm 15$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted.

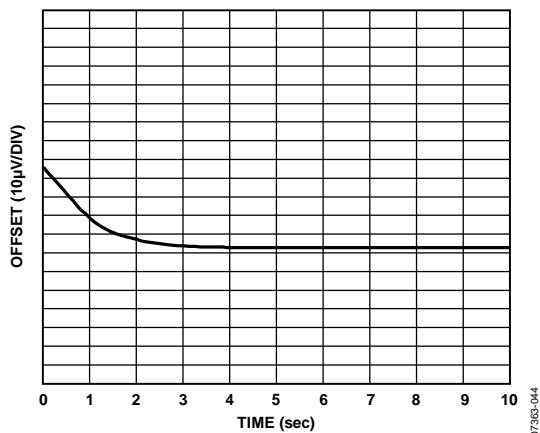


Figure 40. Change in Op Amp Offset Voltage vs. Warm-Up Time

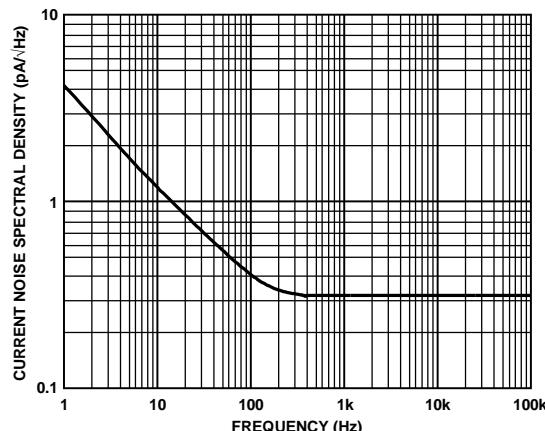


Figure 42. Current Noise Spectral Density vs. Frequency

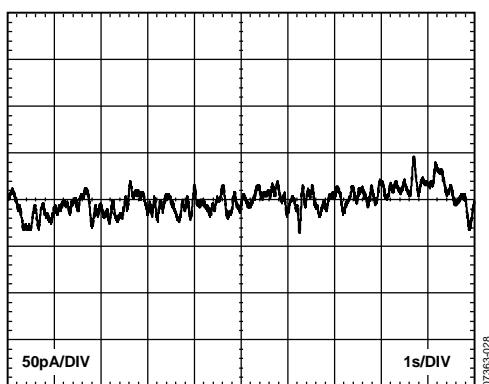


Figure 41. 0.1 Hz to 10 Hz Current Noise

AD8271

APPLICATIONS INFORMATION

The resistors and connections provided on the AD8271 offer abundant versatility through the variety of configurations that are possible.

DIFFERENCE AMPLIFIER CONFIGURATIONS

The AD8271 can be placed in difference amplifier configurations with gains of $\frac{1}{2}$, 1, and 2. Figure 45 through Figure 47 show sample difference amplifier configurations referenced to ground.

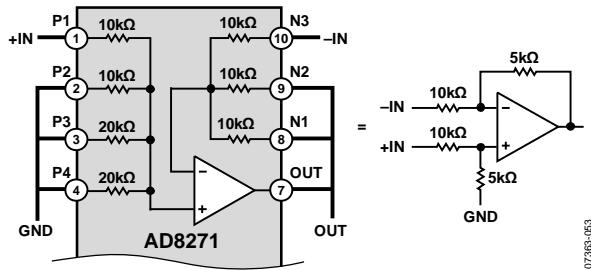


Figure 45. Gain = $\frac{1}{2}$ Difference Amplifier, Referenced to Ground

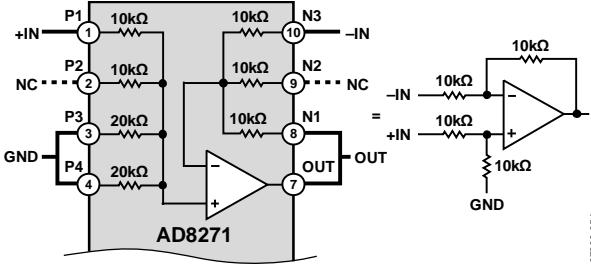


Figure 46. Gain = 1 Difference Amplifier, Referenced to Ground

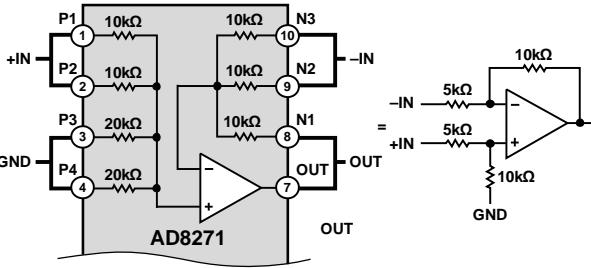


Figure 47. Gain = 2 Difference Amplifier, Referenced to Ground

The AD8271 can also be referred to a combination of reference voltages. For example, the reference can be set at 2.5 V, using just 5 V and GND. Some of the possible configurations are shown in Figure 48 through Figure 50. Note that the output is not internally tied to a feedback path, so any of the 10 kΩ resistors on the inverting input can be used in the feedback network. This flexibility allows for more efficient board layout options.

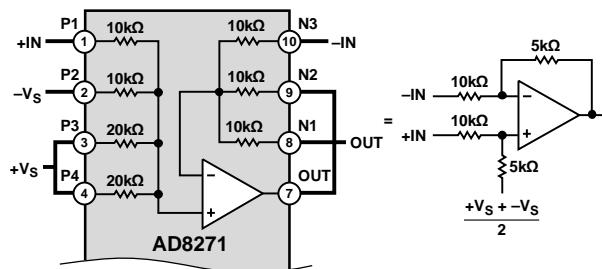


Figure 48. Gain = $\frac{1}{2}$ Difference Amplifier, Referenced to Midsupply

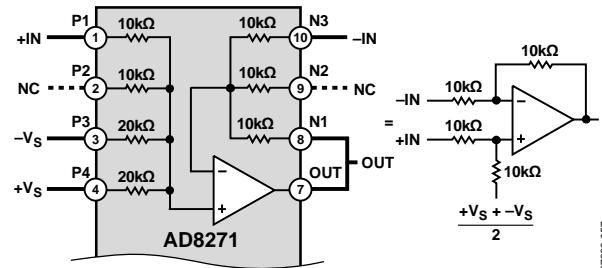


Figure 49. Gain = 1 Difference Amplifier, Referenced to Midsupply

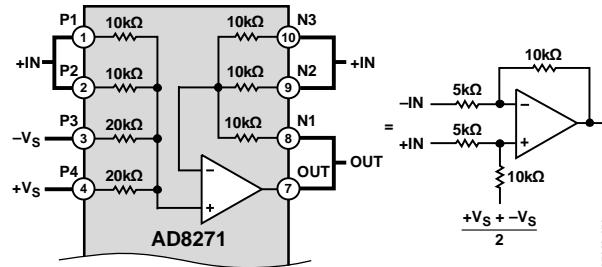


Figure 50. Gain = 2 Difference Amplifier, Referenced to Midsupply

Table 8. Pin Connections for Difference Amplifier Configurations

Gain and Reference	Configuration						
	Pin 1 (P1)	Pin 2 (P2)	Pin 3 (P3)	Pin 4 (P4)	Pin 8 (N1)	Pin 9 (N2)	Pin 10 (N3)
Gain of $\frac{1}{2}$, Referenced to Ground	+IN	GND	GND	GND	OUT	OUT	-IN
Gain of $\frac{1}{2}$, Referenced to Midsupply	+IN	-VS	+VS	+VS	OUT	OUT	-IN
Gain of 1, Referenced to Ground	+IN	NC	GND	GND	OUT	NC	-IN
Gain of 1, Referenced to Midsupply	+IN	NC	-VS	+VS	OUT	NC	-IN
Gain of 2, Referenced to Ground	+IN	+IN	GND	GND	OUT	-IN	-IN
Gain of 2, Referenced to Midsupply	+IN	+IN	-VS	+VS	OUT	-IN	-IN

SINGLE-ENDED CONFIGURATIONS

The AD8271 can be configured for a wide variety of single-ended configurations with gains ranging from -2 to $+3$ (see Table 9).

Table 9. Selected Single-Ended Configurations

Signal Gain	Electrical Performance		Configuration						
	Op Amp Closed-Loop Gain	Input Resistance	Pin 10¹	Pin 9¹	Pin 8¹	Pin 1²	Pin 2²	Pin 3³	Pin 4³
-2	3	5 k Ω	IN	IN	OUT	GND	GND	GND	GND
-1.5	3	4.8 k Ω	IN	IN	OUT	GND	GND	GND	IN
-1.4	3	5 k Ω	IN	IN	OUT	GND	GND	NC	IN
-1.25	3	5.333 k Ω	IN	IN	OUT	GND	NC	GND	IN
-1	3	5 k Ω	IN	IN	OUT	GND	GND	IN	IN
-0.8	3	5.556 k Ω	IN	IN	OUT	IN	GND	NC	GND
-0.667	2	8 k Ω	IN	NC	OUT	GND	GND	GND	IN
-0.6	2	8.333 k Ω	IN	NC	OUT	GND	GND	NC	IN
-0.5	2	8.889 k Ω	IN	NC	OUT	GND	NC	GND	IN
-0.333	2	7.5 k Ω	IN	NC	OUT	GND	GND	IN	IN
-0.25	1.5	8 k Ω	OUT	IN	OUT	GND	GND	GND	IN
-0.2	1.5	8.333 k Ω	OUT	IN	OUT	GND	GND	NC	IN
-0.125	1.5	8.889 k Ω	OUT	IN	OUT	GND	NC	GND	IN
+0.1	1.5	8.333 k Ω	OUT	IN	OUT	IN	GND	NC	GND
+0.2	2	10 k Ω	IN	NC	OUT	GND	IN	NC	IN
+0.25	1.5	24 k Ω	OUT	GND	OUT	GND	GND	GND	IN
+0.3	1.5	25 k Ω	OUT	GND	OUT	GND	GND	NC	IN
+0.333	2	24 k Ω	GND	NC	OUT	GND	GND	GND	IN
+0.375	1.5	26.67 k Ω	OUT	GND	OUT	GND	NC	GND	IN
+0.4	2	25 k Ω	GND	NC	OUT	GND	GND	NC	IN
+0.5	3	24 k Ω	GND	GND	OUT	GND	GND	GND	IN
+0.5	1.5	15 k Ω	OUT	GND	OUT	GND	GND	IN	IN
+0.6	3	25 k Ω	GND	GND	OUT	GND	GND	NC	IN
+0.6	1.5	16.67 k Ω	OUT	GND	OUT	IN	GND	NC	GND
+0.625	1.5	16 k Ω	OUT	IN	OUT	NC	IN	IN	GND
+0.667	2	15 k Ω	GND	NC	OUT	GND	GND	IN	IN
+0.7	1.5	16.67 k Ω	OUT	IN	OUT	IN	IN	NC	GND
+0.75	3	26.67 k Ω	GND	GND	OUT	GND	NC	GND	IN
+0.75	1.5	13.33 k Ω	OUT	GND	OUT	GND	IN	GND	IN
+0.8	2	16.67 k Ω	GND	NC	OUT	IN	GND	NC	GND
+0.9	1.5	16.67 k Ω	OUT	GND	OUT	GND	IN	NC	IN
+1	1.5	15 k Ω	OUT	GND	OUT	IN	IN	GND	GND
+1	1.5	>1 G Ω	OUT	IN	OUT	IN	IN	IN	IN
+1	3	>1 G Ω	IN	IN	OUT	IN	IN	IN	IN
+1.125	1.5	26.67 k Ω	OUT	GND	OUT	NC	IN	IN	GND
+1.2	3	16.67 k Ω	GND	GND	OUT	IN	GND	NC	GND
+1.2	1.5	25 k Ω	OUT	GND	OUT	IN	IN	NC	GND
+1.25	1.5	24 k Ω	OUT	GND	OUT	IN	IN	IN	GND
+1.333	2	15 k Ω	GND	NC	OUT	IN	IN	GND	GND
+1.5	3	13.33 k Ω	GND	GND	OUT	GND	IN	GND	IN
+1.5	1.5	>1 G Ω	OUT	GND	OUT	IN	IN	IN	IN
+1.6	2	25 k Ω	GND	NC	OUT	IN	IN	NC	GND
+1.667	2	24 k Ω	GND	NC	OUT	IN	IN	IN	GND
+1.8	3	16.67 k Ω	GND	GND	OUT	GND	IN	NC	IN
+2	2	>1 G Ω	GND	NC	OUT	IN	IN	IN	IN
+2.25	3	26.67 k Ω	GND	GND	OUT	NC	IN	IN	GND
+2.4	3	25 k Ω	GND	GND	OUT	IN	IN	NC	GND
+2.5	3	24 k Ω	GND	GND	OUT	IN	IN	IN	GND
+3	3	>1 G Ω	GND	GND	OUT	IN	IN	IN	IN

¹ A 10 k Ω resistor is connected to the inverting (–) terminal of the op amp.

² A 10 k Ω resistor is connected to the noninverting (+) terminal of the op amp.

³ A 20 k Ω resistor is connected to the noninverting (+) terminal of the op amp.

AD8271

Many signal gains have more than one configuration choice, which allows freedom in choosing the op amp closed-loop gain. In general, for designs that need to be stable with a large capacitive load on the output, choose a configuration with high loop gain. Otherwise, choose a configuration with low loop gain, because these configurations typically have lower noise, lower offset, and higher bandwidth.

The AD8271 Specifications section and Typical Performance Characteristics section show the performance of the part primarily when it is in the difference amplifier configuration. To estimate the performance of the part in a single-ended configuration, refer to the difference amplifier configuration with the corresponding closed-loop gain (see Table 10).

Table 10. Closed-Loop Gain of the Difference Amplifiers

Difference Amplifier Gain	Closed-Loop Gain
0.5	1.5
1	2
2	3

Gain of 1 Configuration

The AD8271 is designed to be stable for loop gains of 1.5 and greater. Because a typical voltage follower configuration has a loop gain of 1, it may be unstable. Several stable configurations for gain of 1 are listed in Table 9.

KELVIN MEASUREMENT

In the case where the output load is located remotely or at a distance from the AD8271, as shown in Figure 51, wire resistance can actually cause significant errors at the load.

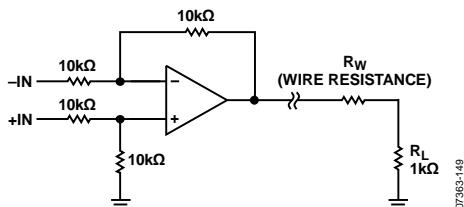


Figure 51. Wire Resistance Causes Errors at Load Voltage

Since the output of the AD8271 is not internally tied to any of the feedback resistors, Kelvin type measurements are possible because the op amp output and feedback can both be connected closer to the load (Figure 52). The Kelvin sensing on the feedback minimizes error at the load caused by voltage drops across the wire resistance. This technique is most effective in reducing errors for loads less than 10 kΩ. As the load resistance increases, the error due to the wire resistance becomes less significant.

Because it adds the sense wire resistance to the feedback resistor, a trade-off of the Kelvin connection is that it can degrade common-mode rejection, especially over temperature. For sense wire resistance less than 1 Ω, it is typically not an issue. If common-mode performance is critical, two amplifier stages can be used: the first stage removes common-mode interference, and the second stage performs the Kelvin drive.

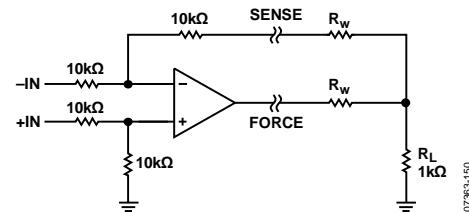


Figure 52. Connecting Both the Output and Feedback at the Load Minimizes Error Due to Wire Resistance

INSTRUMENTATION AMPLIFIER

The AD8271 can be used as a building block for high performance instrumentation amplifiers. For example, Figure 53 shows how to build an ultralow noise instrumentation amplifier using the AD8599 dual op amp. External resistors R_G and R_{F_x} provide gain; therefore, the output is

$$V_{OUT} = (V_{+IN} - V_{-IN}) \left(1 + \frac{2R_{F_x}}{R_G} \right) (G_{AD8271})$$

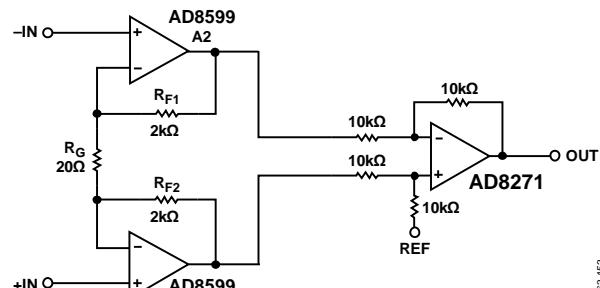


Figure 53. Ultralow Noise Instrumentation Amplifier Using AD8599 Configured for Gain = 201

For optimal noise performance, it is desirable to have a high gain at the input stage using low value gain-setting resistors, as shown in this particular example. With less than 2 nV/√Hz input-referred noise (see Figure 54) at ~10 mA supply current, the AD8271 and AD8599 combination offers an in-amp with a fine balance of critical specifications: a gain bandwidth product of 10 MHz, low bias current, low offset drift, high CMRR, and high slew rate.

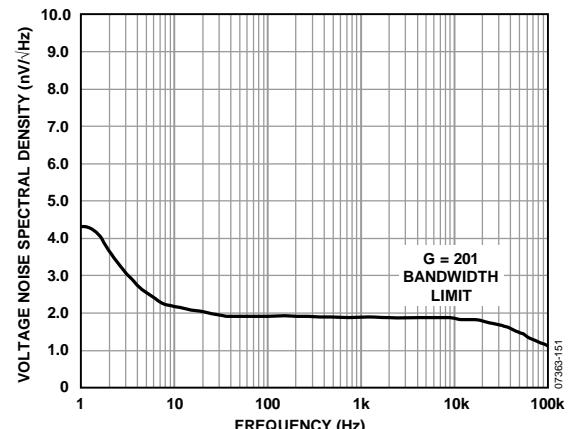


Figure 54. Ultralow Noise In-Amp Voltage Noise Spectral Density vs. Frequency, Referred to Input

DRIVING CABLING

Because the AD8271 can drive large voltages at high output currents and slew rates, it makes an excellent cable driver. It is good practice to put a small value resistor between the AD8271 output and cable, since capacitance in the cable can cause peaking or instability in the output response. A resistance of $20\ \Omega$ or higher is recommended.

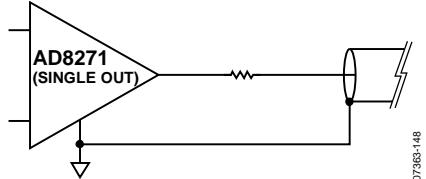


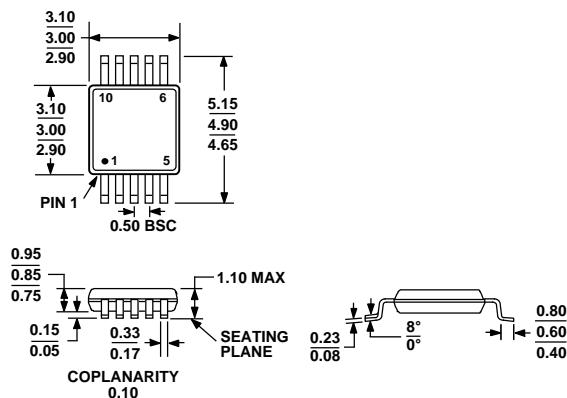
Figure 55. Driving Cabling

DRIVING AN ADC

The AD8271 high slew rate and drive capability, combined with its dc accuracy, make it a good ADC driver. The AD8271 can drive single-ended input ADCs. Many converters require the output to be buffered with a small value resistor combined with a high quality ceramic capacitor. See the relevant converter data sheet for more details.

AD8271

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA
Figure 56. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions are shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8271ARMZ ¹	-40°C to +85°C	10-Lead MSOP	RM-10	Y1E
AD8271ARMZ-R7 ¹	-40°C to +85°C	10-Lead MSOP, 7" Tape and Reel	RM-10	Y1E
AD8271ARMZ-RL ¹	-40°C to +85°C	10-Lead MSOP, 13" Tape and Reel	RM-10	Y1E
AD8271BRMZ ¹	-40°C to +85°C	10-Lead MSOP	RM-10	Y1G
AD8271BRMZ-R7 ¹	-40°C to +85°C	10-Lead MSOP, 7" Tape and Reel	RM-10	Y1G
AD8271BRMZ-RL ¹	-40°C to +85°C	10-Lead MSOP, 13" Tape and Reel	RM-10	Y1G

¹ Z = RoHS Compliant Part.