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Maxim Integrated
MAX17094ETM+

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Distributor of Maxim Integrated: Excellent Integrated System Limited
Datasheet of MAX17094ETM+ - IC REG BOOST ADJ 2A 7OUT 48TQFN
Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com

RELIABILITY REPORT

FOR

MAX17094ETM+

PLASTIC ENCAPSULATED DEVICES

May 16, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Ken Wendel
Quality Assurance
Director, Reliability Engineering

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Conclusion

The MAX17094ETM+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX17094 includes a high-performance step-up regulator, a 250mA low-dropout (LDO) linear regulator, a high-speed operational amplifier, a digitally adjustable VCOM calibration device with nonvolatile memory and I2C interface, and seven integrated high-voltage level shifters. The device is optimized for thin-film transistor (TFT) liquid-crystal display (LCD) applications. The step-up DC-DC converter is a current-mode regulator that provides the regulated supply voltage for panel source driver ICs. The current-mode architecture provides fast-transient responses to pulsed loads typical of source driver loads. The high switching frequency, which is programmable to any frequency between 450kHz to 1.2MHz with a single resistor, allows the use of ultra-small inductors and ceramic capacitors. The step-up regulatorâ€™s soft-start time is controlled by an internal 10ms digital timer that requires no external components; or if desired, the soft-start time can be adjusted by adding a single external capacitor. The low-voltage LDO linear regulator can provide at least 250mA. The output voltage is accurate within ±2%. The high-voltage, level-shifting scan driver is designed to work with panels that incorporate row drivers on the panel glass. Its seven outputs swing from +30V to -10V and can swiftly drive capacitive loads. The high-performance op amp is designed to drive the LCD backplane and features 20MHz bandwidth, 45V/µs slew rate, and 150mA output currents. The programmable VCOM calibrator is externally attached to the VCOM amplifierâ€™s resistive voltage-divider and sinks a programmable current to adjust the VCOM voltage level. An internal 7-bit digital-to-analog converter (DAC) controls the sink current. The DAC is ratiometric relative to AVDD and is guaranteed monotonic over all operating conditions. The calibrator includes a nonvolatile memory device (IVR) to store the desired VCOM voltage level. The 2-wire I2C interface simplifies production equipment. The MAX17094 is available in a 48-pin, 6mm x 6mm TQFN package with a maximum thickness of 0.8mm for thin LCD panels.

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II. Manufacturing Information

A. Description/Function:	Internal-Switch Boost Regulator with Integrated 7-Channel Driver, VCOM Calibrator, Op Amp, and LDO
B. Process:	S45
C. Number of Device Transistors:	21007
D. Fabrication Location:	Texas
E. Assembly Location:	NSEB Thailand
F. Date of Initial Production:	October 23, 2008

III. Packaging Information

A. Package Type:	48-pin TQFN 6x6
B. Lead Frame:	
C. Lead Finish:	100% matte Tin
D. Die Attach:	Nonconductive Epoxy
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	38°C/W
K. Single Layer Theta Jc:	1.4°C/W
L. Multi Layer Theta Ja:	27°C/W
M. Multi Layer Theta Jc:	1.4°C/W

IV. Die Information

A. Dimensions:	116 X 88 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide
C. Interconnect:	Aluminum/0.5% Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.4 \times 10^{-9}$

$\lambda = 22.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S45 Process results in a FIT Rate of 2.33 @ 25C and 28.16 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The PF37 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000 per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA, 1.5x VCCMax Overvoltage per JESD78.

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Table 1
Reliability Evaluation Test Results

MAX17094ETM+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

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