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UC1834  
UC2834  
UC3834

## High Efficiency Linear Regulator

## FEATURES

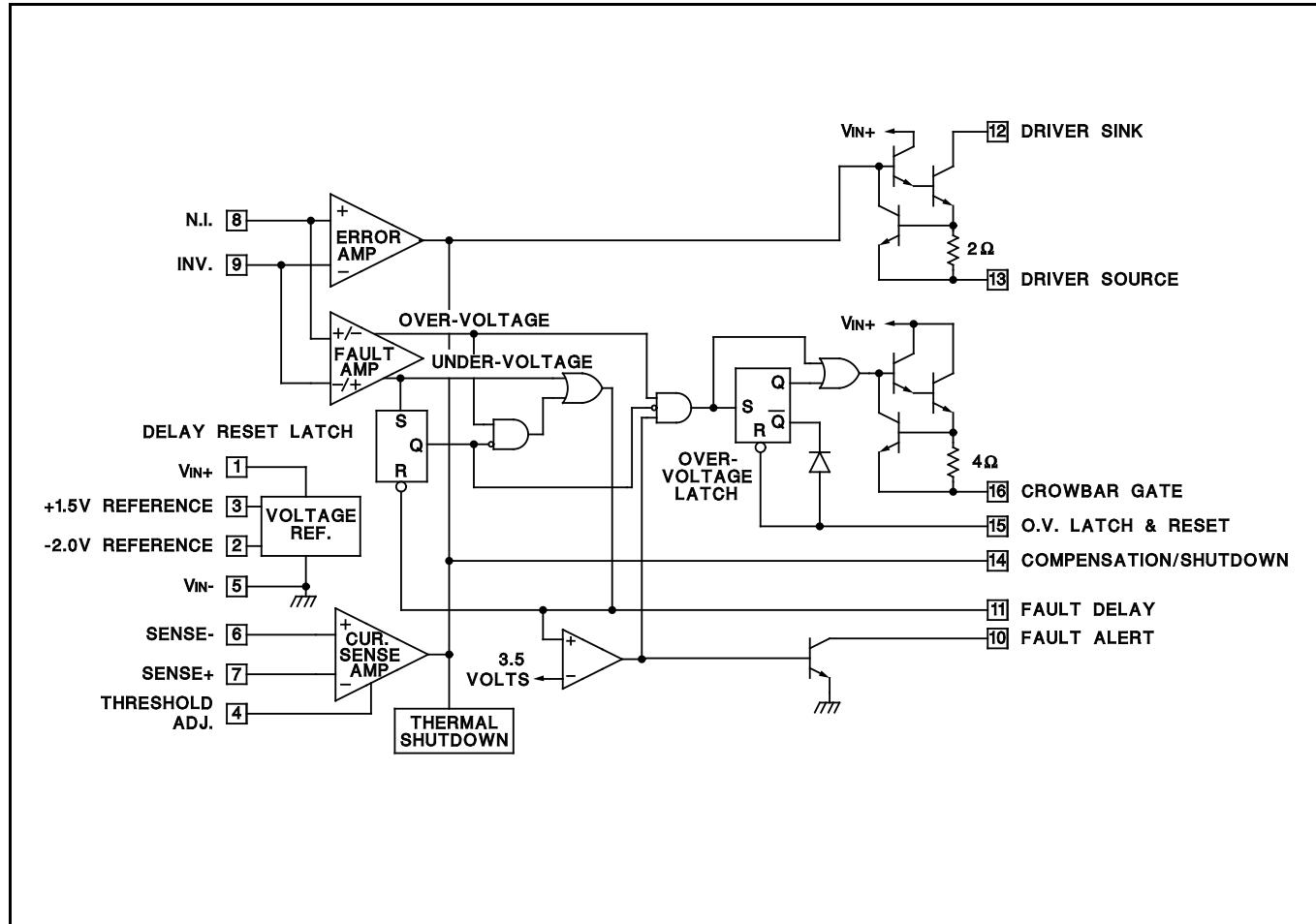
- Minimum VIN - VOUT Less Than 0.5V At 5A Load With External Pass Device
- Equally Usable For Either Positive or Negative Regulator Design
- Adjustable Low Threshold Current Sense Amplifier
- Under And Over-Voltage Fault Alert With Programmable Delay
- Over-Voltage Fault Latch With 100mA Crowbar Drive Output

## DESCRIPTION

The UC1834 family of integrated circuits is optimized for the design of low input-output differential linear regulators. A high gain amplifier and 200mA sink or source drive outputs facilitate high output current designs which use an external pass device. With both positive and negative precision references, either polarity of regulator can be implemented. A current sense amplifier with a low, adjustable, threshold can be used to sense and limit currents in either the positive or negative supply lines.

In addition, this series of parts has a fault monitoring circuit which senses both under and over-voltage fault conditions. After a user defined delay for transient rejection, this circuitry provides a fault alert output for either fault condition. In the over-voltage case, a 100mA crowbar output is activated. An over-voltage latch will maintain the crowbar output and can be used to shutdown the driver outputs. System control to the device can be accommodated at a single input which will act as both a supply reset and remote shutdown terminal. These die are protected against excessive power dissipation by an internal thermal shutdown function.

## BLOCK DIAGRAM



**UC1834**  
**UC2834**  
**UC3834**

### ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage, $V_{IN+}$ .....	40V
Driver Current .....	400mA
Driver Source to Sink Voltage .....	40V
Crowbar Current .....	-200mA
+1.5V Reference Output Current .....	-10mA
Fault Alert Voltage .....	40V
Fault Alert Current .....	15mA
Error Amplifier Inputs .....	-0.5V to 35V
Current Sense Inputs .....	-0.5V to 40V
O.V. Latch Output Voltage .....	-0.5V to 40V
O.V. Latch Output Current .....	15mA

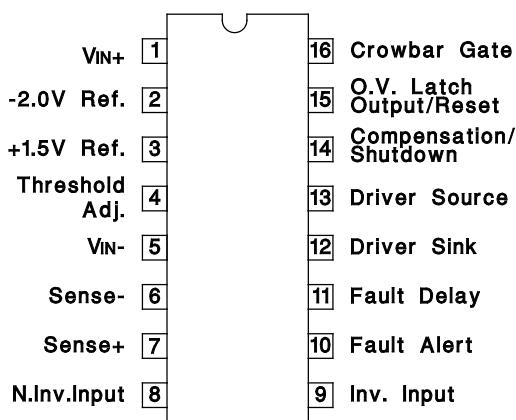
Power Dissipation at $T_A = 25^\circ C$ .....	1000mW
Power Dissipation at $T_C = 25^\circ C$ .....	2000mW
Operating Junction Temperature .....	-55°C to +150°C
Storage Temperature .....	-65°C to +150°C
Lead Temperature (soldering, 10 seconds) .....	300°C

*Note 1: Voltages are reference to  $V_{IN-}$ , Pin 5.*  
*Currents are positive into, negative out of the specified terminals.*

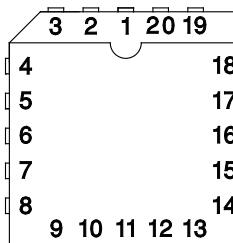
*Consult Packaging section of Databook for thermal limitations and considerations of package.*

### CONNECTION DIAGRAMS

**DIL-16, SOIC-16 (TOP VIEW)**  
 J or N Package, DW Package



**PLCC-20, LCC-20 (TOP VIEW)**  
 Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
$V_{IN+}$	2
-2.0V REF	3
+1.5V REF	4
Threshold Adjust	5
N/C	6
$V_{IN-}$	7
Sense-	8
Sense+	9
N.Inv. Input	10
N/C	11
Inv. Input	12
Fault Alert	13
Fault Delay	14
Driver Sink	15
N/C	16
Driver Source	17
Compensation/ Shutdown	18
O.V. Latch Output/Reset	19
Crowbar Gate	20

**UC1834**  
**UC2834**  
**UC3834**

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1834,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2834, and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3834.  $V_{IN+} = 15\text{V}$ ,  $V_{IN-} = 0\text{V}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	UC1834			UC3834			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Turn-on Characteristics</b>								
Standby Supply Current			5.5	7		5.5	10	mA
<b>+1.5 Volt Reference</b>								
Output Voltage	$T_J = 25^\circ\text{C}$	1.485	1.5	1.515	1.47	1.5	1.53	V
	$T_J(\text{MIN}) \leq T_J \leq T_J(\text{MAX})$	1.47		1.53	1.455		1.545	
Line Regulation	$V_{IN+} = 5$ to $35\text{V}$		1	10		1	15	mV
Load Regulation	$I_{OUT} = 0$ to $2\text{mA}$		1	10		1	15	mV
<b>-2.0 Volt Reference (Note 2)</b>								
Output Voltage (Referenced to $V_{IN^+}$ )	$T_J = 25^\circ\text{C}$	-2.04	-2	-1.96	-2.06	-2	-1.94	V
	$T_J(\text{MIN}) \leq T_J \leq T_J(\text{MAX})$	-2.06		-1.94	-2.08		-1.92	
Line Regulation	$V_{IN+} = 5$ to $35\text{V}$		1.5	15		1.5	20	mV
Output Impedance			2.3			2.3		$\text{k}\Omega$
<b>Error Amplifier Section</b>								
Input Offset Voltage	$V_{CM} = 1.5\text{V}$		1	6		1	10	mV
Input Bias Current	$V_{CM} = 1.5\text{V}$		-1	-4		-1	-8	$\mu\text{A}$
Input Offset Current	$V_{CM} = 1.5\text{V}$		0.1	1		0.1	2	$\mu\text{A}$
Small Signal Open Loop Gain	Output @ Pin 14, Pin 12 = $V_{IN+}$ Pin 13, $20\Omega$ to $V_{IN-}$	50	65		50	65		dB
CMRR	$V_{CM} = 0.5$ to $33\text{V}$ , $V_{IN+} = 35\text{V}$	60	80		60	80		dB
PSRR	$V_{IN+} = 5$ to $35\text{V}$ , $V_{CM} = 1.5\text{V}$	70	100		70	100		dB
<b>Driver Section</b>								
Maximum Output Current		200	350		200	350		mA
Saturation Voltage	$I_{OUT} = 100\text{mA}$		0.5	1.2		0.5	1.5	V
Output Leakage Current	Pin 12 = $35\text{V}$ , Pin 13 = $V_{IN-}$ , Pin 14 = $V_{IN+}$		0.1	50		0.1	50	$\mu\text{A}$
Shutdown Input Voltage at Pin 14	$I_{OUT} \leq 100\mu\text{A}$ , Pin 13 = $V_{IN-}$ , Pin 12 = $V_{IN+}$	0.4	1		0.4	1		V
Shutdown Input Current at Pin 14	Pin 14 = $V_{IN-}$ , Pin 12 = $V_{IN+}$ $I_{OUT} \leq 100\mu\text{A}$ , Pin 13 = $V_{IN-}$		-100	-150		-100	-150	$\mu\text{A}$
Thermal Shutdown (Note 3)			165			165		$^\circ\text{C}$
<b>Fault Amplifier Section</b>								
Under- and Over-Voltage Fault Threshold	$V_{CM} = 1.5\text{V}$ , @ E/A Inputs	120	150	180	110	150	190	mV
Common Mode Sensitivity	$V_{IN+} = 35\text{V}$ , $V_{CM} = 1.5$ to $33\text{V}$		-0.4	-0.8		-0.4	-1.0	%/v
Supply Sensitivity	$V_{CM} = 1.5\text{V}$ , $V_{IN+} = 5$ to $35\text{V}$		-0.5	-1.0		-0.5	-1.2	%/V
Fault Delay		30	45	60	30	45	60	$\text{ms}/\mu\text{F}$
Fault Alert Output Current		2	5		2	5		mA
Fault Alert Saturation Voltage	$I_{OUT} = 1\text{mA}$		0.2	0.5		0.2	0.5	V
O.V. Latch Output Current		2	4		2	4		mA
O.V. Latch Saturation Voltage	$I_{OUT} = 1\text{mA}$		1.0	1.3		1.0	1.3	V
O.V. Latch Output Reset Voltage		0.3	0.4	0.6	0.3	0.4	0.6	V
Crowbar Gate Current		-100	-175		-100	-175		mA
Crowbar Gate Leakage Current	$V_{IN+} = 35\text{V}$ , Pin 16 = $V_{IN-}$		-0.5	-50		-0.5	-50	$\mu\text{A}$

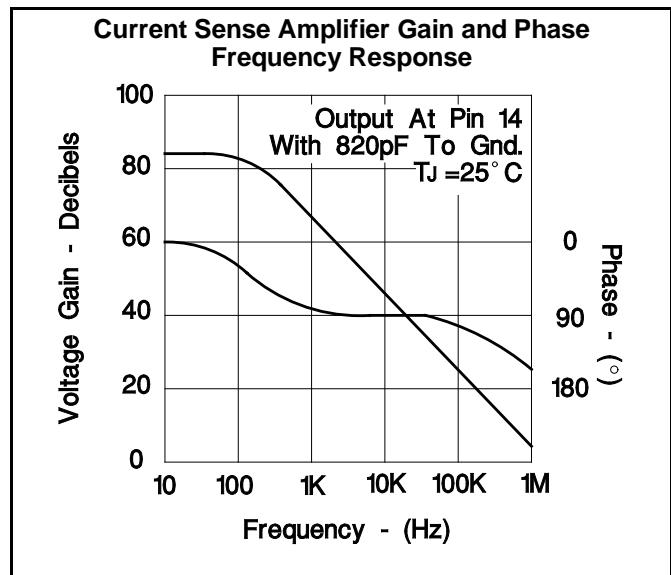
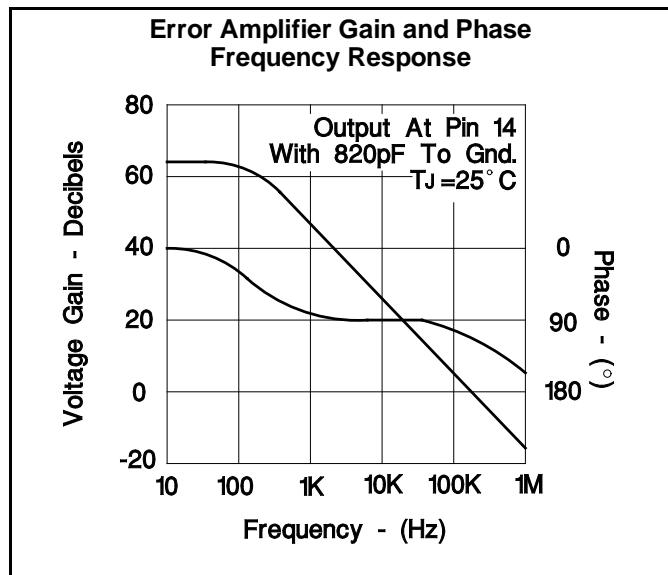
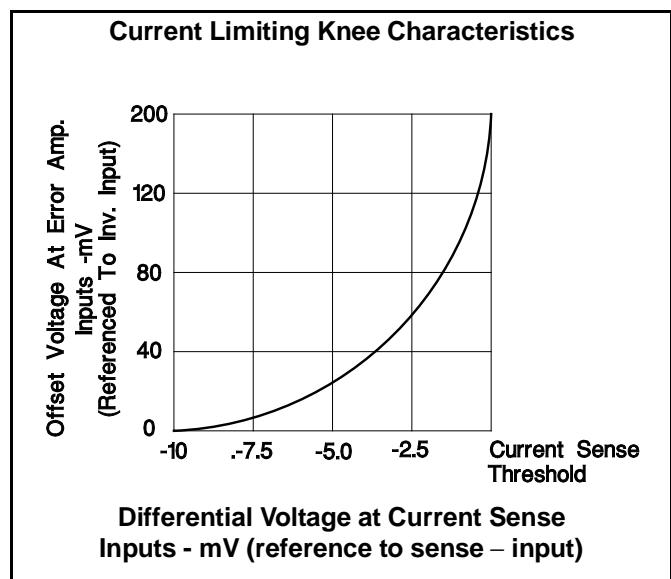
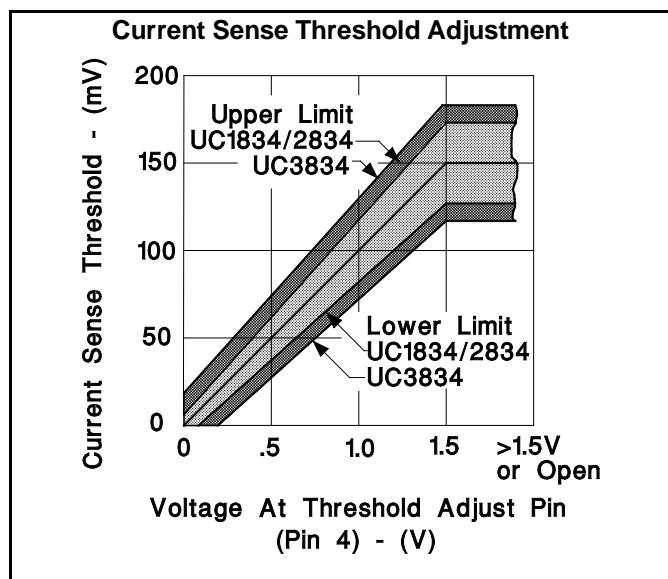
Note 2: When using both the 1.5V and -2.0V references the current out of pin 3 should be balanced by an equivalent current into Pin 2. The -2.0V output will change -2.3mV per  $\mu\text{A}$  of imbalance.

Note 3: Thermal shutdown turns off the driver. If Pin 15 (O.V. Latch Output) is tied to Pin 14 (Compensation/Shutdown) the O.V. Latch will be reset.

**UC1834**  
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**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1834,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2834, and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3834.  $V_{IN+} = 15\text{V}$ ,  $V_{IN-} = 0\text{V}$ .  $T_A = T_J$

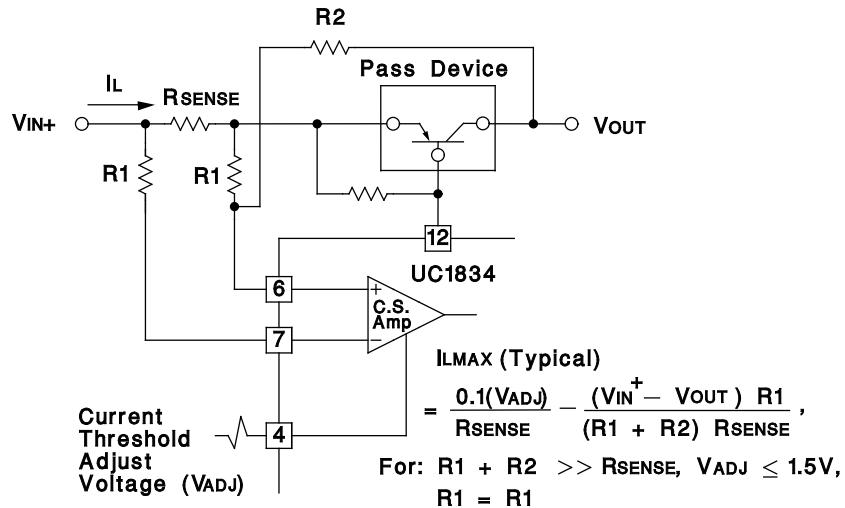
PARAMETER	TEST CONDITIONS	UC1834 UC2834			UC3834			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Current Sense Amplifier Section</b>								
Threshold Voltage	Pin 4 Open, $V_{CM} = V_{IN+}$ or $V_{IN-}$	130	150	170	120	150	180	mV
	Pin 4 = 0.5V, $V_{CM} = V_{IN+}$ or $V_{IN-}$	40	50	60	30	50	70	
Threshold Supply Sensitivity	Pin 4 Open, $V_{CM} = V_{IN-}$ , $V_{IN+} = 5$ to $35\text{V}$		-0.1	-0.3		-0.1	-0.5	%/V
Adj. Input Current	Pin 4 = 0.5V		-2	-10		-2	-10	$\mu\text{A}$
Sense Input Bias Current	$V_{CM} = V_{IN+}$		100	200		100	200	$\mu\text{A}$
	$V_{CM} = V_{IN-}$		-100	-200		-100	-200	



UC1834  
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UC3834

## APPLICATION INFORMATION

### Foldback Current Limiting



Both the current sense and error amplifiers on the UC1834 are transconductance type amplifiers. As a result, their voltage gain is a direct function of the load impedance at their shared output pin, Pin 14. Their small signal voltage gain as a function of load and frequency is nominally given by;

$$Av \text{ E/A} = \frac{Z_L(f)}{700\Omega} \text{ and } Av \text{ c. s./A} = \frac{Z_L(f)}{70\Omega}$$

for:  $f \leq 500\text{kHz}$  and  $|Z_L(f)| \leq 1 \text{ M}\Omega$

Where:

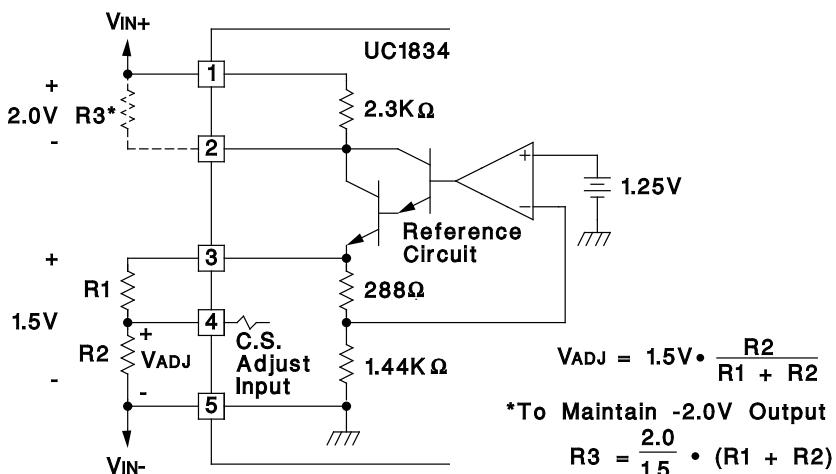
Av=Small Signal Voltage Gain to pin 14.

$Z_L(f)$  = Load Impedance at Pin 14.

The UC1834 fault delay circuitry prevents the fault outputs from responding to transient fault conditions. The delay reset latch insures that the full, user defined, delay passes before an over-voltage fault response occurs. This prevents unnecessary crowbar, or latched-off conditions, from occurring following sharp under-voltage to over-voltage transients.

The crowbar output on the UC1834 is activated following a sustained over-voltage condition. The crowbar output remains high as long as the fault condition persists, or, as long as the over-voltage latch is set. The latch is set with an over-voltage fault if the voltage at Pin 15 is above the latch reset threshold, typically 0.4V. When the latch is set, its Q- output will pull Pin 15 low through a series diode. As long as a nominal pull-up load exists, the series diode prevents Q- from pulling Pin 15 below the reset threshold. However, Pin 15 is pulled low enough to disable the driver outputs if Pins 15 and 14 are tied together. With Pin 15 and 14 common, the regulator will latch off in response to an over-voltage fault. If the fault condition is cleared and Pins 14 and 15 are momentarily pulled below the latch reset threshold, the driver outputs are re-enabled.

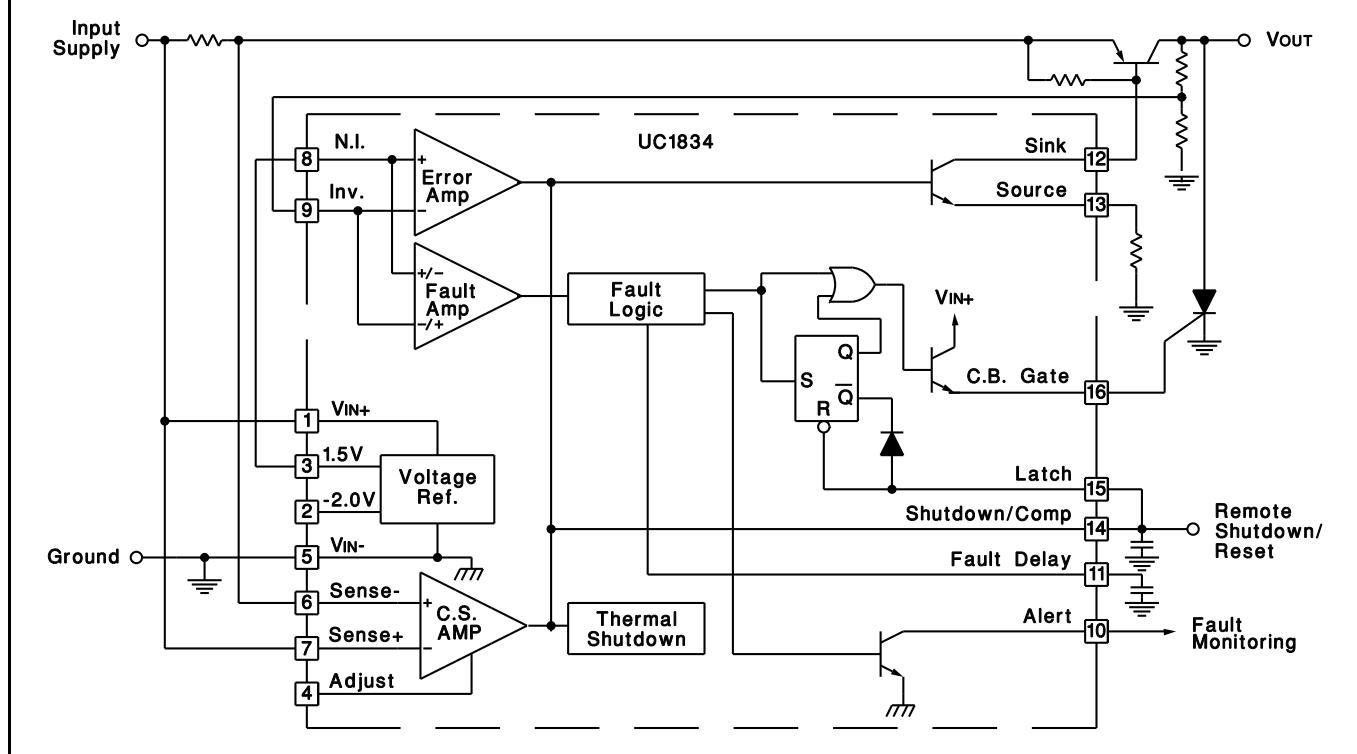
### Setting the Threshold Adjust Voltage (VADJ)



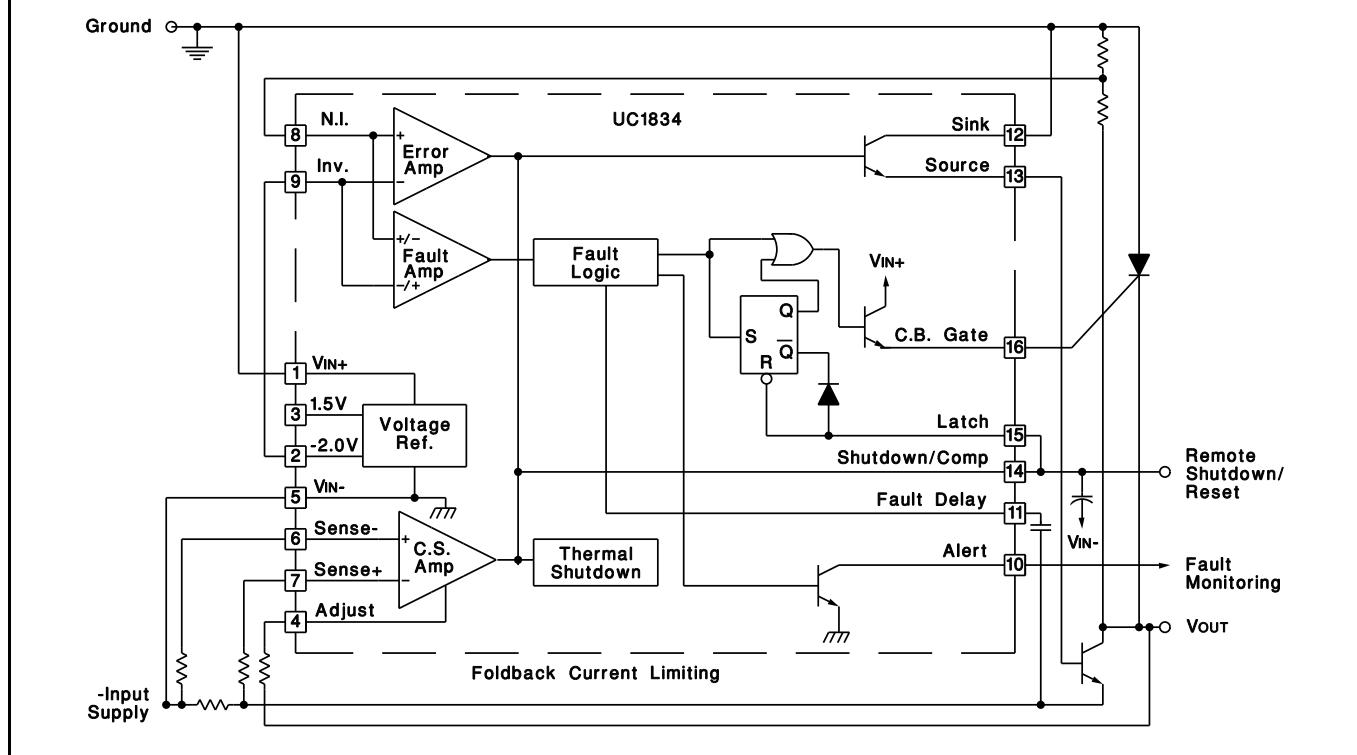
UC1834  
UC2834  
UC3834

## **TYPICAL APPLICATIONS**

## 5-10 Amp Positive Regulator



## 5-10 Amp Negative Regulator



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87742012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87742012A UC1834L/ 883B	<b>Samples</b>
5962-8774201EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8774201EA UC1834J/883B	<b>Samples</b>
5962-8774201V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type		5962-8774201V2A UC1834L QMLV	<b>Samples</b>
5962-8774201VEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type		5962-8774201VE A UC1834JQMLV	<b>Samples</b>
UC1834J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1834J	<b>Samples</b>
UC1834J/81025	OBsolete	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
UC1834J883B	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8774201EA UC1834J/883B	<b>Samples</b>
UC1834L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1834L	<b>Samples</b>
UC1834L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87742012A UC1834L/ 883B	<b>Samples</b>
UC2834DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2834DW	<b>Samples</b>
UC2834DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2834DW	<b>Samples</b>
UC2834DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2834DW	<b>Samples</b>
UC2834DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2834DW	<b>Samples</b>
UC2834J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-40 to 85	UC2834J	<b>Samples</b>
UC2834Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	UC2834Q	<b>Samples</b>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2834QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	UC2834Q	<span style="background-color: red; color: white;">Samples</span>
UC2834QTR	OBsolete	PLCC	FN	20		TBD	Call TI	Call TI	-40 to 85	UC2834Q	
UC3834DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3834DW	<span style="background-color: red; color: white;">Samples</span>
UC3834DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3834DW	<span style="background-color: red; color: white;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF UC1834, UC1834-SP, UC2834, UC2834M, UC3834 :**

• Catalog: [UC3834](#), [UC1834](#), [UC2834](#)

• Military: [UC2834M](#), [UC1834](#)

• Space: [UC1834-SP](#)

**NOTE: Qualified Version Definitions:**

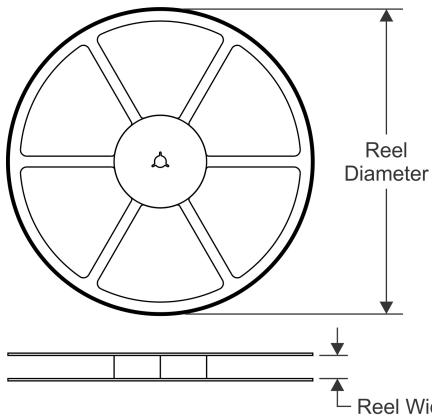
• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

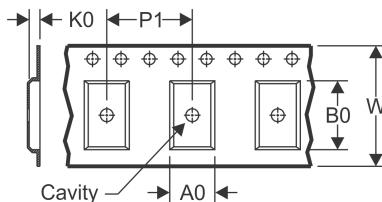
• Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**

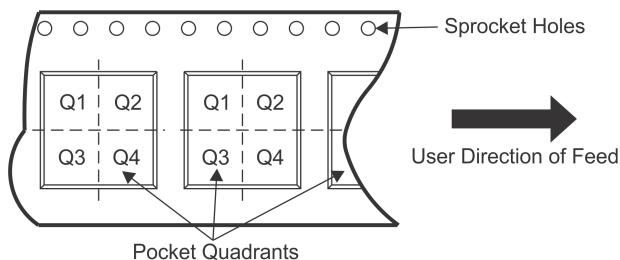


**TAPE DIMENSIONS**



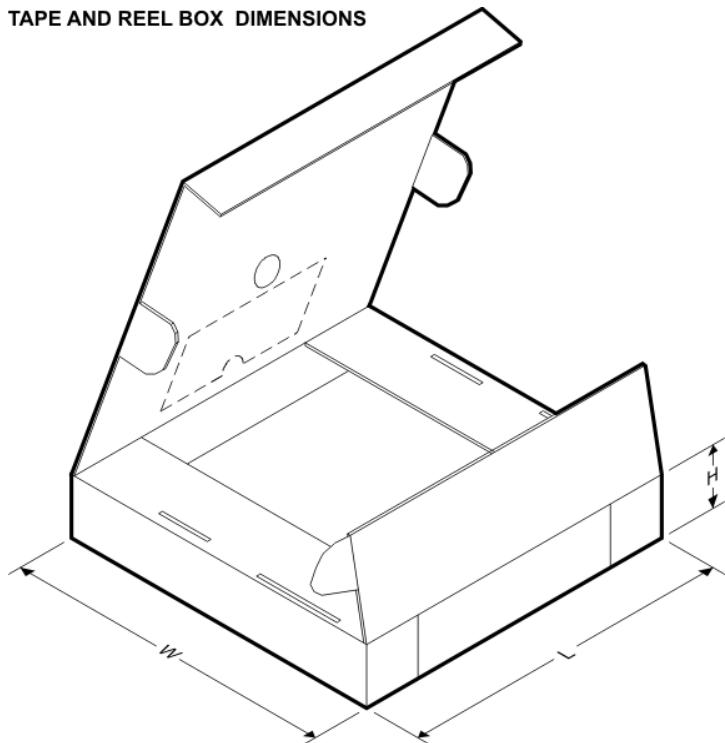
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2834DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2834DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

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