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Skyworks Solutions Inc.
SKY12332-310LF

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**SKYWORKS®**

DATA SHEET

# SKY12332-310LF: 6-Bit Digital Attenuator with Driver LF–1 GHz, 0.5 dB LSB, 31.5 dB Range

## Features

- Attenuation range: 31.5 dB
- LSB: 0.5 dB
- On-board low noise CMOS driver
- Excellent RF noise floor
- Single 5 V supply
- Very low DC power consumption
- Single positive control for each bit
- Small 5 x 5 mm QFN-32 package
- Lead (Pb)-free and RoHS-compliant MSL-1 @ 260 °C per JEDEC J-STD-020

## Description

The Skyworks SKY12332-310LF is 6-bit digital GaAs attenuator with an on-board low-noise CMOS driver. This attenuator offers excellent performance from low frequency through 1 GHz, making it ideal for IF and RF level control applications. It contains an on-board CMOS driver circuit which accepts CMOS logic levels at the 6 control inputs and produces a negative supply voltage to control the GaAs attenuator.

The SKY12332-310LF has excellent linearity for compatibility with non-constant envelope signals, such as W-CDMA and OFDM. The 6 attenuation bits are binary weighted, with an LSB of 0.5 dB and a total nominal attenuation range of 31.5 dB. It also has excellent attenuation accuracy and is monotonic. The low-noise CMOS driver enables a very low RF noise floor, typically -100 dBm.

Typical applications for this attenuator include level control in cellular base stations, wireless data transceivers, broadband systems, etc.

The required supply voltage for SKY12332-310LF is 5V. This part can operate over the temperature range of -40 °C to 85 °C.
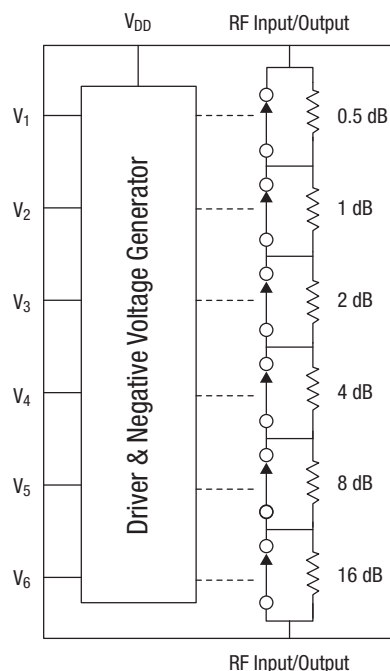
An evaluation board is available upon request.

NEW ▶ Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.
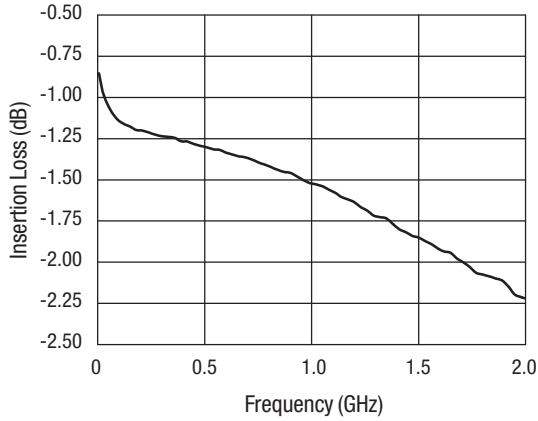
## Functional Block Diagram

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## Electrical Specifications

**$V_{DD}$ = 5 V, T = 25 °C, $Z_0$ = 50 $\Omega$, unless otherwise noted**

| Parameter | Symbol | Condition | Frequency | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Insertion loss | IL | | LF–500 MHz | | 1.5 | 1.8 | dB |
| | | | LF–1.0 GHz | | 1.8 | 2.2 | dB |
| Attenuation range | | | | | 31.5 | | dB |
| Attenuation accuracy | | Attenuation referred to insertion loss | LF–500 MHz | ± (0.20 + 2% of attenuation setting in dB) | | | dB |
| | | | LF–1.0 GHz | ± (0.25 + 3% of attenuation setting in dB) | | | dB |
| RF input/RF output VSWR | | Non-driven port terminated in $Z_0$ | LF–1.0 GHz | | 1.4:1 | 1.6:1 | |
| Control voltage | $V_{CTL}$ | $V_{CTL} = V_{LOW}$ | | 0 | | 0.8 | V |
| | | $V_{CTL} = V_{HIGH}$ | | 2.7 | | $V_{DD}$ | V |
| Control port current | $I_{CTL}$ | $V_{CTL} = V_{LOW}$ | | | 20 | | µA |
| | | $V_{CTL} = V_{HIGH}$ | | | 20 | | µA |
| Switching characteristics Rise, fall time On, off time Video feedthrough | $t_r$, $t_f$ $t_{on}$, $t_{off}$ | 10%/90% or 90%/10% of RF 50% $V_{CTL}$ to 90%/10% of RF $T_{RISE}$ = 1 ns, BW = 500 MHz | | | 30 50 50 | | ns ns mV |
| Input power for 1 dB compression | $IP_{1\,dB}$ | | 50 MHz | | 22 | | dBm |
| | | | 500 MHz–1.0 GHz | | 29 | | dBm |
| Input third order intermodulation intercept point | IIP3 | 2 input tones, 5 dBm each tone | 50 MHz | | 36 | | dBm |
| | | | 500 MHz–1.0 GHz | | 48 | | dBm |
| DC supply voltage | $V_{DD}$ | | | 4.75 | 5 | 5.25 | V |
| DC supply current | $I_{DD}$ | | | | 700 | | µA |

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## Typical Performance Data

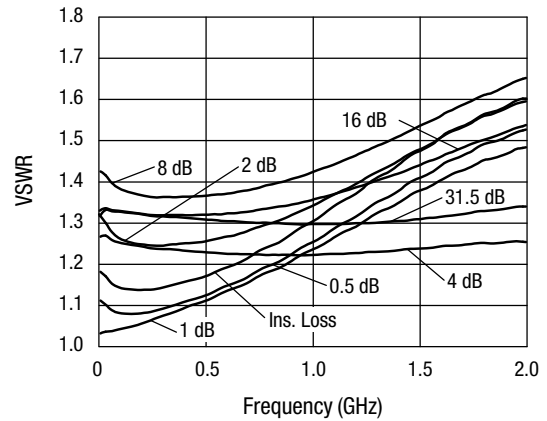$V_{DD}$ = 5 V, T = 25 °C, $Z_0$ = 50 $\Omega$, unless otherwise noted

**Insertion Loss vs. Frequency**
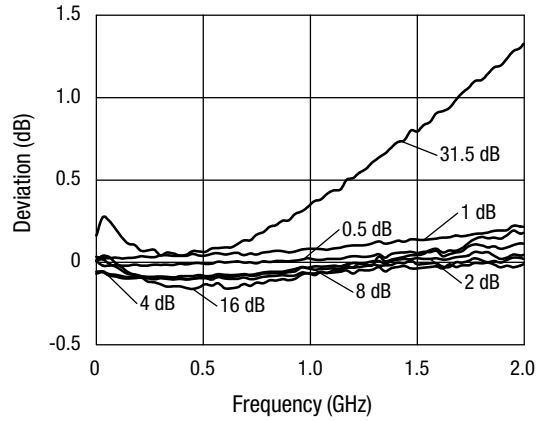
**Attenuation Accuracy vs. Frequency**
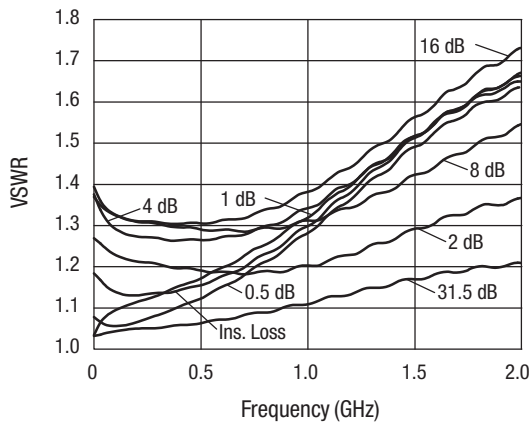
**Input VSWR vs. Frequency**

**Output VSWR vs. Frequency**

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## Absolute Maximum Ratings

| Characteristic | Value |
|---|---|
| RF input power | 2 W for f > 500 MHz<br>0.5 W for 50 MHz $\leq$ f $\leq$ 500 MHz |
| Supply voltage | 6 V |
| Supply current | 2 mA |
| Operating temperature | -40 °C to +85 °C |
| Storage temperature | -65 °C to +150 °C |

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

*CAUTION: Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.*

## Truth Table

| $V_6$ | $V_5$ | $V_4$ | $V_3$ | $V_2$ | $V_1$ | Attenuation |
|---|---|---|---|---|---|---|
| 16 dB | 8 dB | 4 dB | 2 dB | 1 dB | 0.5 dB | $J_1$–$J_2$ |
| 0 | 0 | 0 | 0 | 0 | 0 | Ins. loss |
| 0 | 0 | 0 | 0 | 0 | 1 | 0.5 dB |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 dB |
| 0 | 0 | 0 | 1 | 0 | 0 | 2 dB |
| 0 | 0 | 1 | 0 | 0 | 0 | 4 dB |
| 0 | 1 | 0 | 0 | 0 | 0 | 8 dB |
| 1 | 0 | 0 | 0 | 0 | 0 | 16 dB |
| 1 | 1 | 1 | 1 | 1 | 1 | 31.5 dB |

"0" = $V_{LOW}$
"1" = $V_{HIGH}$

## Pin Out
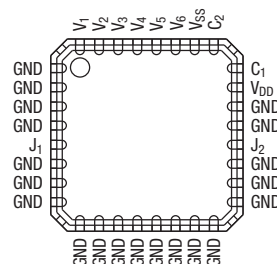


## Pin Description

| Pin | Symbol | Function |
|---|---|---|
| 1–4, 6–19, 21–22 | GND | Connect to system ground via lowest possible impedance |
| 5 | $J_1$ | RF input/output |
| 20 | $J_2$ | RF output/input |
| 23 | $V_{DD}$ | Positive supply voltage input. Bypass this pin to ground via a 10 nF or larger capacitor |
| 24, 25 | $C_1$, $C_2$ | Connect charge pump capacitor, 25 nF typical, between these pins |
| 26 | $V_{SS}$ | Negative supply voltage filter capacitor. Bypass this pin to ground via a 10 nF or larger capacitor. |
| 27 | $V_6$ | Control voltage input for 16 dB bit, MSB |
| 28 | $V_5$ | Control voltage input for 8 dB bit |
| 29 | $V_4$ | Control voltage input for 4 dB bit |
| 30 | $V_3$ | Control voltage input for 2 dB bit |
| 31 | $V_2$ | Control voltage input for 1 dB bit |
| 32 | $V_1$ | Control voltage input for 0.5 dB bit, LSB |
| Paddle | | Connect to system ground via lowest possible electrical and thermal impedance |

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## Circuit Description

The SKY12332-301LF is comprised of a Si CMOS die and a GaAs digital attenuator die, packaged in a 5 x 5 mm, 32-pin QFN surface mount package.

The CMOS die performs the following functions: it contains a charge pump circuit that generates a negative voltage, $V_{SS}$, from the positive supply voltage, $V_{DD}$; it decodes the 6-bit control word applied to ports $V_1$ through $V_6$; and, it drives the corresponding switching FETs on the GaAs attenuator die. This circuit was optimized to produce the lowest possible noise in the RF signal path.

The GaAs attenuator die is comprised of 6 resistive, fixed attenuator sections with nominal input and output impedance of 50 Ω.  The attenuation of these sections is binary weighted, ranging from 0.5 dB nominal up to 16 dB nominal. These attenuator sections are either switched into or out of the main signal path, between ports $J_1$ and $J_2$, according to the 6-bit control word applied to ports $V_1$ through $V_6$. This die is also utilized in AA113-310.

The switching is performed by depletion mode MESFETs on the attenuator die. The charge pump circuit on the CMOS die generates the negative voltage $V_{SS}$, nominally -3.75 V, required to enable reverse bias of the gate-source of the MESFETs that must be switched to high drain-source impedance to properly select or bypass the fixed resistive attenuator sections.

## Recommended Solder Reflow Profiles

Refer to the *"Recommended Solder Reflow Profile"* Application Note.

## Tape and Reel Information

Refer to the *"Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation"* Application Note.

## Suggested Circuit
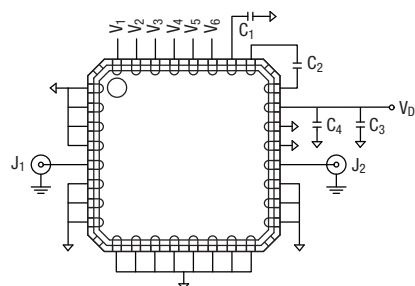


| Component | Suggested Value |
|---|---|
| $C_1$, $C_3$ | 0.01 µF |
| $C_2$ | 0.025 µF |
| $C_4$ | 100 pF |

## QFN 5 x 5 (-310)

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