

## **Excellent Integrated System Limited**

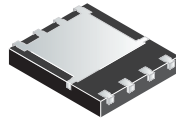
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[CSD16321Q5](#)

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**CSD16321Q5**

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SLPS220B – AUGUST 2009 – REVISED MAY 2010

## N-Channel NexFET™ Power MOSFET

Check for Samples: [CSD16321Q5](#)

### FEATURES

- Optimized for 5V Gate Drive
- Ultra Low Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- SON 5mm x 6mm Plastic Package

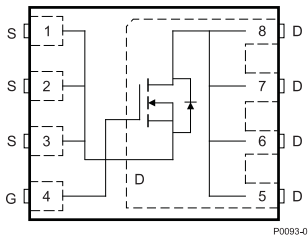
### APPLICATIONS

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Synchronous FET Applications

### DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

Top View



### PRODUCT SUMMARY

$V_{DS}$	Drain to Source Voltage	25	V
$Q_g$	Gate Charge Total (4.5V)	14	nC
$Q_{gd}$	Gate Charge Gate to Drain	2.5	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V$	2.8 mΩ
		$V_{GS} = 4.5V$	2.1 mΩ
		$V_{GS} = 8V$	1.9 mΩ
$V_{GS(th)}$	Threshold Voltage	1.1	V

### ORDERING INFORMATION

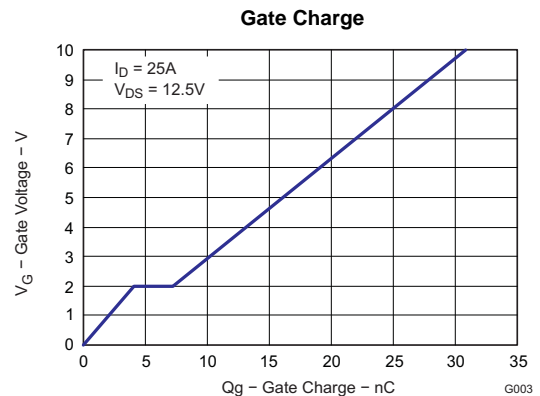
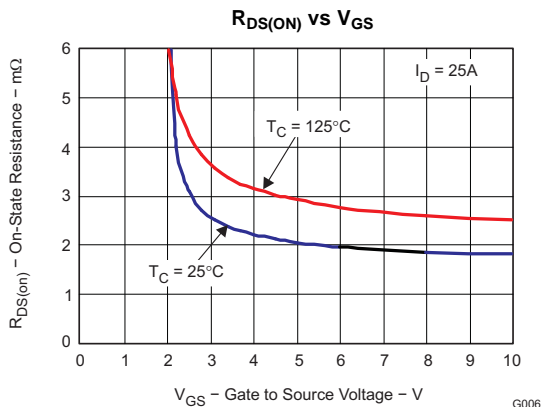
Device	Package	Media	Qty	Ship
CSD16321Q5	SON 5 x 6 Plastic Package	13-inch reel	2500	Tape and Reel

### ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage	+10 / -8	V
$I_D$	Continuous Drain Current, $T_C = 25^\circ\text{C}$	100	A
	Continuous Drain Current(1)	31	A
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ (2)	200	A
$P_D$	Power Dissipation(1)	3.1	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, single pulse $I_D = 66\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	218	mJ

(1) Typical  $R_{\theta JA} = 39^\circ\text{C/W}$  on 1in<sup>2</sup> Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$



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**CSD16321Q5**

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**ELECTRICAL CHARACTERISTICS**

 ( $T_A = 25^\circ\text{C}$  unless otherwise stated)

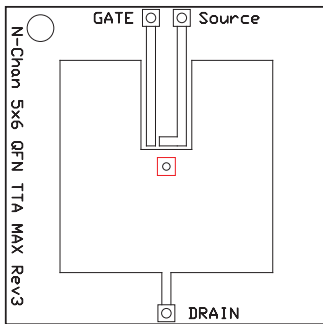
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	25			V
$I_{DSS}$	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 20V$			1	$\mu A$
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +10 / -8V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.9	1.1	1.4	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V, I_D = 25A$		2.8	3.8	m $\Omega$
		$V_{GS} = 4.5V, I_D = 25A$		2.1	2.6	m $\Omega$
		$V_{GS} = 8V, I_D = 25A$		1.9	2.4	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 12.5V, I_D = 25A$		150		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance			2360	3100	pF
$C_{oss}$	Output Capacitance	$V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz$		1700	2200	pF
$C_{rss}$	Reverse Transfer Capacitance			115	150	pF
$R_G$	Series Gate Resistance			1.5	3	$\Omega$
$Q_g$	Gate Charge Total (4.5V)			14	19	nC
$Q_{gd}$	Gate Charge Gate to Drain	$V_{DS} = 12.5V, I_D = 25A$		2.5		nC
$Q_{gs}$	Gate Charge Gate to Source			4		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			2.1		nC
$Q_{oss}$	Output Charge	$V_{DS} = 15V, V_{GS} = 0V$		36		nC
$t_{d(on)}$	Turn On Delay Time			9		ns
$t_r$	Rise Time	$V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 25A, R_G = 2\Omega$		15		ns
$t_{d(off)}$	Turn Off Delay Time			27		ns
$t_f$	Fall Time			17		ns
<b>Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage	$I_{SD} = 25A, V_{GS} = 0V$		0.8	1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 13V, I_F = 25A, di/dt = 300A/\mu s$		33		nC
$t_{rr}$	Reverse Recovery Time	$V_{DD} = 13V, I_F = 25A, di/dt = 300A/\mu s$		32		ns

**THERMAL CHARACTERISTICS**

 ( $T_A = 25^\circ\text{C}$  unless otherwise stated)

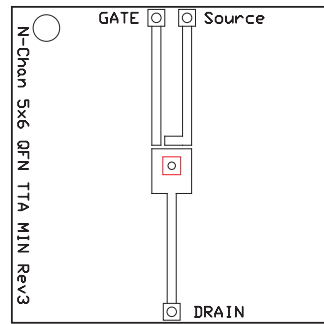
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case <sup>(1)</sup>			1.1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1) (2)</sup>			48	$^\circ\text{C/W}$

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1 inch square 2 oz. Cu pad on a 1.5 x 1.5 in .060 inch thick FR4 board.  $R_{\theta JC}$  is specified by design while  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 Material with 1 inch<sup>2</sup> of 2 oz. Cu.



M0137-01

Max  $R_{\theta JA} = 48^{\circ}\text{C/W}$   
when mounted on 1  
 $\text{inch}^2$  of 2 oz. Cu.

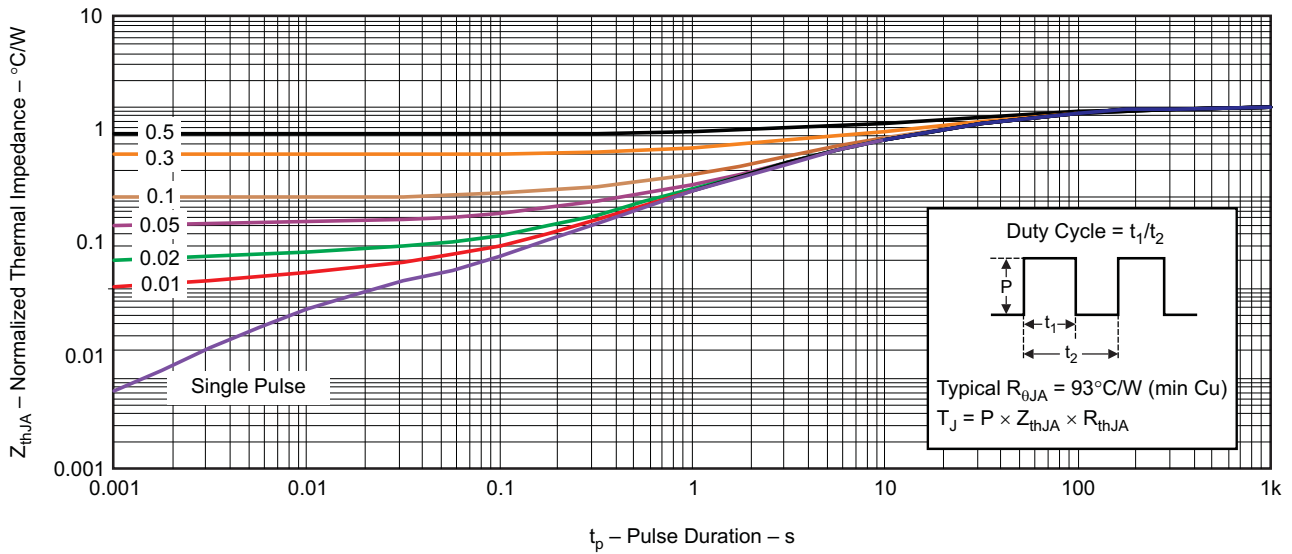


M0137-02

Max  $R_{\theta JA} = 115^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of 2  
oz. Cu.

**TYPICAL MOSFET CHARACTERISTICS**

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

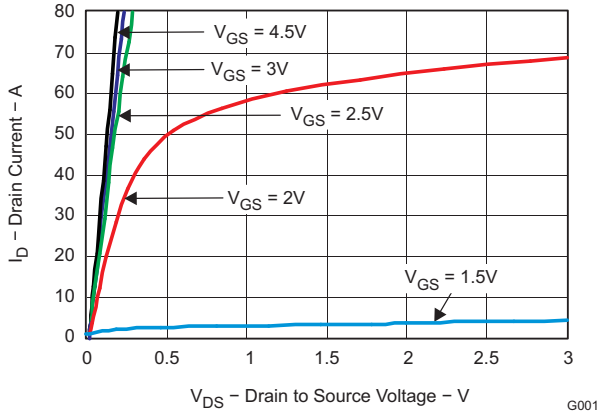


G012

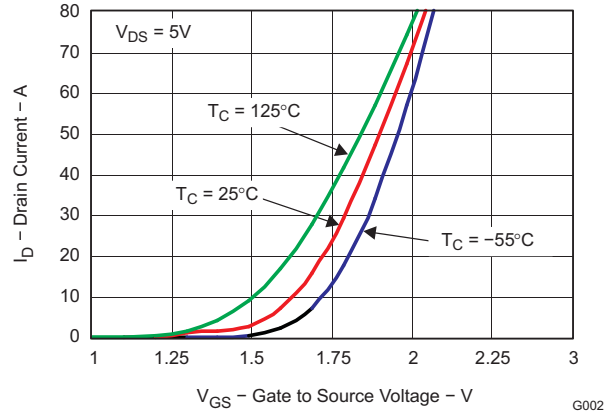
**Figure 1. Transient Thermal Impedance**

**TYPICAL MOSFET CHARACTERISTICS (continued)**

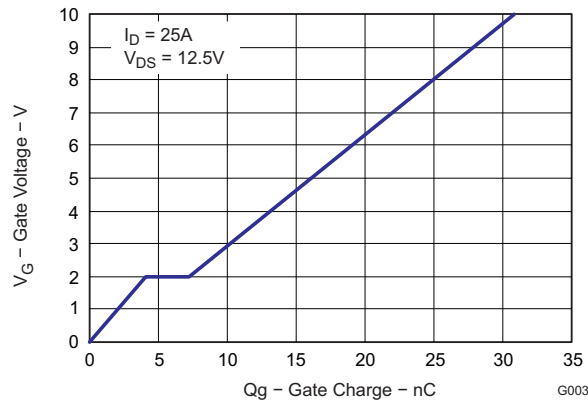
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



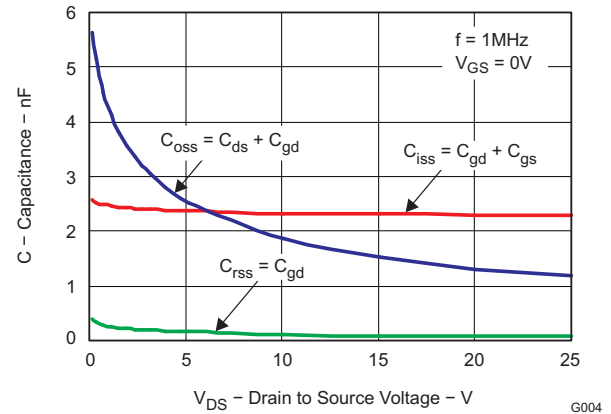
**Figure 2. Saturation Characteristics**



**Figure 3. Transfer Characteristics**



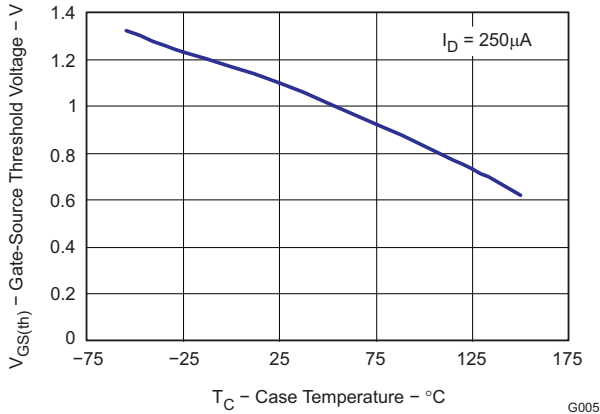
**Figure 4. Gate Charge**



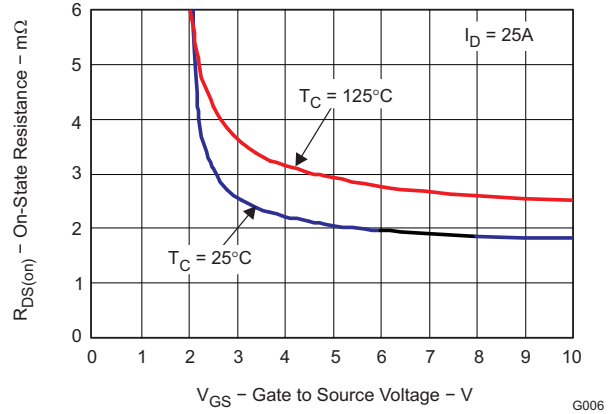
**Figure 5. Capacitance**

**TYPICAL MOSFET CHARACTERISTICS (continued)**

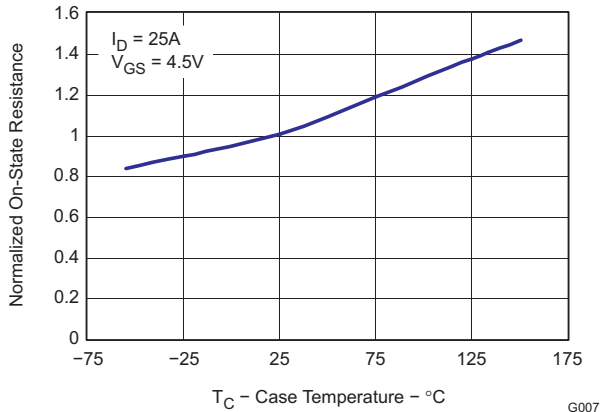
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



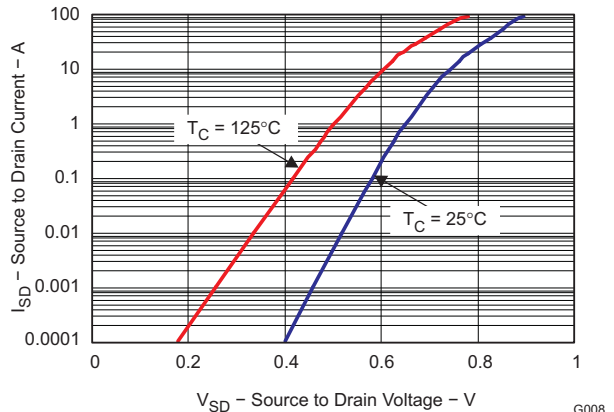
**Figure 6. Threshold Voltage vs. Temperature**



**Figure 7. On Resistance vs. Gate Voltage**



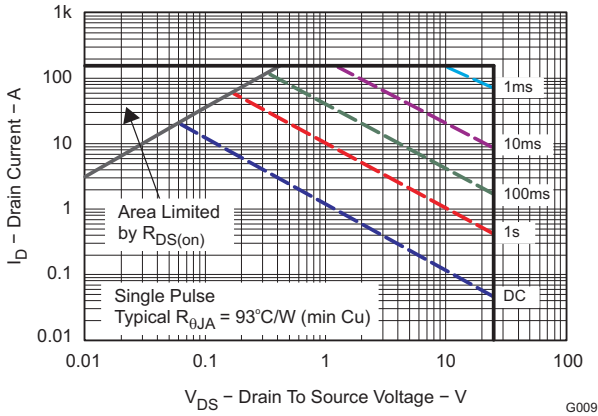
**Figure 8. On Resistance vs. Temperature**



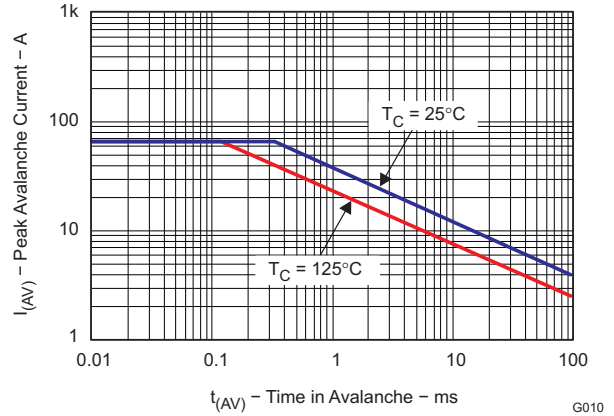
**Figure 9. Typical Diode Forward Voltage**

**TYPICAL MOSFET CHARACTERISTICS (continued)**

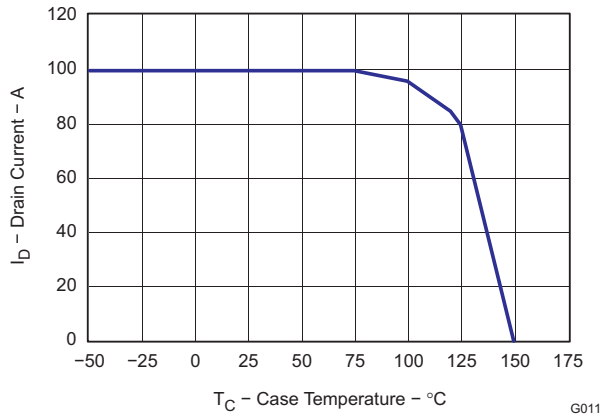
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



**Figure 10. Maximum Safe Operating Area**



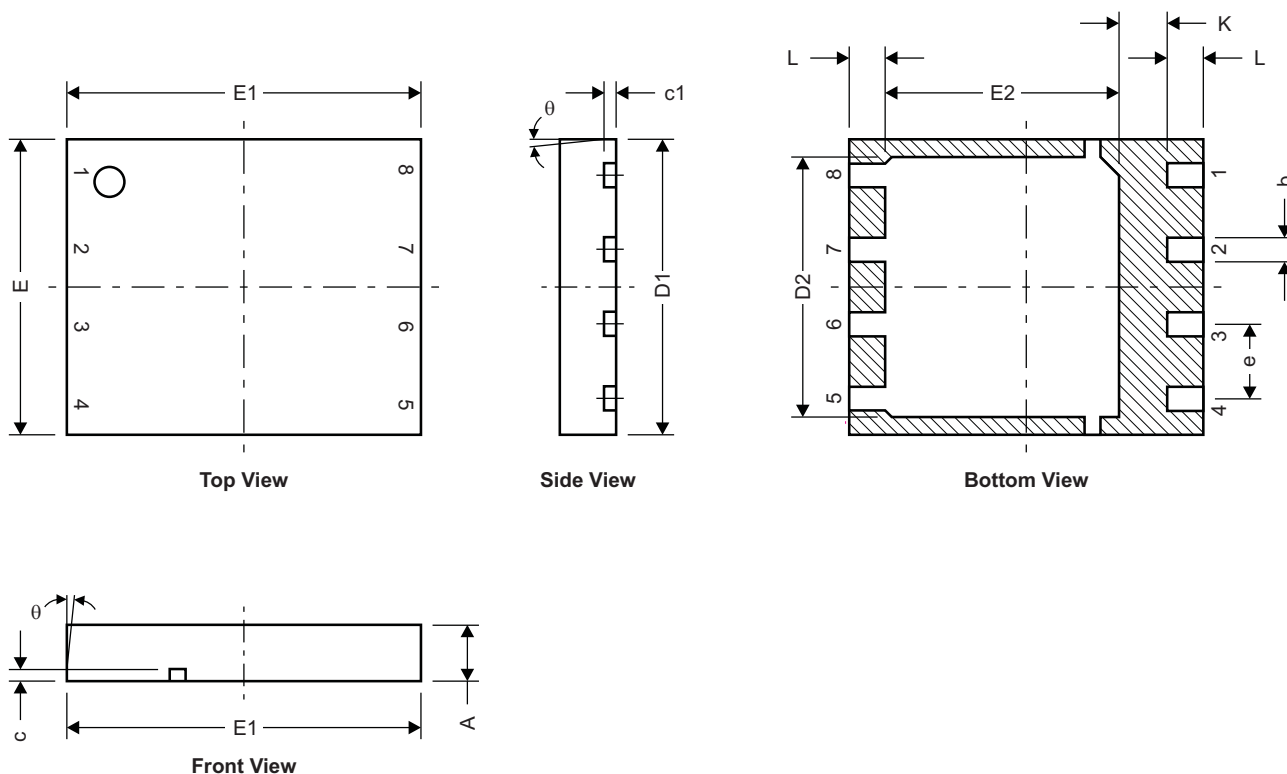
**Figure 11. Single Pulse Unclamped Inductive Switching**



**Figure 12. Maximum Drain Current vs. Temperature**

**MECHANICAL DATA**

**Q5 Package Dimensions**



M0140-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
K	0.760		0.030	
L	0.510	0.710	0.020	0.028
$\theta$	0.00			

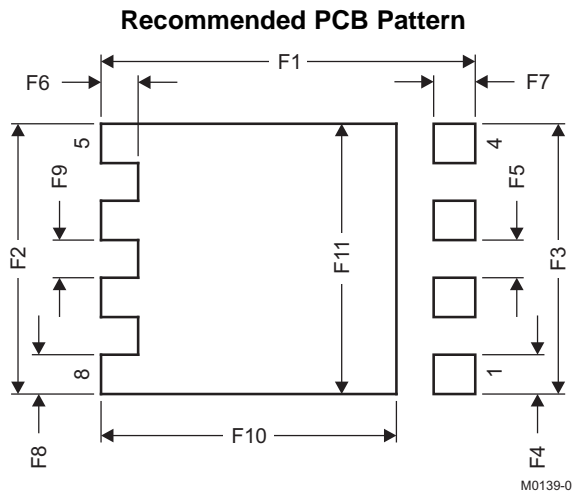


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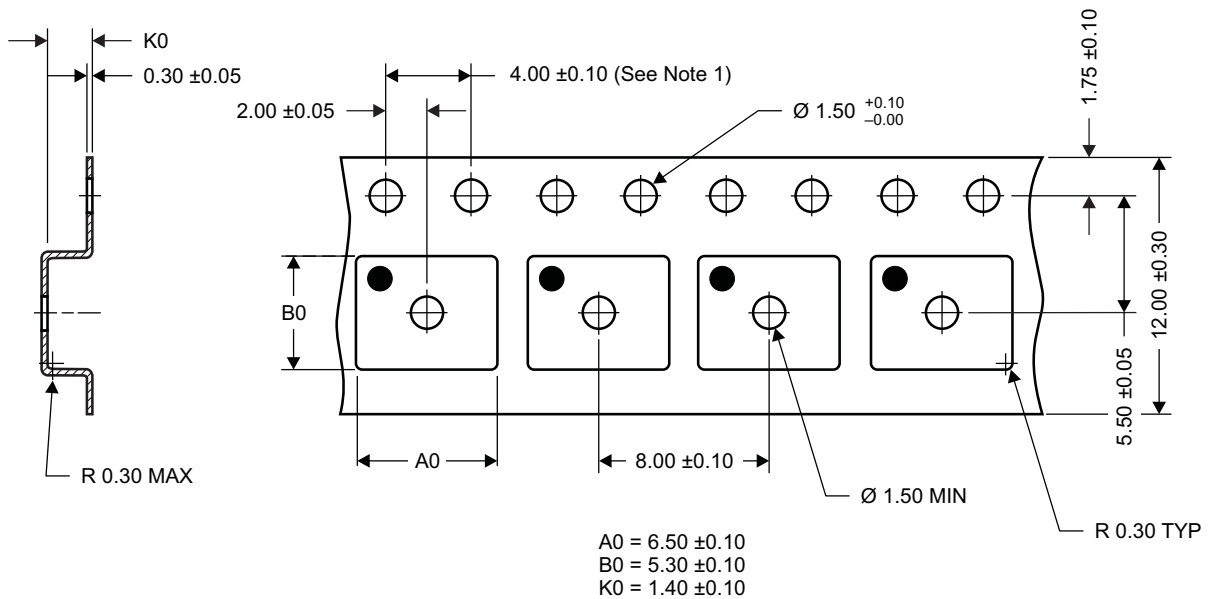
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DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.460	4.560	0.176	0.180
F3	4.460	4.560	0.176	0.180
F4	0.650	0.700	0.026	0.028
F5	0.620	0.670	0.024	0.026
F6	0.630	0.680	0.025	0.027
F7	0.700	0.800	0.028	0.031
F8	0.650	0.700	0.026	0.028
F9	0.620	0.670	0.024	0.026
F10	4.900	5.000	0.193	0.197
F11	4.460	4.560	0.176	0.180

For recommended circuit layout for PCB designs, see application note [SLPA005](#) – Reducing Ringing Through PCB Layout Techniques.

**Q5 Tape and Reel Information**



**Notes:**

- 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$
- Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
- Material: black static dissipative polystyrene
- All dimensions are in mm (unless otherwise specified)
- ThickNess:  $0.30 \pm 0.05$ mm
- MSL1 260°C (IR and Convection) PbF Reflow Compatible

**REVISION HISTORY**

**Changes from Original (August 2009) to Revision A Page**

- Changed the labels on the Top View pinout image ..... 1
- Changed Note 1 of the ABSOLUTE MAXIMUM RATINGS From:  $R_{\theta JA} = 39^{\circ}\text{C/W}$  To: Typical  $R_{\theta JA} = 39^{\circ}\text{C/W}$  ..... 1
- Changed [Figure 1](#) text From:  $R_{\theta JA} = 92^{\circ}\text{C/W}$  To: Typical  $R_{\theta JA} = 93^{\circ}\text{C/W}$  ..... 3
- Changed [Figure 10](#) text From:  $R_{\theta JA} = 92^{\circ}\text{C/W}$  To: Typical  $R_{\theta JA} = 93^{\circ}\text{C/W}$  ..... 6
- Changed [Figure 11](#) X-axis values ..... 6

**Changes from Revision A (January 2010) to Revision B Page**

- Changed  $R_{DS(on)} - V_{GS} = 3\text{V}, I_D = 25\text{A}$  MAX value From: 3.5 To: 3.8 ..... 2
- Deleted the Package Marking Information section ..... 8



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16321Q5	ACTIVE	VSON-CLIP	DQH	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD16321	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**PACKAGE OPTION ADDENDUM**

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7-Jan-2016

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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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