

Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[Fairchild Semiconductor](#)
[29F52SC](#)

For any questions, you can email us directly:

sales@integrated-circuit.com



April 1988
Revised September 2000

29F52 • 29F53 8-Bit Registered Transceiver

General Description

The 29F52 and 29F53 are 8-bit registered transceivers. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-STATE output enable signals are provided for each register. The A_0 – A_7 output pins are guaranteed to sink 24 mA while the B_0 – B_7 output pins are designed for 64 mA.

The 29F53 is an inverting option of the 29F52. Both transceivers are AMD Am2952/2953 functional equivalents.

Features

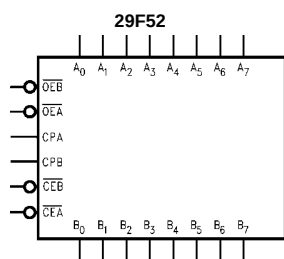
- 8-bit registered transceivers
- Separate clock, clock enable and 3-STATE output enable provided for each register
- AMD Am2952/2953 functional equivalents
- Both inverting and non-inverting options available
- 24-Pin slimline package

Ordering Code:

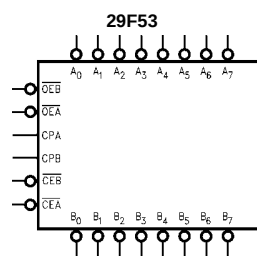
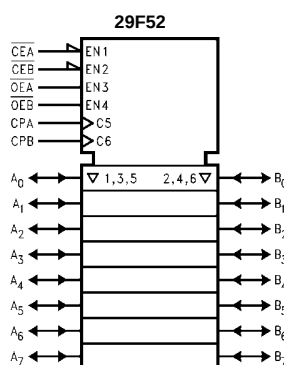
Order Number	Package Number	Package Description
29F52SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
29F52SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
29F53SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

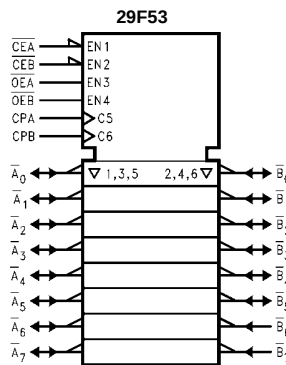
Logic Symbols



IEEE/IEC



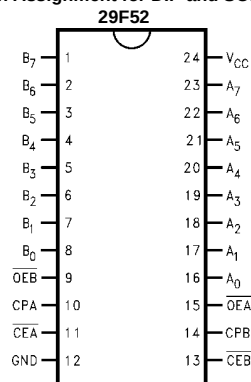
IEEE/IEC



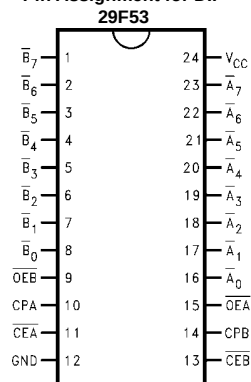
29F52 • 29F53

Connection Diagrams

Pin Assignment for DIP and SOIC



Pin Assignment for DIP



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A ₀ –A ₇	A-Register Inputs/ B-Register 3-STATE Outputs	3.5/1.083	70 μ A/0.65 mA
B ₀ –B ₇	B Register Inputs/ A-Register 3-STATE Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)
		3.5/1.083	70 μ A/0.65 mA
		600/106.6 (80)	–12 mA/64 mA (48 mA)
OEA	Output Enable A-Register	1.0/1.0	20 μ A/–0.6 mA
CPA	A-Register Clock	1.0/1.0	20 μ A/–0.6 mA
CEA	A-Register Clock Enable	1.0/1.0	20 μ A/–0.6 mA
OEB	Output Enable B-Register	1.0/1.0	20 μ A/–0.6 mA
CPB	B-Register Clock	1.0/1.0	20 μ A/–0.6 mA
CEB	B-Register Clock Enable	1.0/1.0	20 μ A/–0.6 mA

Output Control

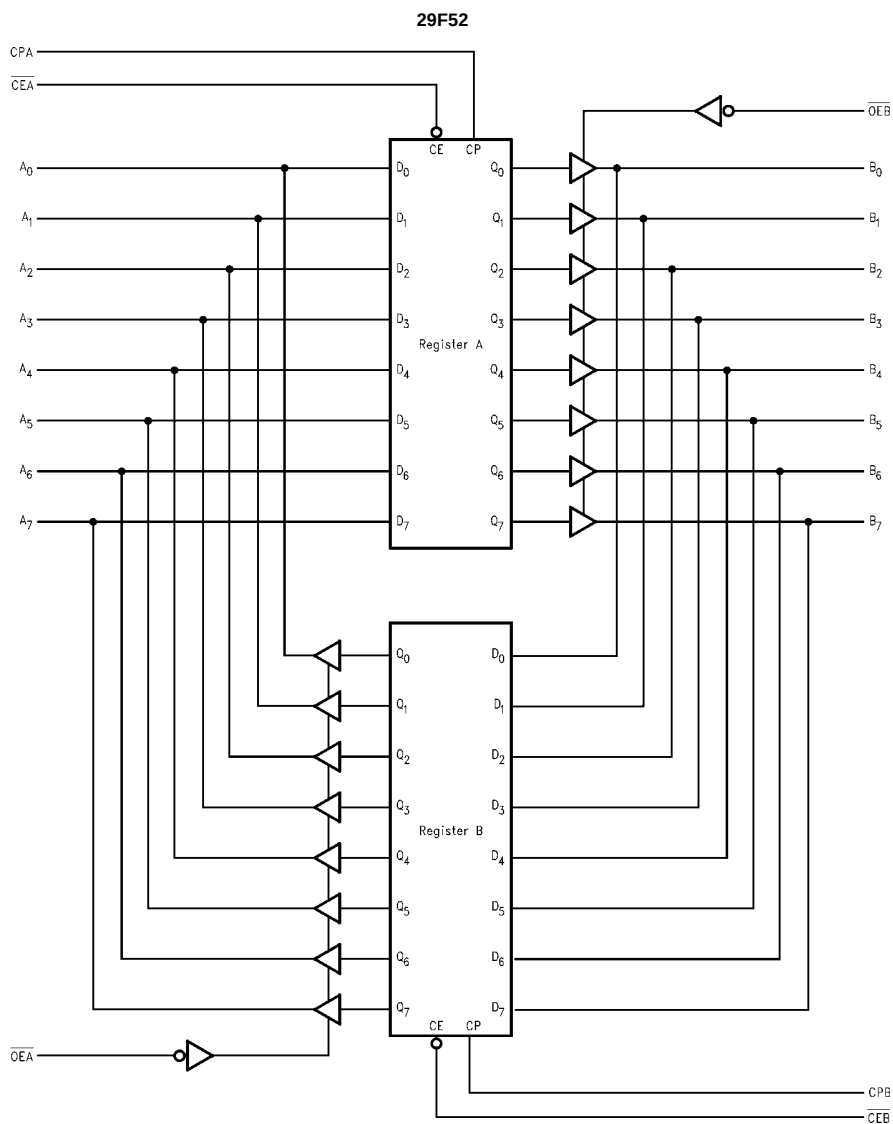
OE	Internal Q	Y-Output		Function
		29F52	29F53	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
N = LOW-to-HIGH Transition
NC = No Change

Register Function Table (Applies to A or B Register)

Inputs			Internal Q	Function
D	CP	CE		
X	X	H	NC	Hold Data
L	N	L	L	Load Data
H	N	L	H	

Block Diagrams

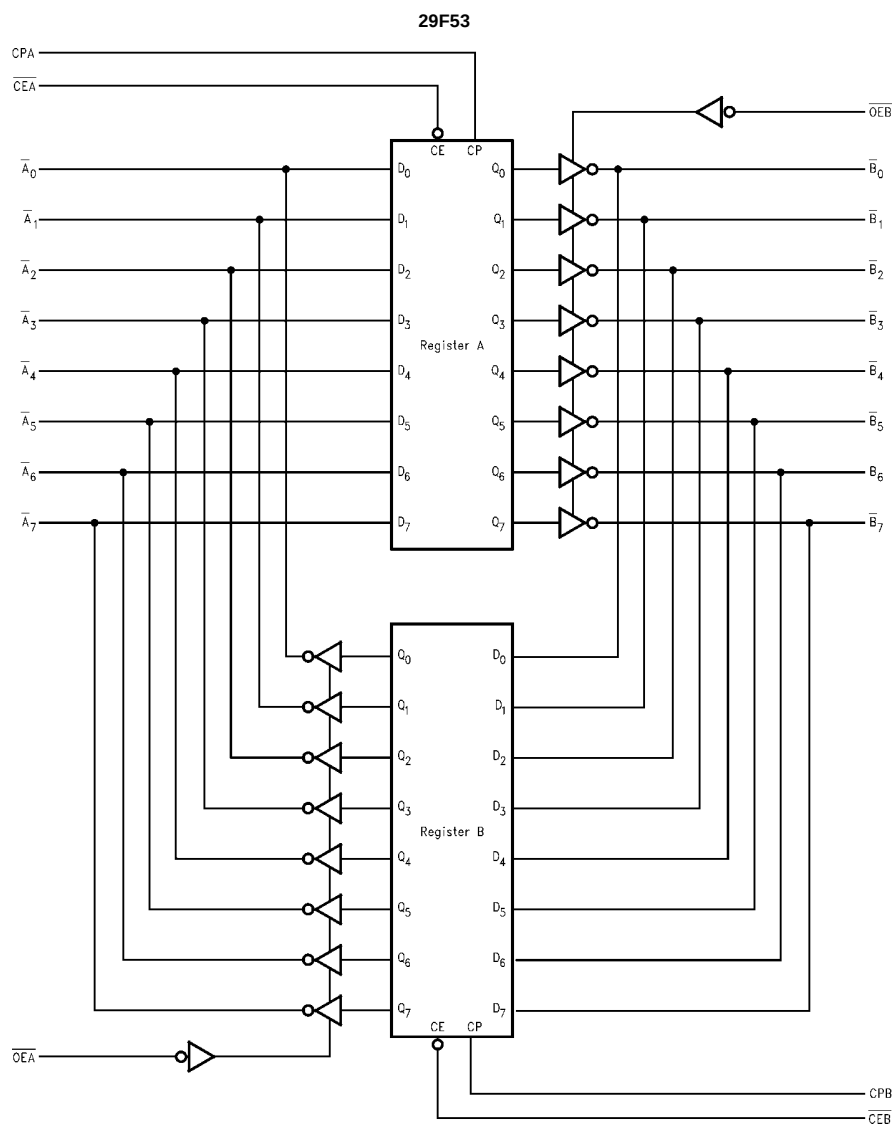


29F52 • 29F53

29F52 • 29F53

Block Diagrams (Continued)

Block Diagrams (continued)



Absolute Maximum Ratings^(Note 1)

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +150°C
V _{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	–0.5V to V _{CC}
3-STATE Output	–0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			–1.2	V	Min	I _{IN} = –18 mA (Non I/O Pins)
V _{OH}	Output HIGH Voltage	10% V _{CC} 10% V _{CC} 10% V _{CC} 5% V _{CC} 5% V _{CC}	2.5 2.4 2.0 2.7 2.7		V	Min	I _{OH} = –1 mA (A _n) I _{OH} = –3 mA (A _n , B _n) I _{OH} = –15 mA (B _n) I _{OH} = –1 mA (A _n) I _{OH} = –3 mA (A _n , B _n)
V _{OL}	Output LOW Voltage	10% V _{CC} 10% V _{CC}		0.5 0.55	V	Min	I _{OL} = 24 mA (A _n) I _{OL} = 64 mA (B _n)
I _{IH}	Input HIGH Current			20	μA	Max	V _{IN} = 2.7V (Non-I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test			100	μA	Max	V _{IN} = 7.0V (Non-I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)			1.0	mA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{IL}	Input LOW Current			–0.6	mA	Max	V _{IN} = 0.5V (Non-I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (A _n , B _n)
I _{IL} + I _{OZL}	Output Leakage Current			–650	μA	Max	V _{OUT} = 0.5V (A _n , B _n)
I _{OS}	Output Short-Circuit Current	–60 –100		–150 –225	mA	Max	V _{OUT} = 0V (A _n) V _{OUT} = 0V (B _n)
I _{CEX}	Output HIGH Leakage Current			250	μA	Max	V _{OUT} = V _{CC} (A _n , B _n)
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V (A _n , B _n)
I _{CCH}	Power Supply Current		130	190	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current			190	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current			190	mA	Max	V _O = HIGH Z

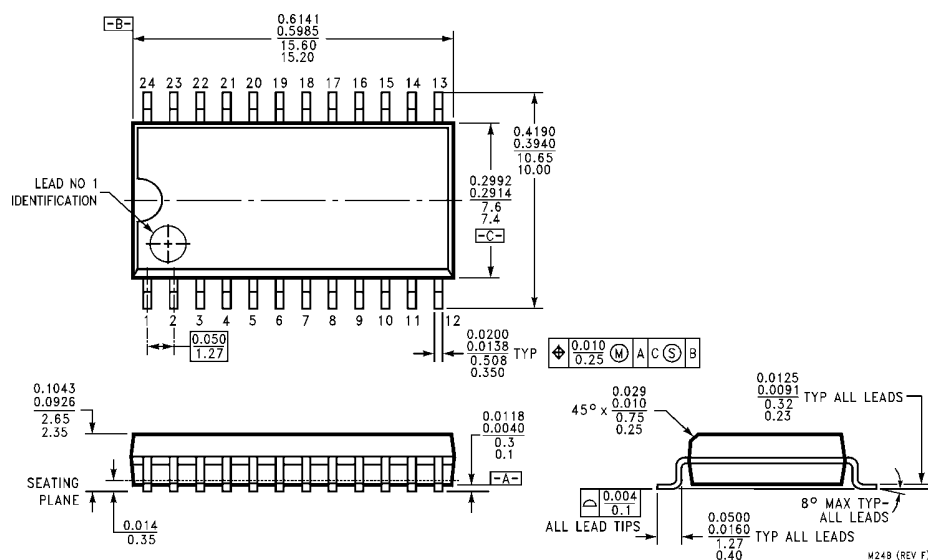
29F52 • 29F53

AC Electrical Characteristics

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = +5.0V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.0	5.5	7.5			2.5	8.5	ns
t _{PHL}	CPA or CPB to A _n or B _n	4.0	7.0	9.0			3.5	10.0	
t _{PZH}	Output Enable Time	2.5	5.5	7.5			2.0	8.5	ns
t _{PZL}	$\overline{\text{OEA}}$ or $\overline{\text{OEB}}$ to A _n or B _n	3.5	7.0	9.5			3.0	10.5	
t _{PHZ}	Output Disable Time	2.5	6.5	9.0			2.0	10.0	ns
t _{PLZ}	$\overline{\text{OEA}}$ or $\overline{\text{OEB}}$ to A _n or B _n	2.5	5.5	7.5			2.0	8.5	

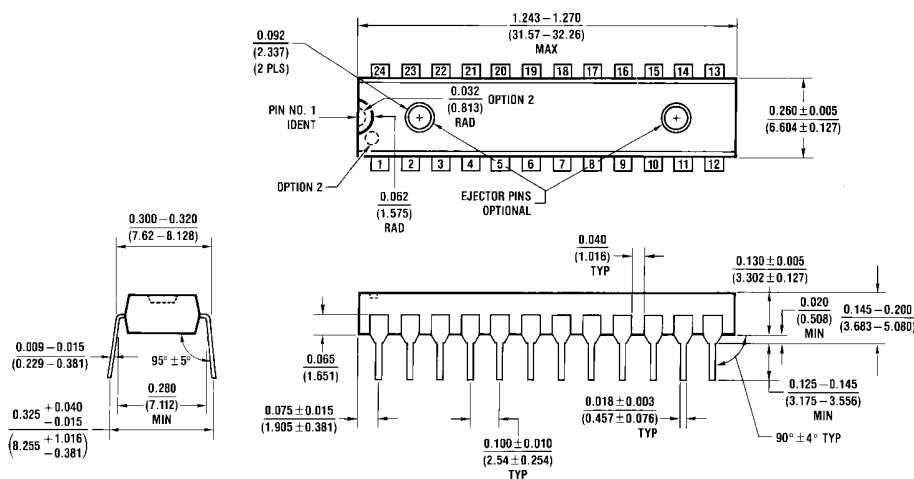
AC Operating Requirements

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V		T _A = -55°C to +125°C V _{CC} = +5.0V		T _A = 0°C to +70°C V _{CC} = +5.0V		Units
		Min	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	4.0				4.5		ns
t _S (L)	A _n or B _n to CPA or CPB	4.0				4.5		
t _H (H)	Hold Time, HIGH or LOW	2.0				2.5		ns
t _H (L)	A _n or B _n to CPA or CPB	2.0				2.5		
t _S (H)	Setup Time, HIGH or LOW	1.0				1.5		ns
t _S (L)	$\overline{\text{CEA}}$ or $\overline{\text{CEB}}$ to CPA or CPB	4.0				4.5		
t _H (H)	Hold Time, HIGH or LOW	2.0				2.5		ns
t _H (L)	$\overline{\text{CEA}}$ or $\overline{\text{CEB}}$ to CPA or CPB	2.0				2.5		
t _W (H)	Pulse Width, HIGH or LOW	3.0				3.5		ns
t _W (L)	CPA or CPB	3.0				3.5		

Physical Dimensions inches (millimeters) unless otherwise noted

**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N24C (REV F)

**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N24C**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com