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TPS65000RTET

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TPS6500xx 2.25-MHz Step-Down Converter With Dual Low Dropouts and Supply Voltage Supervisor

1 Features

- Step-Down Converters:
  - V_{IN} Range From 2.3 V to 6 V
  - Spread Spectrum Clock (SSC) Generation for Reduced EMI
  - 2.25-MHz Fixed Frequency Operation
  - 600-mA or 1-A (TPS650061) Output Current
- Low Dropouts (LDOs):
  - V_{IN} Range From 1.6 V to 6 V
  - Adjustable Output Voltage
  - Up to 300-mA Output Current
  - Separate Power Inputs and Enables
- Supply Voltage Supervisor (TPS65001)
  - Manual Reset Input for Push Button
  - Adjustable Reset Time
  - Adjustable Reset Voltage
- 3-mm × 3-mm 16-Pin WQFN (TPS65000)
- 3-mm × 3-mm 20-Pin WQFN (TPS65001)

2 Applications

- Points-of-Load
- Embedded Processor Power
- Cell Phones
- Smart Phones
- PDAs
- Pocket PCs
- Portable Media Players

3 Description

The TPS6500xx devices are single-chip power management (PWM) ICs for portable applications. Both devices combine a single step-down converter with two low-dropout (LDO) regulators. The step-down converter enters a low-power mode at light load for maximum efficiency across the widest possible range of load currents. For low-noise applications, the devices can be forced into fixed-frequency PWM through a pin. The step-down converter is small because of its small inductor and capacitors. The step-down converter has power good status output for sequencing. The LDOs can supply 300 mA and operate with an input voltage range from 1.6 V to 6 V. A step-down converter or main battery can power the LDOs directly. The step-down converter and the LDOs have separate voltage inputs that enable maximum design and sequencing flexibility.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65000, TPS650001, TPS650003, TPS650006	WQFN (16)	3.00 mm × 3.00 mm
TPS65001, TPS650061	WQFN (20)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Circuit

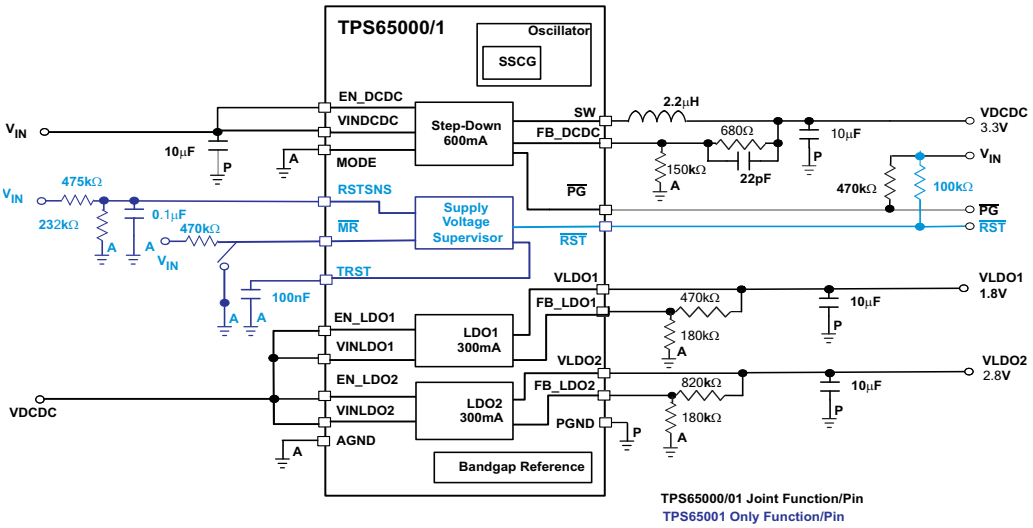


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2010) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (October 2009) to Revision B — **Page**

- In the Ordering Information Table, changed the SVS column From: Included To: N/A for devices TPS650001, TPS650003, TPS650006 ... 3

Changes from Original (June 2009) to Revision A — **Page**

- Added device numbers TPA650001, TPS650003, TPS650006 and TPA650061 to the data sheet. ... 1
- Changed the $\overline{PG}$ pin connection From: VDCDC To: V_{IN} in the application circuit. ... 1
- Changed resistor values for VLDO1 and VLDO2 in the application circuit. ... 1
- Changed the configuration of the $\overline{PG}$ and $\overline{RST}$ pins in the application circuit ... 1
- Added Note 2: to the Electrical Characteristics table. ... 6
- Changed Figure 1 title From: EFFICIENCY (DCDC PFM Mode) To: EFFICIENCY (DCDC 600mA PFM Mode) ... 9
- Changed Figure 2 title From: EFFICIENCY (DCDC PFM Mode) To: EFFICIENCY (DCDC 600mA PFM Mode) ... 9
- Added Figure 3, EFFICIENCY (DCDC PWM Mode) ... 9
- Added Figure 4, EFFICIENCY (DCDC PWM Mode) ... 9
- Changed the configuration of the $\overline{PG}$ pin in Figure 24 ... 20
- Changed the $\overline{PG}$ pin connection From: VDCDC To: V_{IN} in Figure 31. ... 24
- Changed the configuration of the $\overline{PG}$ and $\overline{RST}$ pins in Figure 31 ... 24
- Added Figure 32, Typical TPS650001 Application Schematic ... 25
- Added Figure 33, Typical TPS650061 Application Schematic ... 26

5 Description (continued)

The TPS65001 extends functionality by adding a supply voltage supervisor (SVS). To maximize the flexibility of the SVS, the reset voltage is set with two external resistors and the reset time is set by a small external capacitor. For external control, the SVS can use its active-low manual reset input to connect to a push button.

The TPS65000 is available in a 16-pin leadless package (3 mm × 3 mm QFN). The TPS65001 is available in a 20-pin leadless package (3 mm × 3 mm QFN).

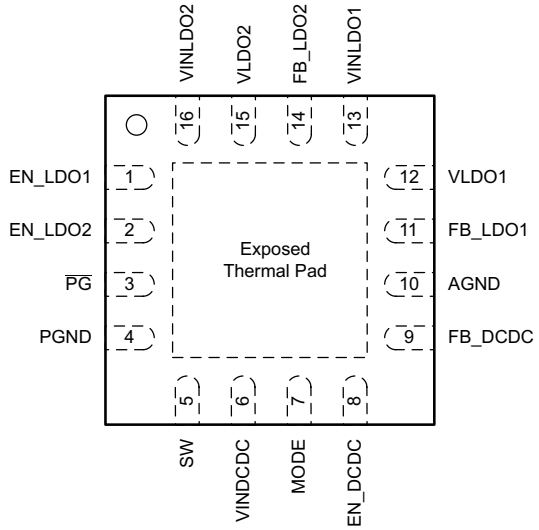
6 Device Options

PART NUMBER(1)(2)	OPTIONS	SVS	SSC
TPS65000	LDO voltages externally adjustable DC-DC converters 600 mA, V_{OUT} externally adjustable	N/A	Included
TPS65001		Included	Included
TPS650001	LDO1 = 1.8 V fixed, LDO2 = 2.8 V fixed, DC-DC Converter 600 MA, DCDC VOUT = 1.2 V fixed	N/A	Included
TPS650003	LDO1 = 3.3 V fixed, LDO2 = 1.8 V fixed, DC-DC Converter 600 MA, DCDC VOUT = 1.5 V fixed	N/A	Included
TPS650006	LDO1 = 1.8 V fixed, LDO2 = 3.3 V fixed, DC-DC Converter 600 MA, DCDC VOUT = 1.2 V fixed	N/A	Included
TPS650061	LDO1 = 3.3 V fixed, LDO2 = 1.8 V fixed, DC-DC Converter 1 A, VOUT externally adjustable	Included	Included

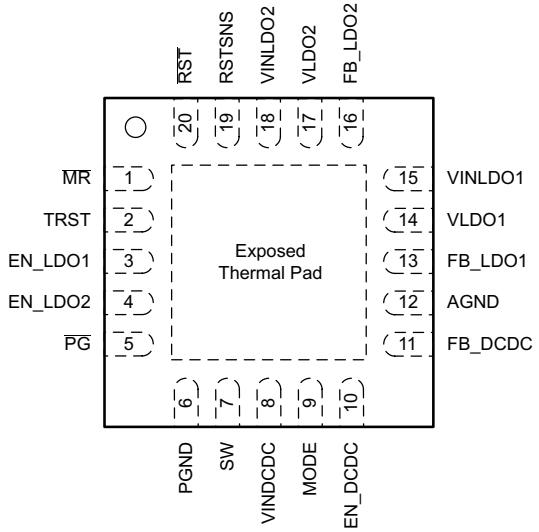
(1) TPS650001, TPS650003, and TPS650006 are spin versions of TPS65000. TPS650061 is a spin version of TPS65001. Different DC-DC current limits and fixed voltage outputs of the DC-DC and LDOs are available. Please contact your TI sales representative for further information.
(2) For the most current package and ordering information, see the *Mechanical, Packaging, and Orderable Information* at the end of this document, or see the TI website at www.ti.com.

7 Pin Configuration and Functions

RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View



RUK Package
20-Pin WQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	16-PIN RTE	20-PIN RUK		
AGND	10	12	—	Analog ground - Start back to PGND as close to the IC as possible.
EN_DCDC	8	10	I	Enable DC-DC converter
EN_LDO1	1	3	I	Enable LDO1
EN_LDO2	2	4	I	Enable LDO2
FB_DCDC	9	11	I	Voltage to DC-DC error amplifier
FB_LDO1	11	13	I	Voltage to LDO1 error amplifier
FB_LDO2	14	16	I	Voltage to LDO2 error amplifier
MODE	7	9	I	Selects force PWM or PWM/PFM automatic-transition mode
$\overline{MR}$	—	1	I	Active-low input to force a reset. (1)
$\overline{PG}$	3	5	O	Open-drain active low power good output.
PGND	4	6	—	Power ground – Connected to the thermal pad
$\overline{RST}$	—	20	O	Open-drain active low reset output
RSTSNS	—	19	I	Voltage for $\overline{RST}$ generation
SW	5	7	O	Switch pin – connect inductor here
TRST	—	2	I/O	Capacitor connection for setting reset time
VINDCDC	6	8	I	Input voltage to DC-DC converter and all other control blocks
VINLDO1	13	15	I	Input voltage to LDO1
VINLDO2	16	18	I	Input voltage to LDO2
VLDO1	12	14	O	LDO1 output voltage
VLDO2	15	17	O	LDO2 output voltage

(1) External pull up on $\overline{MR}$ is required.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage range	On all pins except AGND, PGND, EN_DCDC, VLDO1, VLDO2, FB_LDO1, FB_LDO2, FB_DCDC pins with respect to AGND	–0.3	7	V
	On EN_DCDC with respect to AGND	–0.3	V_{IN} + 0.3, ≤ 7	
Output voltage range	On VLDO1, VLDO2, FB_LDO1, FB_LDO2, FB_DCDC	–0.3	3.6	V
Current	VINDCDC, SW, PGND,		1800	mA
	VINLDO1/2, VLDO1/2, AGND		800	mA
	At all other pins		1	mA
Continuous total power dissipation		See *Dissipation Ratings*		
Operating free-air temperature, T_A		–40	85	°C
Maximum junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±2000	
		Machine model (MM)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
L1	SW pin inductor	1.5	2.2	3.3	µH
C_I	Input capacitor at VINDCDC	10			µF
	Input capacitor at VINLDO1/2	2.2			µF
C_O	Output capacitor for DCDC	10		22	µF
	Output capacitor for LDO1/2	2.2			µF
I_O	DC-DC converter output current			600	mA
	DC-DC converter output current (TPS650061 ONLY)			1000	mA
	LDO1 output current			300	mA
	LDO2 output current			300	mA
T_A	Operating ambient temperature	–40		85	°C

8.4 Thermal Information

THERMAL METRIC[1]		TPS6500x		UNIT
		RTE (WQFN)	RUK (WQFN)	
		16 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.7	46.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.7	51	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16	17.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16	17.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.4	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN_LDOx = EN_DCDC = 3.6 V. External components L = 2.2 µH, C_{OUT} = 10 µF, C_{IN} = 4.7 µF, (see the *Typical Application* section).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING VOLTAGE						
V_{IN}	Input voltage for VINDCDC of DC-DC converter		2.3		6	V
	Input voltage for LDO1 (VINLDO1)	See (1)	1.6		6	
	Input voltage for LDO2 (VINLDO2)	See (1)	1.6		6	
UVLO	Internal undervoltage lockout threshold	V_{CC} falling	1.72	1.77	1.82	V
	Internal undervoltage lockout hysteresis			160		mV
SUPPLY CURRENT TPS65000						
I_Q	Operating quiescent current	MODE low, EN_DCDC high, EN_LDO1/2 low, I_{OUT} = 0 mA and no switching		23	32	µA
		MODE low, EN_DCDC low, EN_LDO1/2 high, I_{OUT} = 0 mA I_{OUT} = 0 mA and no switching (2)		50	57	
		EN_DCDC high, MODE high, EN_LDO1/2 low, I_{OUT} = 0 mA		4		mA
I_{SD}	Shutdown Current	EN_DCDC low EN_LDO1 and EN_LDO2 low		0.16	2.2	µA
SUPPLY CURRENT TPS65001						
I_Q	Operating quiescent current	MODE low, EN_DCDC high, EN_LDO1/2 low, I_{OUT} = 0 mA and no switching		24	37	µA
		MODE low, EN_DCDC low, EN_LDO1/2 high, I_{OUT} = 0 mA I_{OUT} = 0 mA and no switching (2)		55	62	µA
		EN_DCDC high, MODE high, EN_LDO1/2 low, I_{OUT} = 0 mA		4		mA
I_{SD}	Shutdown Current	EN_DCDC low EN_LDO1 and EN_LDO2 low		11	17	µA

(1) The design principle lets only VINDCDC be the highest supply in the system if different voltage input supplies separately to DC-DC converter and LDOs, meaning VINDCDC ≥ VINLDO1, VINDCDC ≥ VINLDO2.
(2) The max quiescent current of enabling LDOs is 8 µA higher for TPS650001, TPS650003, TPS650006, and TPS650061.

Electrical Characteristics (continued)

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN_LDOx = EN_DCDC = 3.6 V. External components L = 2.2 µH, C_{OUT} = 10 µF, C_{IN} = 4.7 µF, (see the *Typical Application* section).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL PINS (EN_DCDC, EN_LDO1, EN_LDO2, MODE, $\overline{PG}$, $\overline{MR}$, $\overline{RST}$)						
V_{IH}	High-level input voltage		1.2			V
V_{IL}	Low-level input voltage				0.4	V
V_{OL}	Low-level output voltage	$\overline{PG}$ and $\overline{RST}$ pins only, I_O = -100 µA			0.4	V
I_{lkg}	Input leakage current	MODE, EN_DCDC, EN_LDO1, EN_LDO2 tied to GND or VINDCDC		0.01	0.1	µA
OSCILLATOR						
f_{SW}	Oscillator frequency		1.722	2.25	2.847	MHz
STEP DOWN CONVERTER POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET ON-resistance	VINDCDC = V_{GS} = 3.6 V		240	480	mΩ
	Low-side MOSFET ON-resistance			185	380	
I_O	DC-output current	2.3 V ≤ VINDCDC ≤ 2.5 V			300	mA
		2.5 V ≤ VINDCDC ≤ 6 V			600	
I_O	DC-output current (TPS650061 ONLY)	2.7 V ≤ VINDCDC ≤ 6 V			1000	mA
I_{LIMF}	Forward current limit PMOS and NMOS	2.3 V ≤ VINDCDC ≤ 6 V	800	1000	1400	mA
I_{LIMF}	Forward current limit PMOS and NMOS (TPS650061 ONLY)	2.7 V ≤ VINDCDC ≤ 6 V	1200	1500	1680	mA
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		30		
STEP DOWN CONVERTER OUTPUT VOLTAGE						
VDCDC	Adjustable output voltage range, DCDC		0.6		VINDCDC	V
	FB_DCDC pin current				0.1	µA
V_{ref}	Internal reference voltage		0.594	0.6	0.606	V
VDCDC	Output Voltage Accuracy (PWM Mode)(3)	MODE = high, 2.3 ≤ VINDCDC ≤ 6 V	–1.5%	0%	1.5%	
	Output Voltage Accuracy (PFM mode) (4)	MODE low 1% voltage positioning active		1%		
	Load regulation (PWM mode)	MODE high		0.5%		A
R_{DIS}	Internal discharge resistance at SW	EN_DCDC low		450		Ω
LOW DROP OUT REGULATORS						
V_I	Input voltage for LDOx (VINLDOx)		1.6		6	V
V_O	Adjustable output voltage, LDOx (VLDOx)(5)		0.73	VINLDOx – V_{DO}		V
I_O	Continuous Pass FET Current				300	mA
I_{SC}	Short circuit current limit	2.3 V ≤ VINLDOx	340		700	mA
		VINLDOx < 2.3V	210		700	
	FB_LDOx pin current				0.1	µA
	FB_LDOx voltage	Adjustable V_{OUT} mode only		0.5		V
V_{DO}	Dropout Voltage (6)	VINLDOx ≥ 2.3 V, I_{OUT} = 250 mA			370	mV
		VINLDOx < 2.3V I_{OUT} = 175 mA			370	mV

(3) For VINDCDC = VDCDC + 1 V
(4) In PFM Mode, the internal reference voltage is typ 1.01 × V_{REF}.
(5) Maximum output voltage VLDOx = 3.6 V.
(6) V_{DO} = VINLDOx – VLDOx where VINLDOx = VLDOx (nominal) – 100 mV

Electrical Characteristics (continued)

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN_LDOx = EN_DCDC = 3.6 V. External components L = 2.2 µH, C_{OUT} = 10 µF, C_{IN} = 4.7 µF, (see the *Typical Application* section).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW DROP OUT REGULATORS (continued)						
	Output Voltage Accuracy (7)	I_O = 1 mA to 300 mA, VINLDOx = 2.3 V – 6 V, VLDOx = 1.2 V	–3.5%		3.5%	
		I_O = 1mA to 175 mA VINLDOx = 1.6 V – 6 V, VLDOx = 1.2 V	–3.5%		3.5%	
	Load regulation	I_O = 1mA to 300 mA VINLDOx = 3.6 V VLDOx = 1.2 V	–1.5%		1.5%	
	Line regulation	VINLDOx = 1.6 V – 6 V VLDOx = 1.2 V at I_O = 1 mA	–0.5%		0.5%	
PSRR	Power Supply Rejection Ratio	f_{NOISE} ≤ 10 kHz, C_{OUT} ≥ 2.2 µF, V_{IN} = 2.3 V, V_{OUT} = 1.3 V I_{OUT} = 10 mA		40		dB
R_{DIS}	Internal discharge resistance at VLDOx	EN_LDOx low		450		Ω
T_{SD}	Thermal shutdown	Increasing temperature		150		°C
	Thermal shutdown hysteresis	Decreasing temperature		30		°C
SUPPLY VOLTAGE SUPERVISOR						
V_{IN}	Input voltage for RSTSNS pin		0		6	V
$t_{\overline{MRDEGLITCH}}$	$\overline{MR}$ Deglitch time			1		ms
V_{IH}	Input high voltage	$\overline{MR}$ pin only	1.2		6	V
V_{IL}	Input low voltage	$\overline{MR}$ pin only	0		0.4	V
I_{lkg}	High-input leakage current	$\overline{RST}$ pin		0.01	0.1	µA
V_{OL}	Output low voltage	$\overline{RST}$ pin only, I_O = –100 µA			0.4	V
I_{TRST}	Reset timer capacitor current		1.6	2	2.2	µA
	Reset voltage trip voltage	Voltage rising (Reset time begins)	0.58	0.6	0.63	V
	Reset voltage trip hysteresis	Voltage falling ($\overline{RST}$ pulled low)		–5%		

(7) Output voltage specification does not include tolerance of external programming resistors.

8.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STEP DOWN CONVERTER OUTPUT VOLTAGE						
t_{Start}	Start-up time	EN_DCDC to start of switching (10%)		250		µs
t_{Ramp}	VDCDC ramp-up time	VDCDC ramp from 10% to 90%		250		µs
LOW DROP OUT REGULATORS						
t_{RAMP}	VLDOx Ramp Time	VLDOx ramp from 10% to 90%		200		µs

8.7 Dissipation Ratings

DEVICE	PACKAGE	$R_{θJA}$	$R_{θJB}$	T_A ≤ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
TPS65000/01 (1)	RTE/RUK	270°C/W	14°C/W	370 mW	204 mW	148 mW
TPS65000/01 (2)		48.7°C/W	14°C/W	2.05 W	1.13 W	821 mW

(1) The JEDEC low-K (1s) board used to derive this data was a 3 in × 3 in, two-layer board with 2-oz copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3 in × 3 in, multilayer board with 1-oz internal power and ground.

8.8 Typical Characteristics

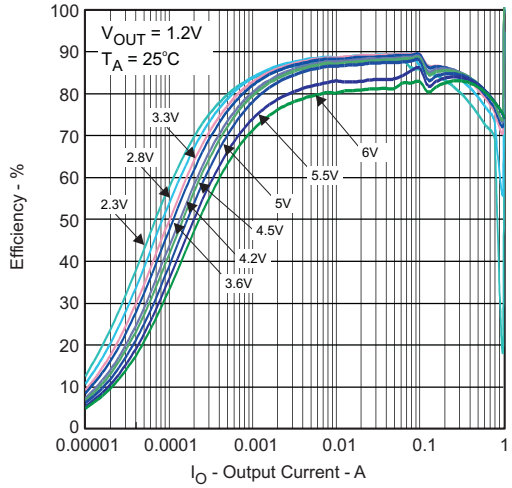


Figure 1. Efficiency (DC-DC 600-mA PFM Mode) vs Output Current

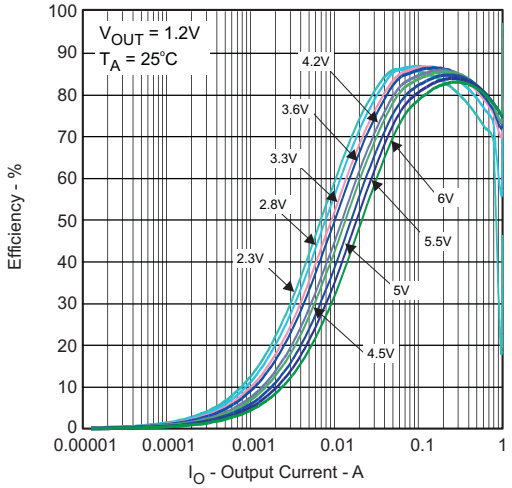


Figure 2. Efficiency (DC-DC 600-mA PWM Mode) vs Output Current

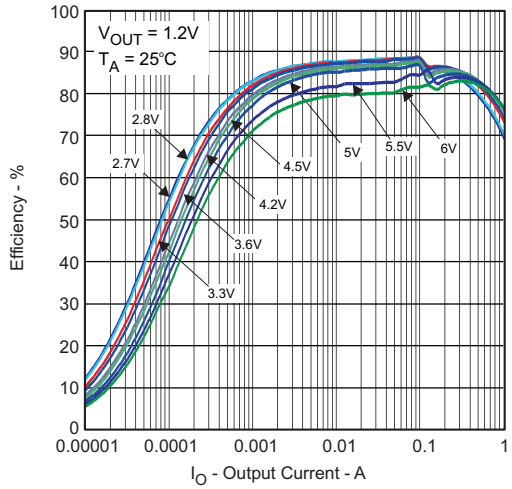


Figure 3. Efficiency (DC-DC 1A TPS650061 Only, PFM Mode) vs Output Current

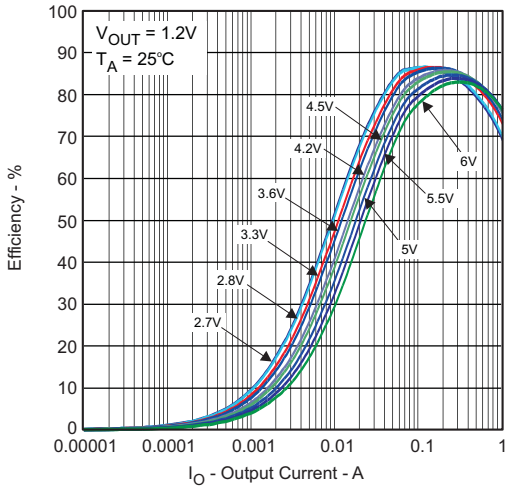


Figure 4. Efficiency (DC-DC 1 A TPS650061 Only, PWM Mode) vs Output Current

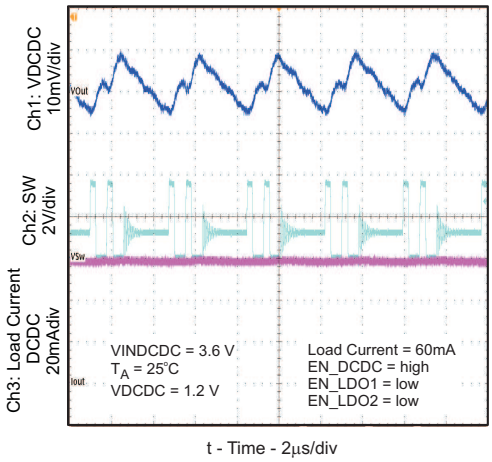


Figure 5. Output Voltage Ripple (DC-DC PFM Mode)

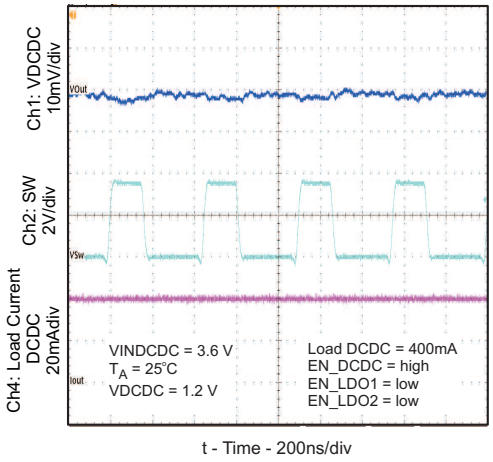


Figure 6. Output Voltage Ripple (DC-DC PWM Mode)

Typical Characteristics (continued)

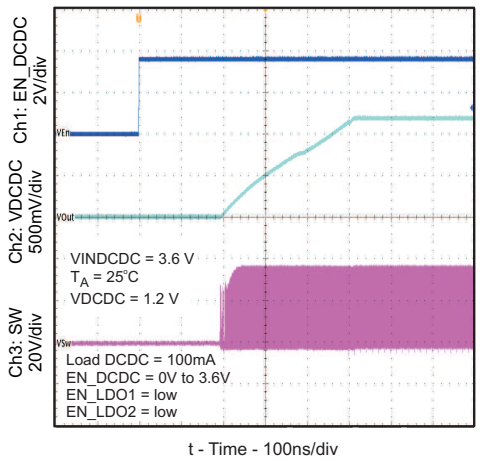


Figure 7. Startup Timing (DC-DC)

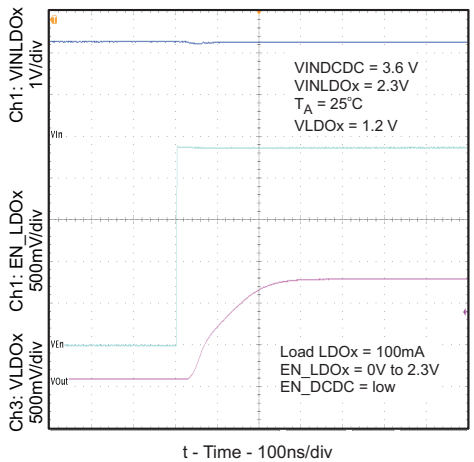


Figure 8. Start-Up Timing (LDOx)

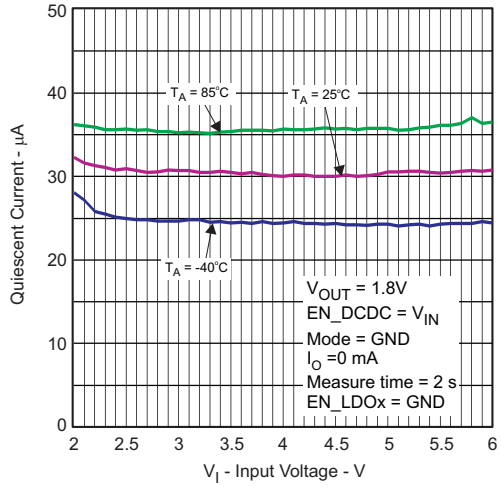


Figure 9. TPS650001 Quiescent Current (DC-DC PFM Mode) vs Input Voltage

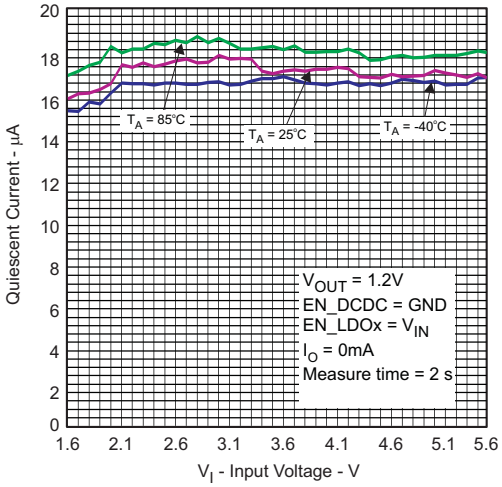


Figure 10. TPS650001 Quiescent Current (LDOx) vs Input Voltage

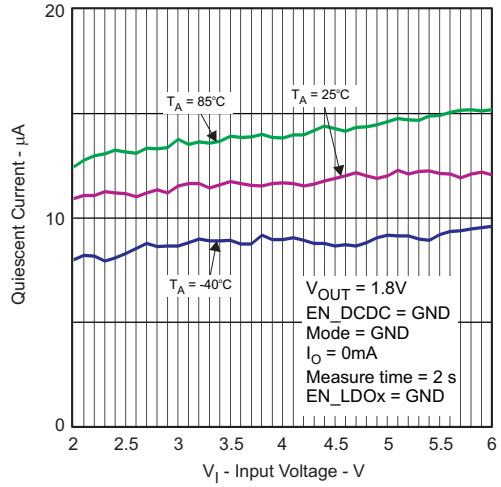


Figure 11. TPS650001 Shutdown Current vs Input Voltage

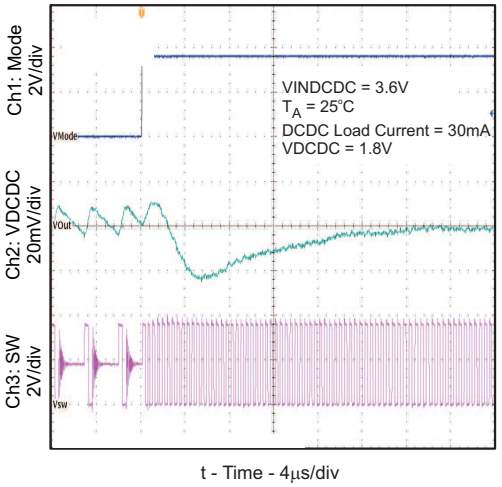


Figure 12. PFM to PWM Transition (DC-DC)

Typical Characteristics (continued)

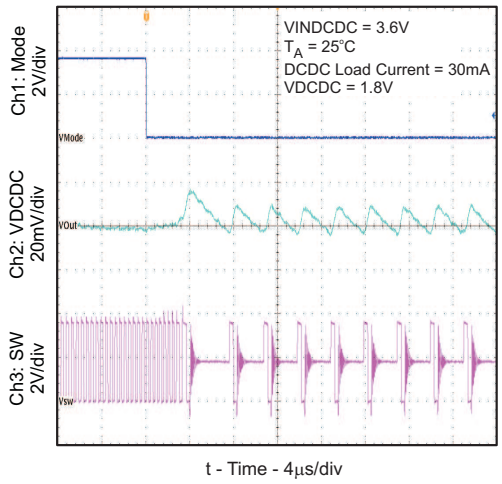


Figure 13. PWM to PFM Transition (DC-DC)

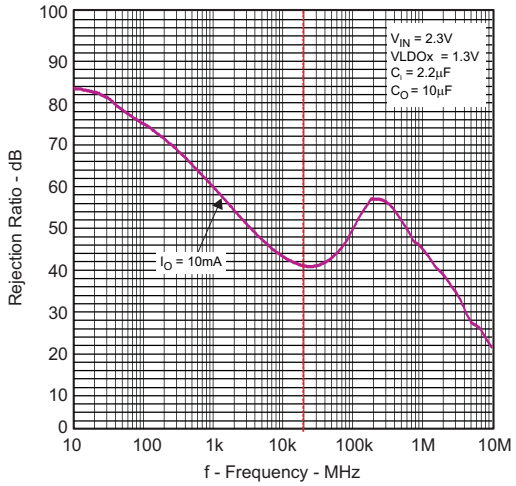


Figure 14. Power Supply Rejection Ratio (LDOx) vs Frequency

9 Detailed Description

9.1 Overview

The TPS6500x provides one step-down converter, two low dropout regulators, spread spectrum clock generation, and a supply voltage supervisor for the TPS65001 only. The device has an input voltage range of 2.3 V to 6 V and is characterized across a –40°C to 85°C range. This device is intended, but not limited, to powering smart phones, embedded processors, and point-of-load devices.

The output voltage of the step-down converter can be selected through resistor networks on the output. To maximize efficiency, there are two modes of operation based on load conditions: PWM or PFM. By pulling the MODE pin high, forced PWM can be achieved. Pulling this pin low results in an automatic adjustment between PFM and PWM modes.

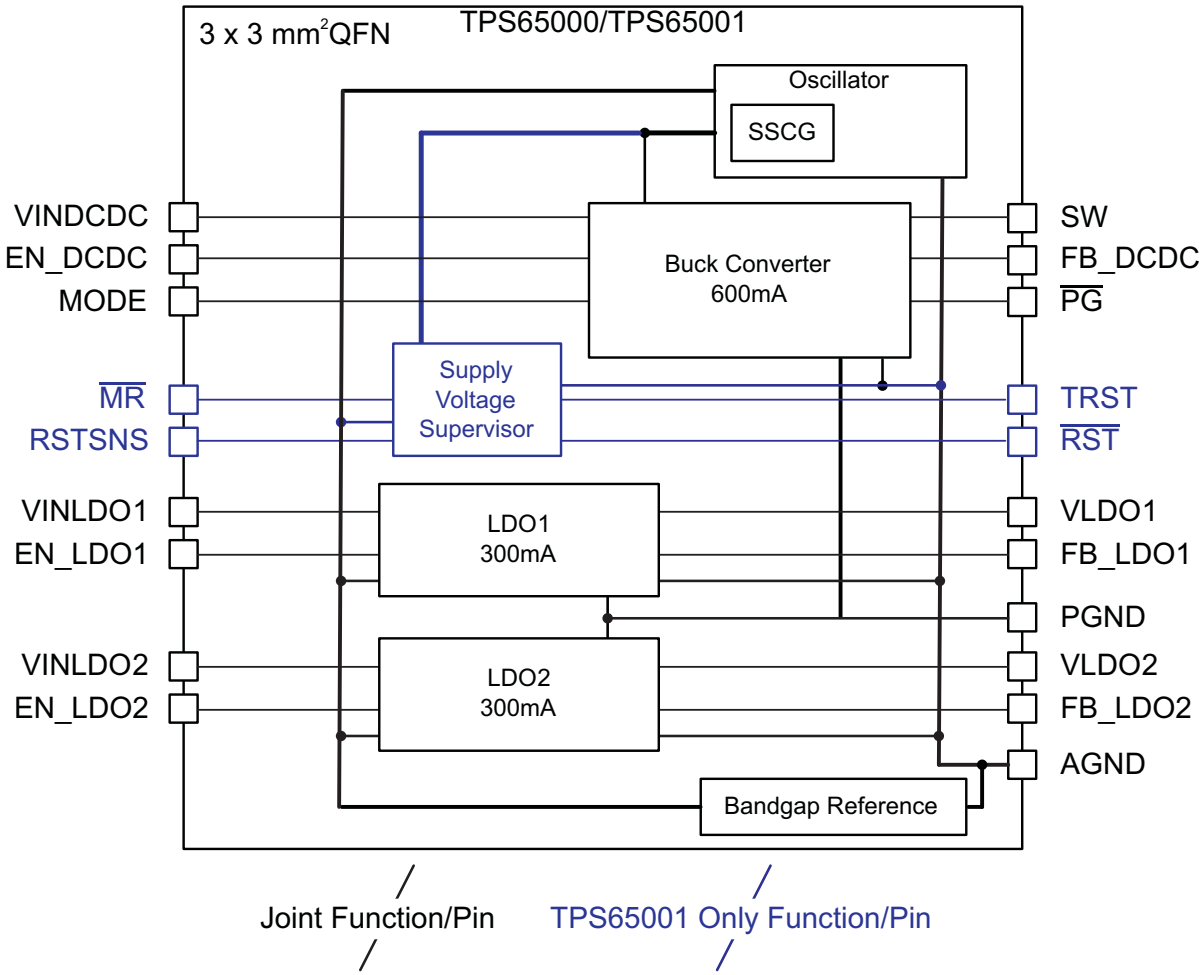
The two general purpose low drop-out regulators each have their own separate enables and voltage inputs. The inputs can be tied to the output of the step-down converter or to a separate voltage source. Resistor networks are required on the output of the regulator to set the output voltage. Their wide voltage range lets them handle direct connections to a battery.

The switching frequency of the step-down converter is handled by the oscillator, with a typical frequency of 2.25 MHz. The spread spectrum clock (SSC) modulates this frequency when the device is in PWM mode. This additional circuit in the oscillator block reduces power that may cause EMI.

The TPS6500x devices also provide a power good signal to monitor the condition of the DC-DC and both LDOs. The DC-DC and LDOs are only monitored if their enable signal is high. If all enabled resources are in regulation, the pin is pulled low. If one or more of the enabled resources are out of regulation, the pin is pulled in Hi-Z.

The supply voltage supervisor is only available for the TPS65001 and TPS650061 devices. This circuit monitors the supply voltage to the device that the TPS65001 and TPS650061 is powering for under voltage conditions. The circuit can connect to a button for manual resets. Reset-recovery time can also be set. Four different scenarios can trigger the circuit to cause a rest.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Step-Down Converter

TI intends the step-down converter to maximize the flexibility in the equipment. The output voltage is selectable with a resistor network on the output. Figure 15 shows the required connections.

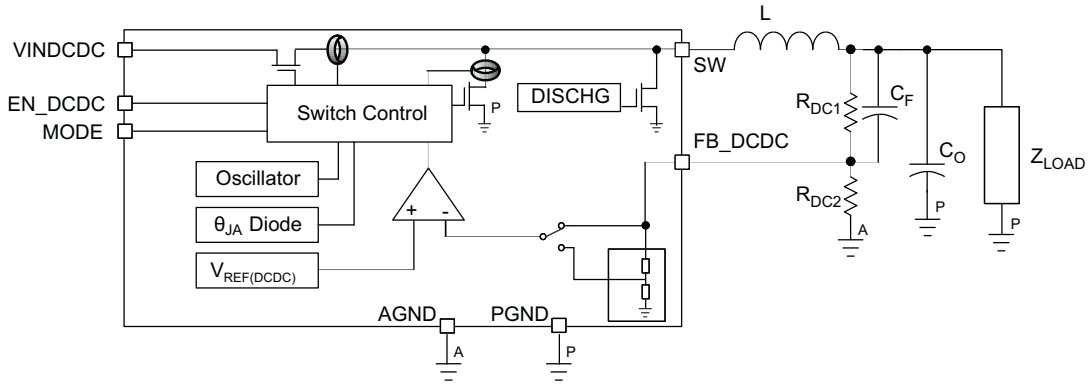


Figure 15. DCDC Block Diagram and Output Voltage Setting

Feature Description (continued)

The output voltage of the DC-DC converter is set by Equation 1:

$$V_{DCDC} = V_{FB\_DCDC} \times \frac{(R_{DC1} + R_{DC2})}{R_{DC2}}$$

$$V_{DCDC} = 0.6V \times \frac{(R_{DC1} + R_{DC2})}{R_{DC2}} \quad (1)$$

The combined resistance of R_{DC1} and R_{DC2} should be less than 1 MΩ.

Fixed output voltages and additional current limit options are also possible. Contact TI for further information.

The step-down converter has two modes of operation to maximize efficiency at different load conditions. At moderate to heavy load currents, the device operates in a fixed-frequency pulse width modulation (PWM) mode that results in small output ripple and high efficiency. Pulling the MODE pin to a DC-high level results in PWM mode over the load range.

At light-load currents, the device operates in a pulsed-frequency modulation (PFM) mode to improve efficiency. The transition to this mode occurs when the inductor current through the low-side FET becomes zero, indicating discontinuous conduction. PFM mode also results in the output voltage increasing by 1% from its nominally set value. TI intends this voltage positioning to minimize the voltage undershoot of a load step from light to heavy loads, as when a processor moves from sleep to active modes, and the voltage overshoot at load throw-off. Figure 16 shows the voltage positioning behavior for a light to heavy load step.

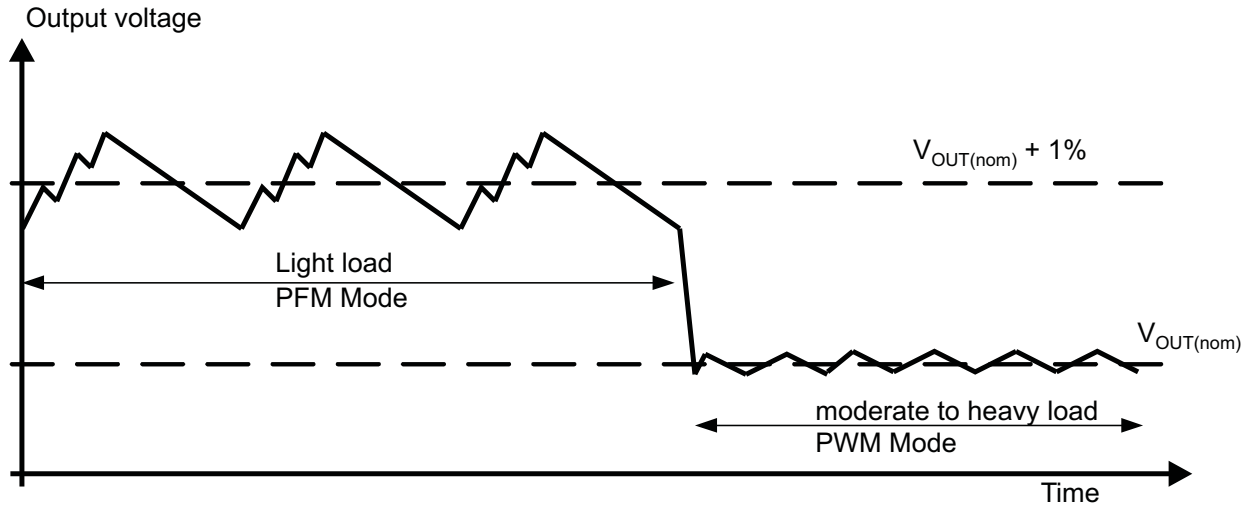


Figure 16. PFM Voltage Positioning

Pulling the MODE pin to DC ground results in an automatic transition between PFM and PWM modes to maximize efficiency.

The DC-DC converter output automatically discharges to ground through an internal 450-Ω load when EN_DCDC goes low or when the UVLO condition is met.

9.3.2 Soft Start

The step-down converter has an internal soft start circuit that limits the inrush current during start-up. During a soft start, the output voltage ramp up is controlled as Figure 17 shows.

Feature Description (continued)

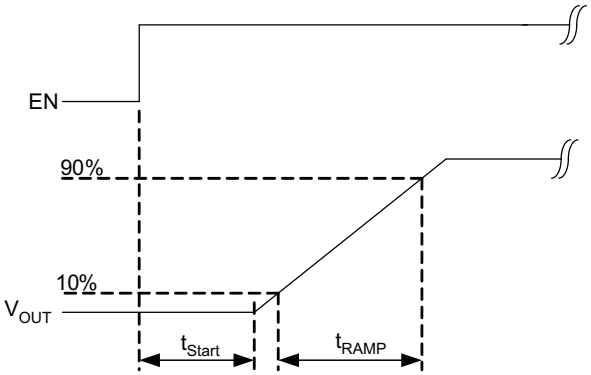


Figure 17. Soft Start

9.3.3 Linear Regulators

TI designed the two linear drop-out regulators (LDOs) in the TPS65000 and TPS65001 to provide flexibility in system design. Each LDO has a separate voltage input and enable signal. The input can be tied to the output of the step-down converter or the output of another voltage source. Each LDO output discharge to ground automatically when EN_LDOx goes low.

A resistor network is required to set the output voltage of the LDOs. Fixed-voltage output versions are also available. Contact TI sales representative for more information.

The LDOs are general-purpose devices that can handle inputs from 6 V to 1.6 V, making them suitable for directly connecting to the battery. Figure 18 illustrates the connections for LDO1. The same architecture applies to LDO2.

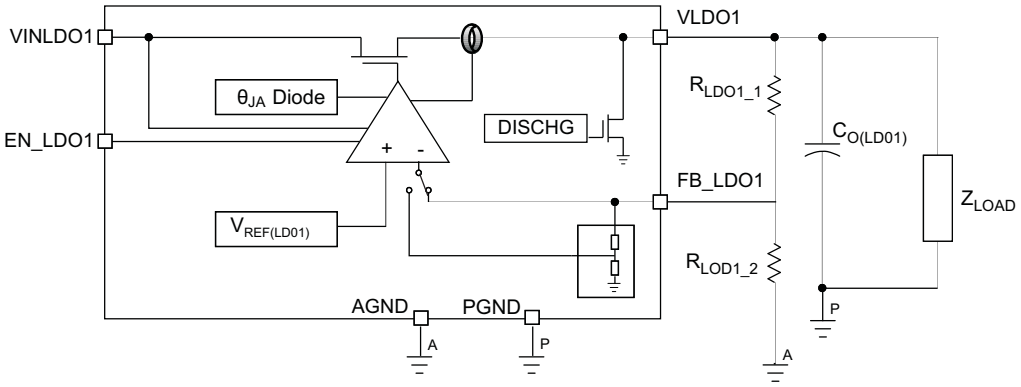


Figure 18. LDO Block Diagram and Output Voltage Setting

The output voltages of the LDOs are set by Equation 2:

$$V_{LDO1} = V_{FB\_LDO1} \times \frac{\left(R_{LDO1\_1} + R_{LDO1\_2}\right)}{R_{LDO1\_2}}$$

$$V_{LDO1} = 0.5V \times \frac{\left(R_{LDO1\_1} + R_{LDO1\_2}\right)}{R_{LDO1\_2}} \quad (2)$$

The combined resistance of R_{LDO1_1} and R_{LDO1_2} should be less than 1 MΩ.

Feature Description (continued)

9.3.4 Oscillator and Spread Spectrum Clock Generation

The TPS6500x contains an internal oscillator running at a typical frequency of 2.25 MHz. This frequency is the fundamental switching frequency of the step-down converter when running in PWM mode. An additional circuit in the oscillator block implements spread spectrum clocking, which modulates the main-switching frequency when the device is in PWM mode. This spread spectrum oscillation reduces the power that may cause EMI. When viewed in the frequency domain, the SSC spreads out the frequency that may introduce interference while simultaneously reducing the power. Because the frequency is continually shifting, the amount of time the switcher spends at any single frequency is reduced. This reduction in time indicates that the receiver that may sense the interference has less time to integrate the interference.

Different spin versions of SSC settings are also feasible. Contact a TI sales representative for more information.

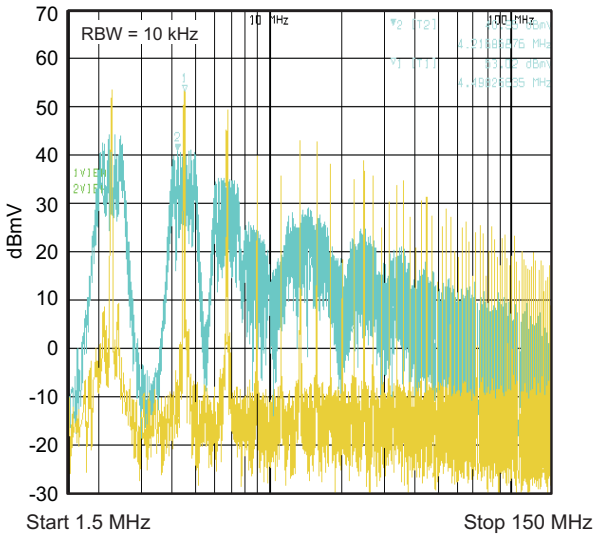


Figure 19. SSC On/Off Comparison from 1.5 MHz to 150 MHz

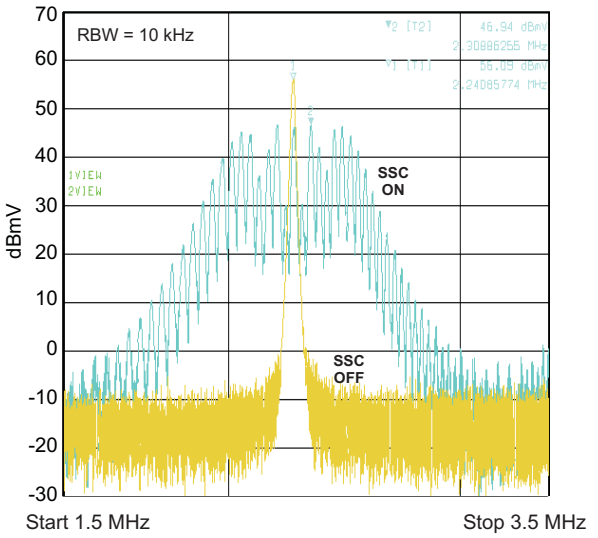


Figure 20. Zoom In of SSC On/Off Comparison from 1.5 MHz to 3.5 MHz

Figure 19 to Figure 20 shows the advantage of SSC with the frequency spectrum centering on the nominal frequency 2.25 MHz. The blue spectrum is the result of the spread change. The figures show the harmonic spectrum is attenuated 10 dB comparing to the same device without SSC.

9.3.5 Power Good

The open drain $\overline{PG}$ output indicates the condition of the step-down converter and each LDO. This output is combined, with the outputs being compared when the appropriate enable signal is high. The pin is pulled low when all enabled outputs are greater than 90% of the target voltage and Hi-Z when an enabled output is less than 90% of its intended value or when all the enable signals are pulled low.

Feature Description (continued)

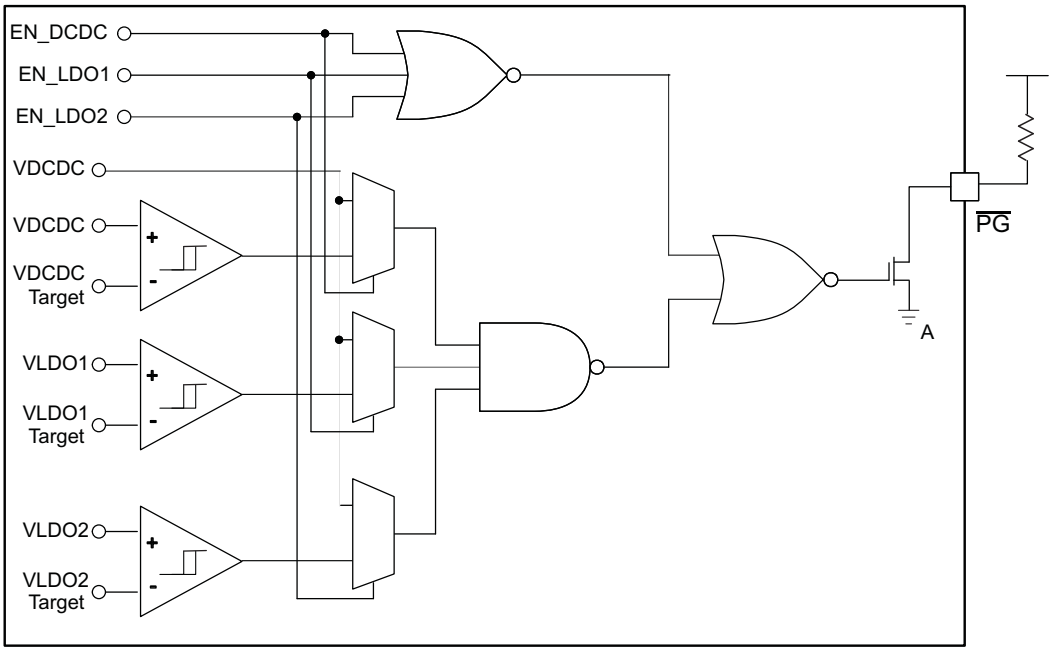


Figure 21. Power Good Functionality

9.3.6 Supply Voltage Supervisor (SVS) [TPS65001 and TPS650061 Only]

The SVS has fourinputs and one output. The $\overline{RST}$ pin is an active-low high-impedance output. The $\overline{MR}$ pin is an active-low input that suitable for connecting to a push-button circuit for manual reset generation. The RSTSNS pin is an analog-input pin for voltage comparison. The TRST pin is connected to an external capacitor, allowing the reset timing to be set in the application. The VINDCDC pin is the main-supply input for the control circuits and the switch-mode converter.

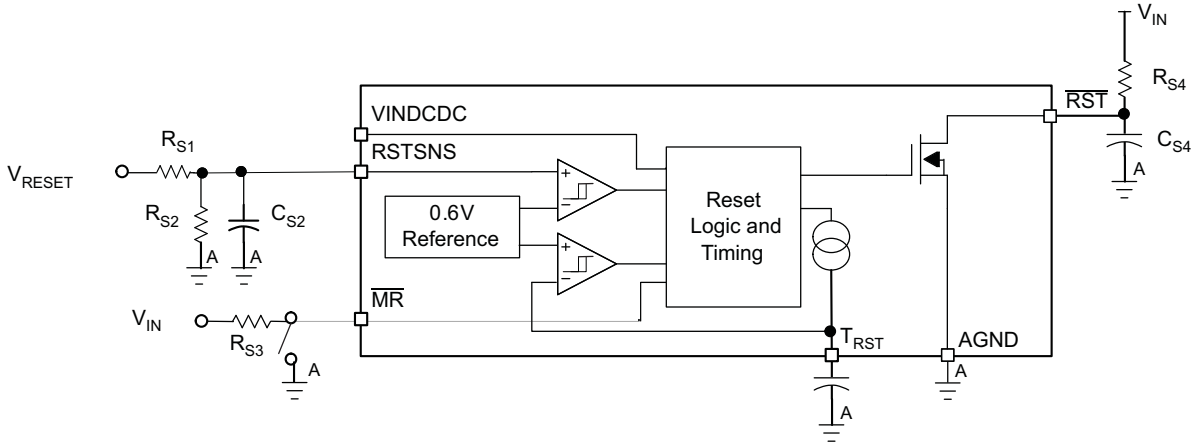


Figure 22. SVS Block Diagram

Each input can individually trigger $\overline{RST}$ to go active. Table 1 outlines the paths to activate the reset.

Feature Description (continued)

Table 1. $\overline{RST}$ Generation Table

INPUTS			OUTPUTS
VINDCDC	$\overline{MR}$	V_{RSTSNS}	$\overline{RST}$
0.4 < V < UVLO	X	X	Low
> UVLO	≥ $V_{IH(\overline{MR})}$	≤ 0.6 V	Low
> UVLO	≥ $V_{IH(\overline{MR})}$	> 0.6 V	High-Z
> UVLO	< $V_{IL(\overline{MR})}$	X	Low

The RSTSNS pin must be tied to VINDCDC if the reset functionality is not required from this pin. This action causes the reset to activate only when VINDCDC is rising from 0 V or when VINDCDC drops below UVLO. The RSTSNS pin must connect to an external RC network to set the deglitch timing for triggering a reset when VINDCDC is below the UVLO threshold. The reset threshold voltage is given by Equation 3:

$$V_{RST} = 0.6V \times \frac{(R_{S2} + R_{S1})}{R_{S2}} \quad (3)$$

The $\overline{RST}$ recovery timing is set by the capacitor on the TRST pin. A 2-µA current is enabled when the reset condition is met, charging the capacitor. The TRST voltage is monitored internally and the reset ends when the voltage reaches 0.6 V. The capacitor value to reset time can be computed with Equation 4:

$$t_{RST} = 0.6V \times \frac{C}{2 \times 10^{-6} A} \quad (4)$$

The value t_{RST} is the time from the end of condition that activated $\overline{RST}$ until $\overline{RST}$ returns to its Hi-Z state. The TRST pin would be internally discharged to ground when the reset condition is true or after t_{RST}.

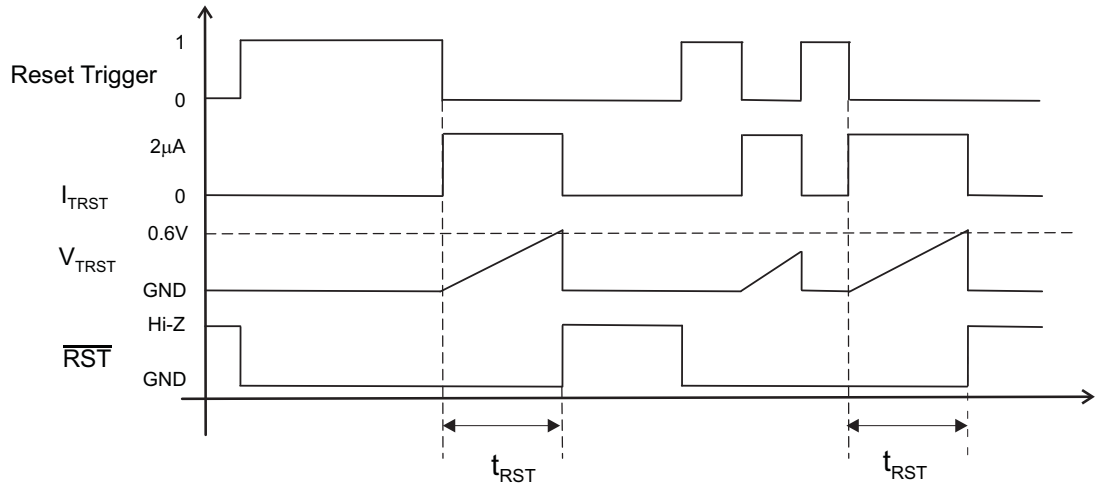


Figure 23. $\overline{RST}$ Recovery Timing

9.4 Device Functional Modes

The step-down converter has two modes of operation to maximize efficiency:

PFM

- For light loads
- For automatic transition to between this mode and PWM mode automatically when MODE pin is pulled low over all load ranges
- To increase in output voltage setting by 1%
- For better accuracy

PWM

- For moderate to heavy loads
- For a small output ripple
- For pulling MODE pin high to result in PWM mode over all load range

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI-component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS65000 device is designed to pair with various applications, such as embedded processor power and portable media players. For detailed information on using the TPS65000 with TMS32C2834x, see *Related Documentation*.

TI designed the TPS65001 device to pair with various applications, such as PDAs and pocket PCs. For detailed information on using the TPS65001 with TMS320C5504/05, see *Related Documentation*.

TI designed the TPS650001 and TPS650061 devices to pair with various applications, such as cell and smart phones, as well as point-of-load. For detailed information on using the TPS650001 and TPS650061 with OMAP-L13x, see *Related Documentation*.

10.2 Typical Application

10.2.1 Typical TPS65000 Application

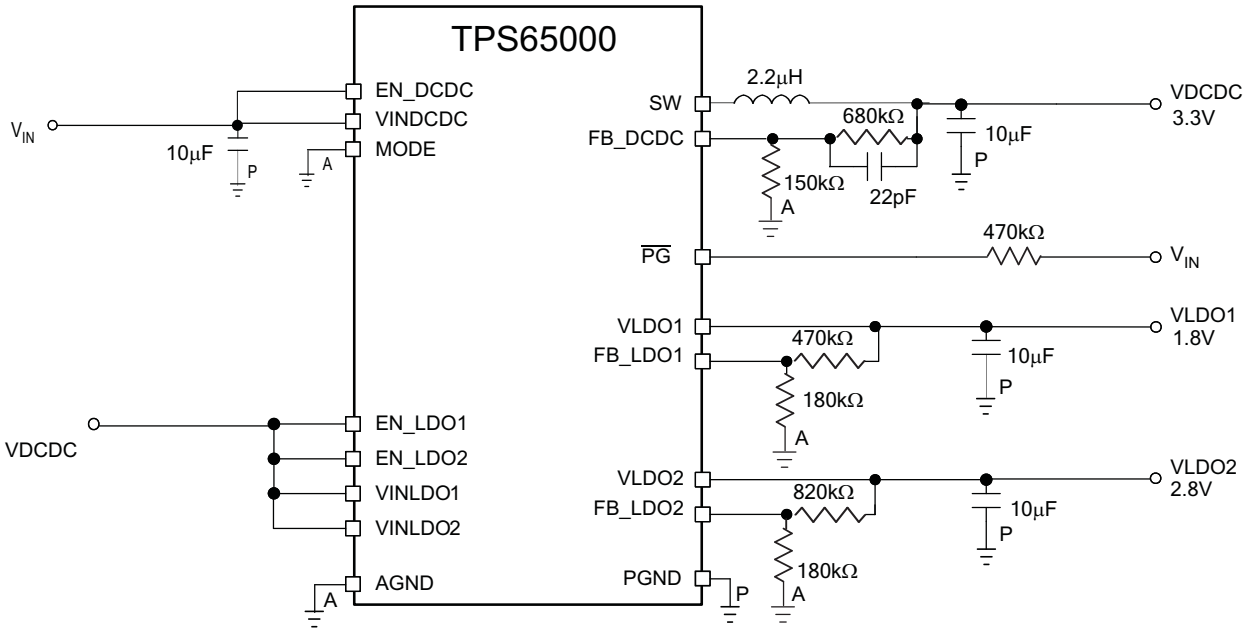


Figure 24. Typical TPS65000 Application Schematic

10.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

RESOURCES	VOLTAGE
SW	3.3 V
VLDO1	1.8 V
VLDO2	2.8 V

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Output Filter Design (Inductor and Output Capacitor)

10.2.1.2.1.1 Inductor Selection

The typical value for the converter inductor is 2.2-µH output inductor. Larger or smaller inductor values in the range of 1.5 µH to 3.3 µH can optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductance influences the efficiency of the converter directly. An inductor with lowest DC resistance must be selected for highest efficiency. See SLVA157 for more information on inductor selection.

Equation 5 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 6. TI recommends this because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \quad (5)$$

where

- f = Switching Frequency (2.25 MHz typical)
- L = Inductor Value
- ΔI_L = Peak to Peak Inductor Ripple Current

$$I_{Lmax} = I_{OUTmax} + \frac{\Delta I_L}{2} \quad (6)$$

where

- I_{Lmax} = Maximum Inductor Current

The highest inductor current occurs at maximum V_{IN}.

Open-core inductors have a soft saturation characteristic and can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. Consider that the core material from inductor to inductor differs and impacts the efficiency especially at high-switching frequencies.

The step down converter has internal loop compensation. TI designed the internal loop compensation to work with a certain output filter corner frequency calculated as follows:

$$f_C = \frac{1}{2\pi \sqrt{L \times C_{OUT}}} \text{ with } L = 2.2\mu H,\ C_{OUT} = 10\mu F \quad (7)$$

The selection of external L-C filter must be coped with Equation 7. The product of L × C_{OUT} must be constant while selecting smaller inductor or increasing output capacitor value.

See Table 3 and the typical applications for possible inductors.

Table 3. Inductors

INDUCTOR TYPE	INDUCTANCE (µH)	SUPPLIER	MAX DIMENSIONS (mm)
MIPS2520D2R2	2.0	FDK	2.5 × 2.0 × 1.0
MIPSA2520D2R2	2.0	FDK	2.5 × 2.0 × 1.2
KSLI-252010AG2R2	2.2	Htachi Metals	2.5 × 2.0 × 1.0
LQM2HPN2R2MJ0L	2.2	Murata	2.5 × 2.0 × 1.2
LPS15222	2.2	Coilcraft	3.0 × 3.0 × 1.5

10.2.1.2.1.2 Output Capacitor Selection

The advanced fast response voltage mode control scheme of the converter allows the use of small ceramic capacitors with a typical value of 22 µF, without having large output voltage under and overshoots during heavy load transients. TI recommends ceramic capacitors with low ESR values because they result in lowest output voltage ripple. See the TI-recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. The RMS ripple current is calculated as the following:

$$I_{RMSCout} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (8)$$

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad (9)$$

Where the highest output voltage ripple occurs at the highest input voltage V_{IN}.

At light load currents, the converter operates in power save mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

The adjustable output voltage of the DC-DC converter is calculated by Equation 1 in the *Step-Down Converter*. To keep the external resistor divider network robust against noise, an external feed forward capacitor is required for optimum load transient response. The value of feed forward capacitor must be in the range between 22 pF and 33 pF provided the equivalent resistance of RDC1 || RDC2 in Equation 1 is approximately 300 kΩ. Scale change on RDC1||RDC2 would apply a scale change to the feed forward capacitor to keep the RC product a constant.

10.2.1.2.1.3 Input Capacitor Selection

Due to the DC-DC converter having a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering, and minimizing the interference with other circuits caused by high-input voltage spikes. Put the input capacitor as close to the VINDCDC pin as close as possible with the clean GND connection. Do the same for the output capacitor and the inductor. The converters require a ceramic input capacitor of 10 µF. The input capacitor can increase without any limit for better input voltage filtering.

Table 4. Capacitors

CAPACITANCE	SUPPLIER	TYPE
22 µF	TDK C2012X5R0J226MT	Ceramic
22 µF	Taiyo Yuden JMK212BJ226MG	Ceramic
10 µF	Taiyo Yuden JMK212BJ106M	Ceramic
10 µF	TDK C2012X5R0J106M	Ceramic
10 µF	Murata GRM188R60J106M69D	Ceramic

10.2.1.3 Application Curves

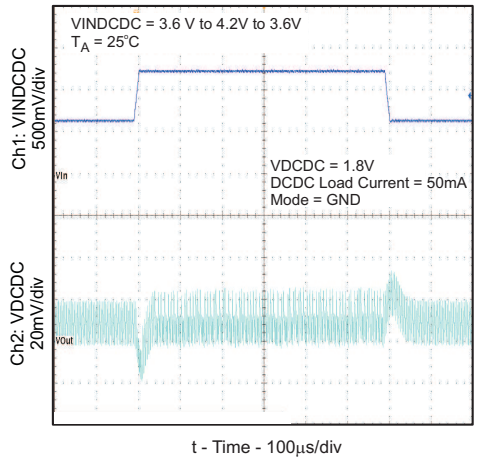


Figure 25. Line Transient Response (DC-DC PFM Mode)

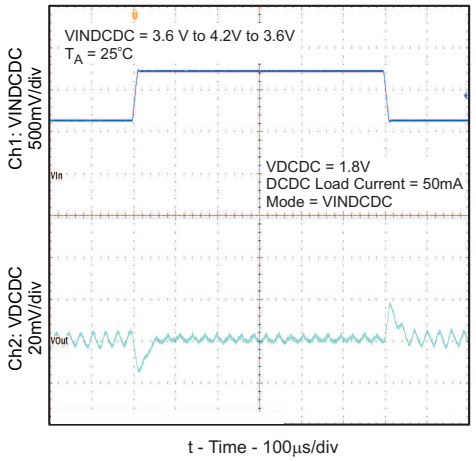


Figure 26. Line Transient Response (DC-DC PWM Mode)

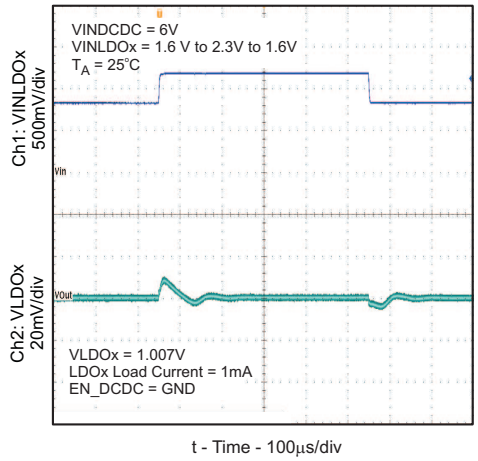


Figure 27. Line Transient Response (LDOx)

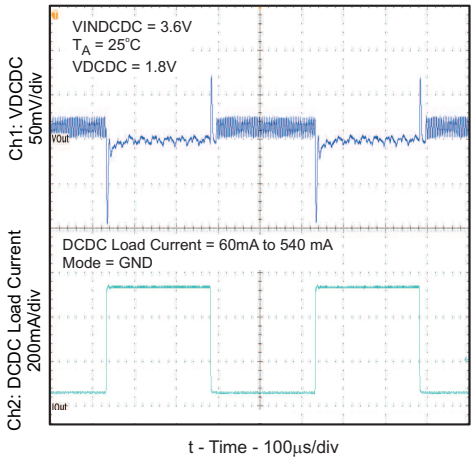


Figure 28. Load Transient Response (DC-DC PFM Mode)

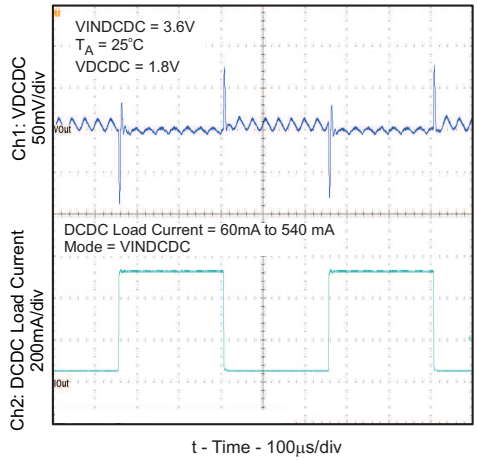


Figure 29. Load Transient Response (DC-DC PWM Mode)

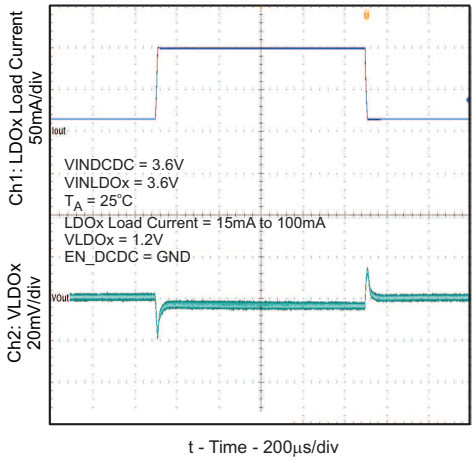


Figure 30. Load Transient Response (LDOx)

10.2.2 Typical TPS65001 Application

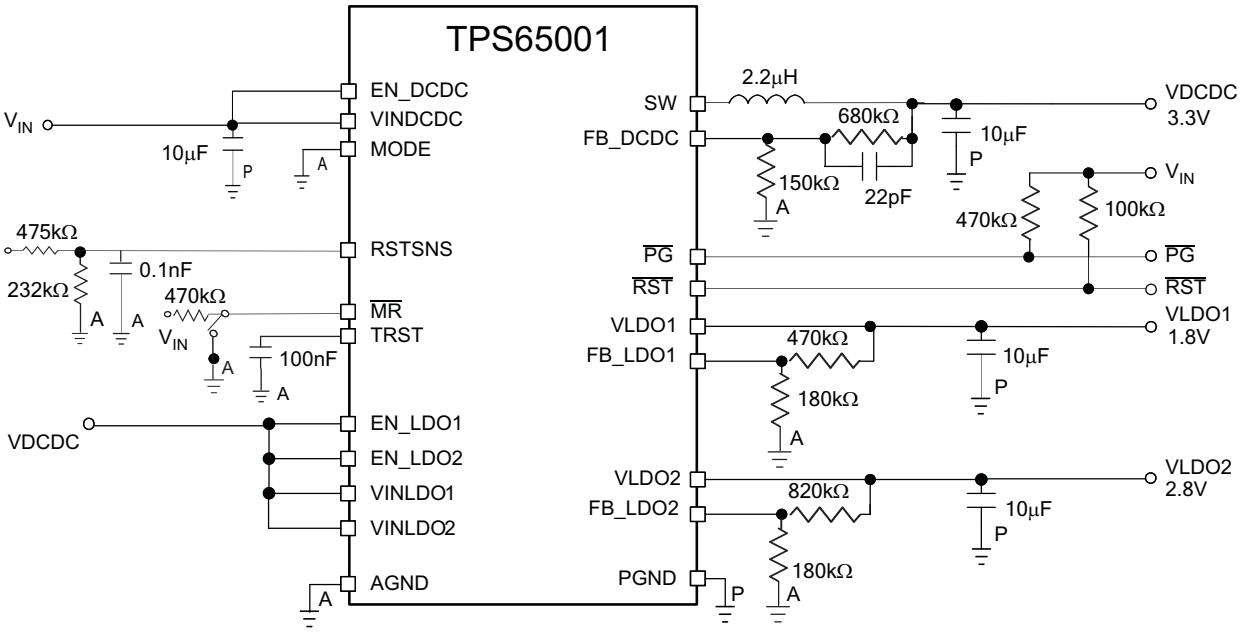


Figure 31. Typical TPS65001 Application Schematic

10.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 5.

Table 5. Design Parameters

RESOURCES	VOLTAGE
SW	1.2 V
VLDO1	1.8 V
VLDO2	2.8 V

10.2.3 Typical TPS650001 Application

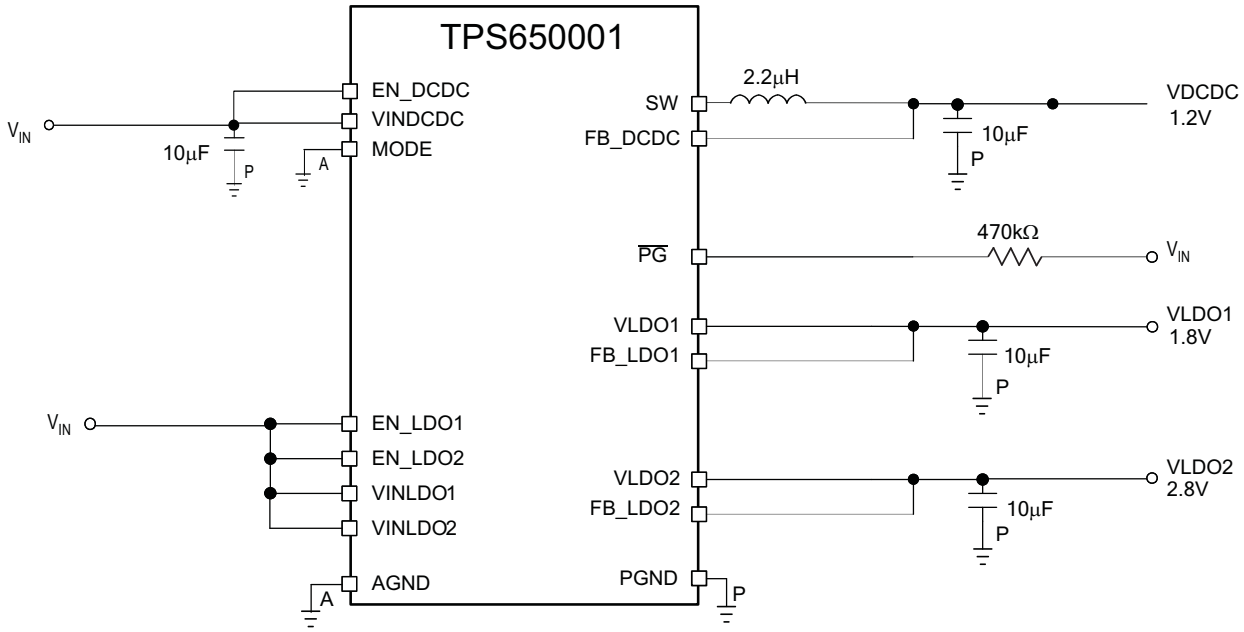


Figure 32. Typical TPS650001 Application Schematic

Table 6. Design Parameters

RESOURCES	VOLTAGE
SW	1.2 V
VLDO1	3.3 V
VLDO2	1.8 V

10.2.4 Typical TPS650061 Application

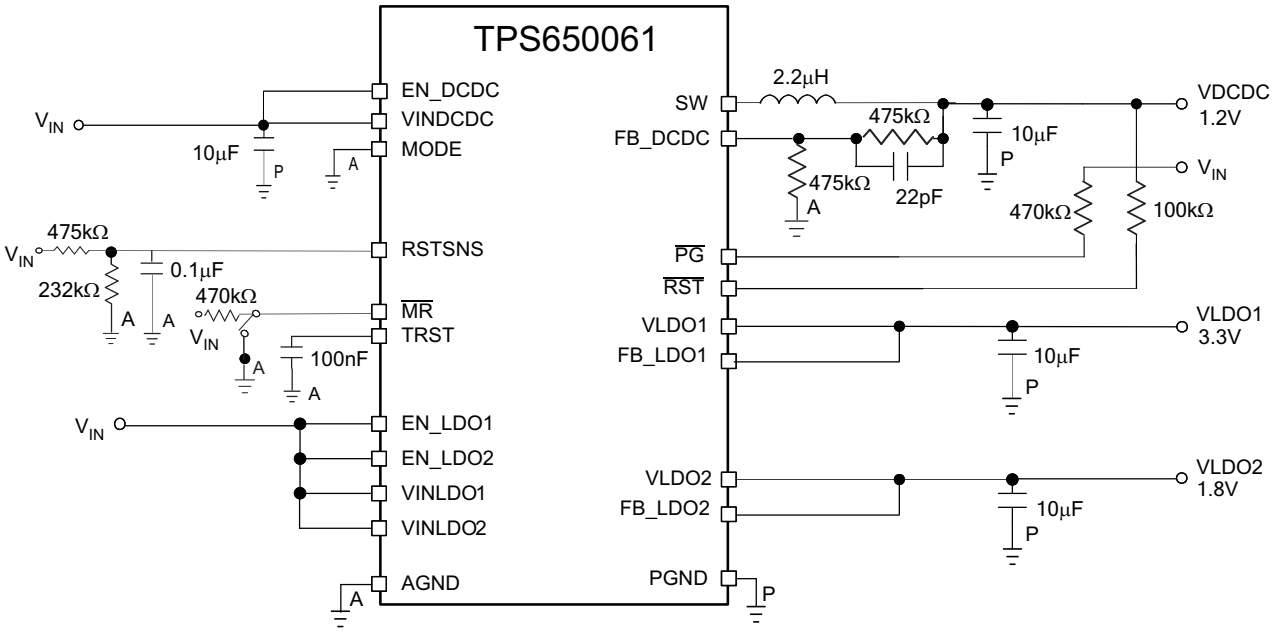


Figure 33. Typical TPS650061 Application Schematic

10.2.4.1 Design Requirements

For this design example, use the parameters listed in Table 7.

Table 7. Design Parameters

RESOURCES	VOLTAGE
SW	1.2 V
VLDO1	3.3 V
VLDO2	1.8 V

11 Power Supply Recommendations

The device is designed to operate with an input voltage supply range from 1.6 V to 6 V. This input supply can be from a DC supply, or other externally regulated supply. If the input supply is located more than a few inches from the TPS65000, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 10 µF is a typical choice.

12 Layout

12.1 Layout Guidelines

- The VINDCDC and VINLDOx pins must be bypassed to ground with a low-ESR ceramic bypass capacitor. TI recommends the typical bypass capacitance is 10 µF and 2.2 µF with a X5R dielectric.
- The optimum placement is closest to the VINDCDCx and VINLDOx pins of the device. Minimize the loop area formed by the bypass capacitor connection, the VINDCDC and VINLDO pins, and the thermal pad of the device.
- The thermal pad must be tied to the PCB ground plane with multiple vias.
- The VLDOx and VDCDCx pins (feedback pins) traces must be routed away from any potential noise source to avoid coupling.
- VODC output capacitance must be placed immediately at the VODC pin. Excessive distance between the capacitance and DCDCx pin may cause poor converter performance.
- AGND star back to PGND as close to IC as possible.
- DGND connect to thermal pad.

12.2 Layout Example

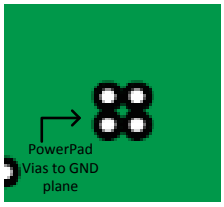


Figure 34. Layout Recommendation

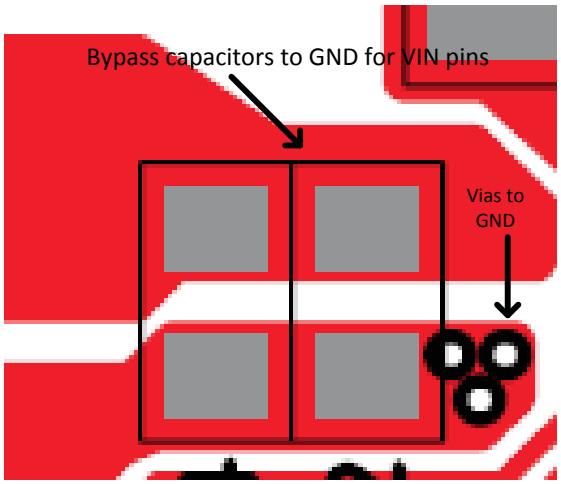


Figure 35. Bypass Capacitor and Via Placement Recommendation

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- *Choosing Inductors and Capacitors for DC/DC Converters*, SLVA157
- *High Efficiency Power Solution for TMS32C2834x MCU*, SLDA039
- *Power for TMS320C5504/05*, SLVA401
- *Power for OMAP-L13x*, SLYT405

13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS65000	Click here	Click here	Click here	Click here	Click here
TPS65001	Click here	Click here	Click here	Click here	Click here
TPS650001	Click here	Click here	Click here	Click here	Click here
TPS650003	Click here	Click here	Click here	Click here	Click here
TPS650006	Click here	Click here	Click here	Click here	Click here
TPS650061	Click here	Click here	Click here	Click here	Click here

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS650001RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAG	Samples
TPS650001RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAG	Samples
TPS650003RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAH	Samples
TPS650003RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAH	Samples
TPS650006RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	DAI	Samples
TPS650006RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAI	Samples
TPS65000RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CFO	Samples
TPS65000RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CFO	Samples
TPS65001RUKR	ACTIVE	WQFN	RUK	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CFQ	Samples
TPS65001RUKT	ACTIVE	WQFN	RUK	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CFQ	Samples
TPS650061RUKR	ACTIVE	WQFN	RUK	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAJ	Samples
TPS650061RUKT	ACTIVE	WQFN	RUK	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS65000 :

- Automotive: TPS65000-Q1

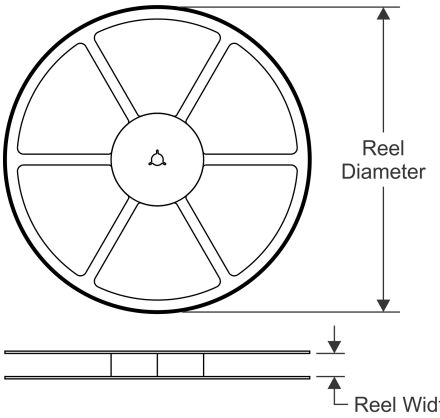
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

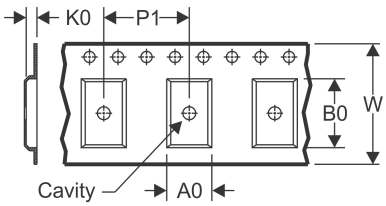
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

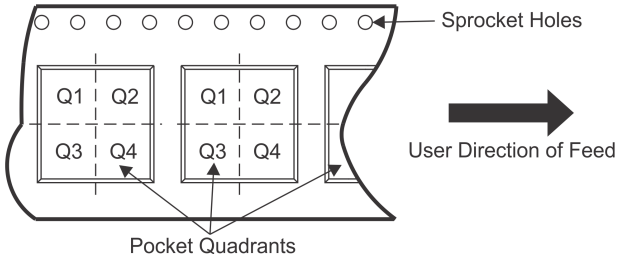


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

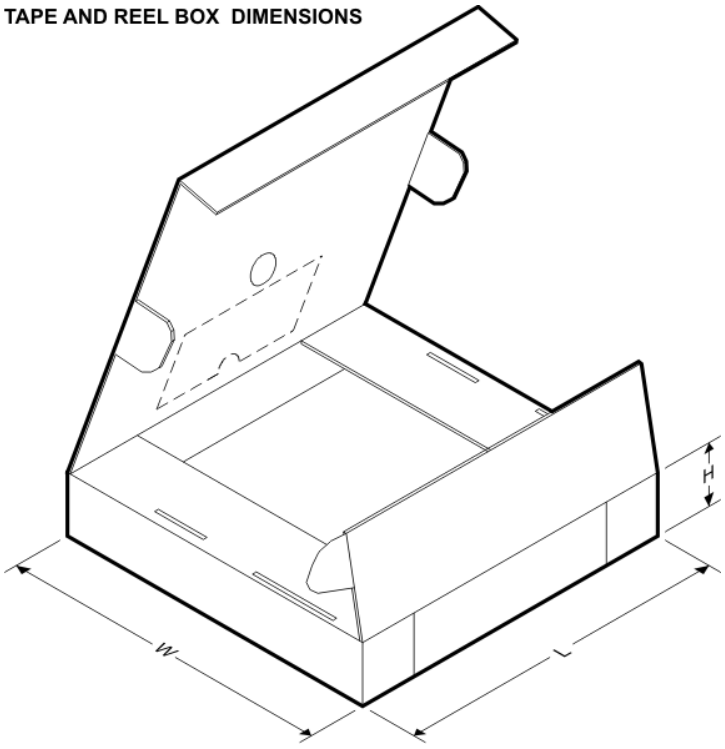


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS650001RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS650001RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS650003RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS650003RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS650006RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS650006RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65000RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65000RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65001RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65001RUKT	WQFN	RUK	20	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS650061RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS650061RUKT	WQFN	RUK	20	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

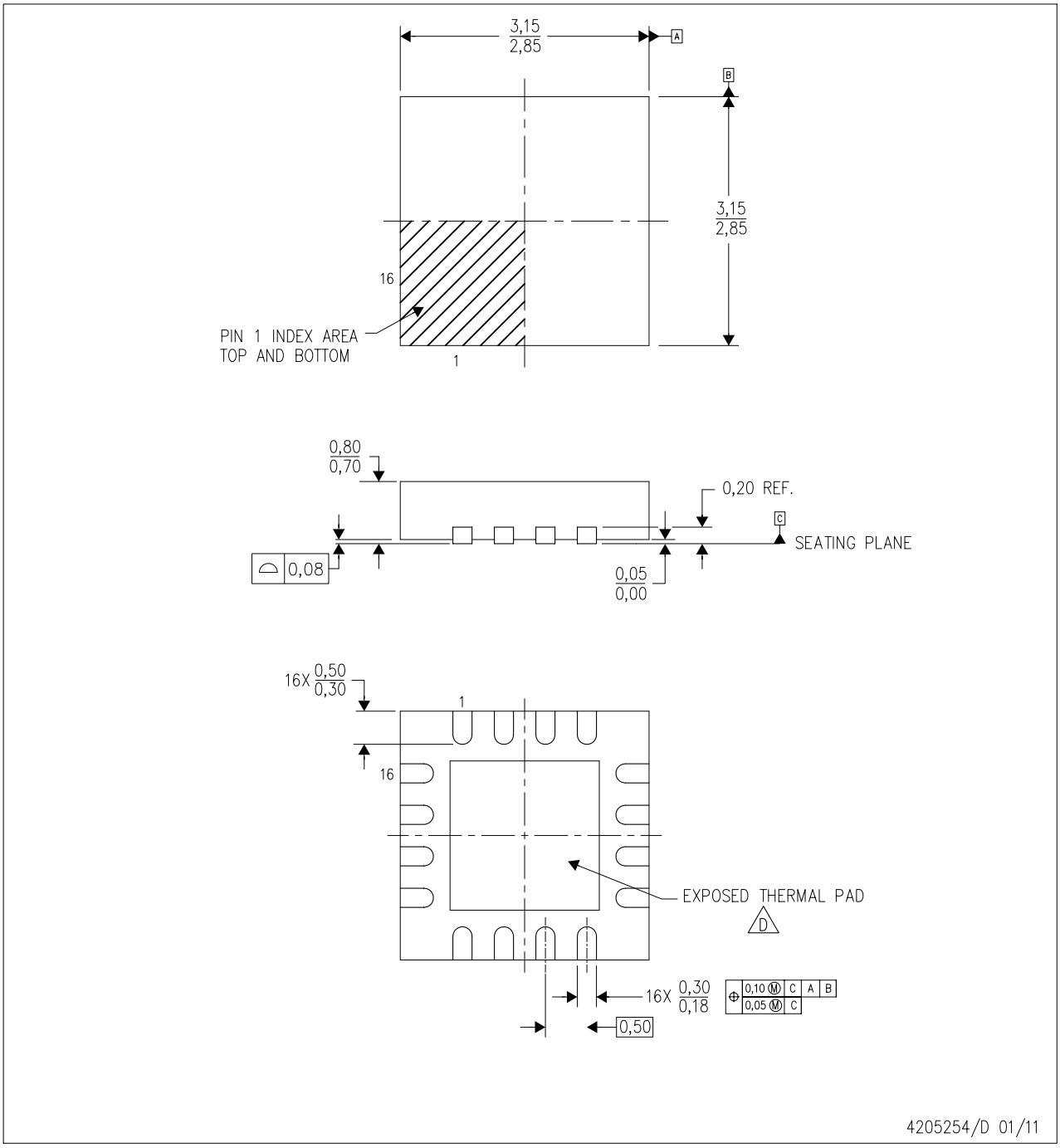


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS650001RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS650001RTET	WQFN	RTE	16	250	210.0	185.0	35.0
TPS650003RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS650003RTET	WQFN	RTE	16	250	210.0	185.0	35.0
TPS650006RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS650006RTET	WQFN	RTE	16	250	210.0	185.0	35.0
TPS65000RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS65000RTET	WQFN	RTE	16	250	210.0	185.0	35.0
TPS65001RUKR	WQFN	RUK	20	3000	367.0	367.0	35.0
TPS65001RUKT	WQFN	RUK	20	250	210.0	185.0	35.0
TPS650061RUKR	WQFN	RUK	20	3000	367.0	367.0	35.0
TPS650061RUKT	WQFN	RUK	20	250	210.0	185.0	35.0

MECHANICAL DATA

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

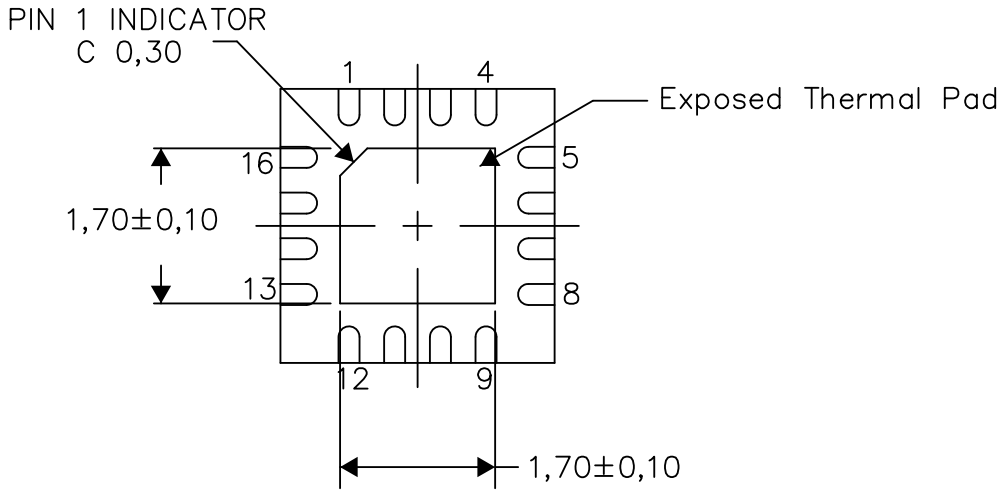
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

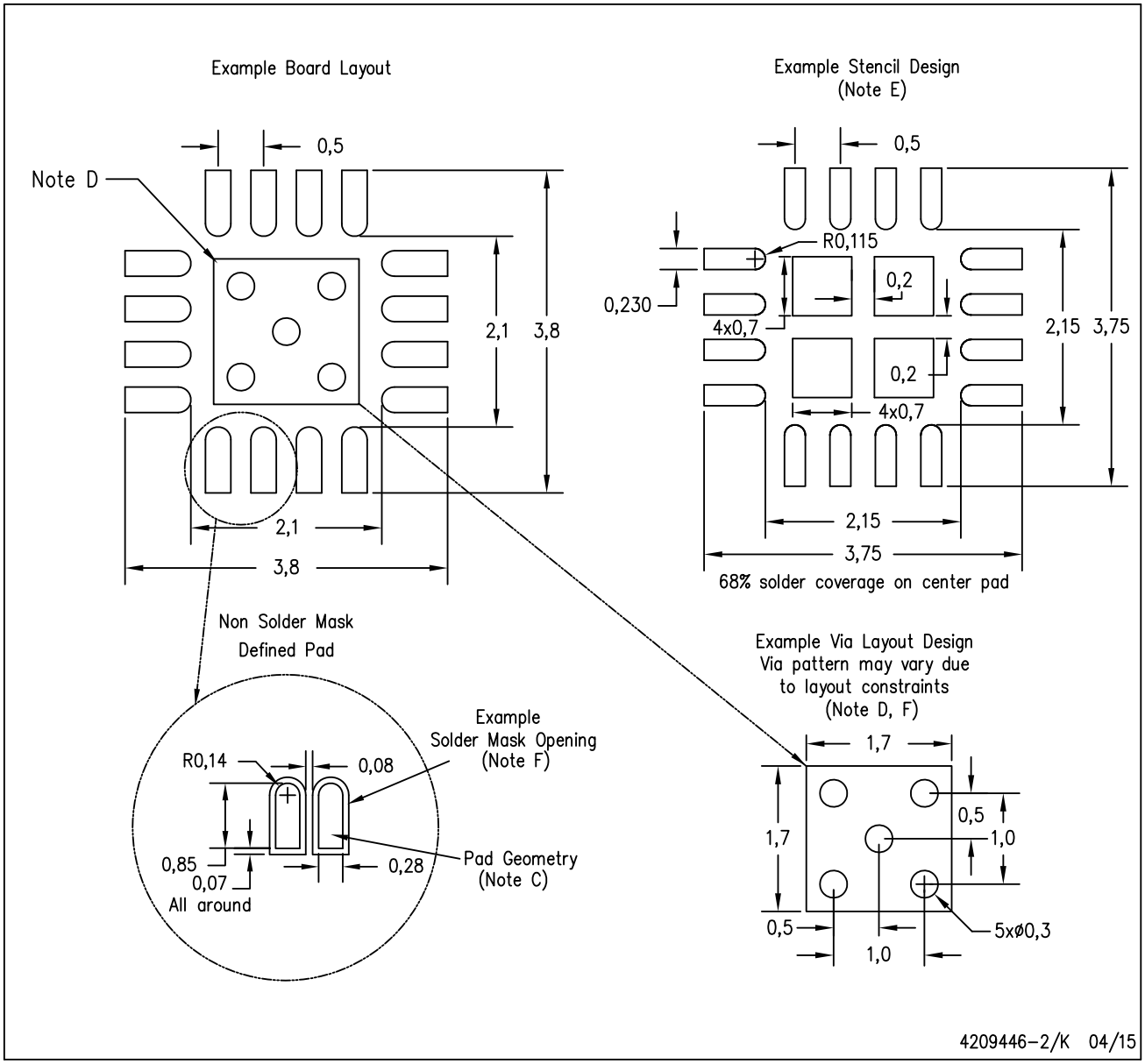
Exposed Thermal Pad Dimensions

4206446–3/U 08/15

NOTE: A. All linear dimensions are in millimeters

LAND PATTERN DATA

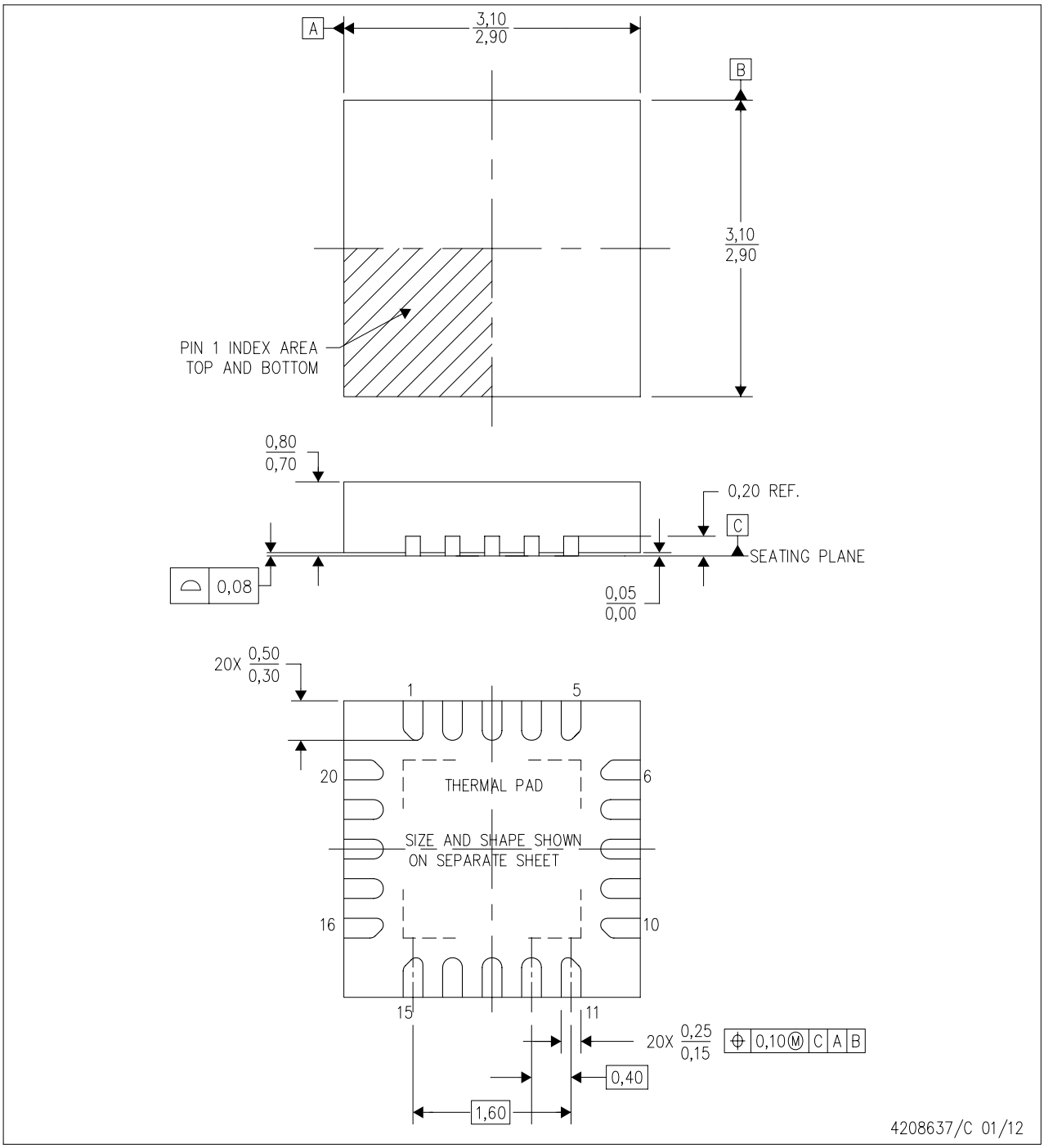
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

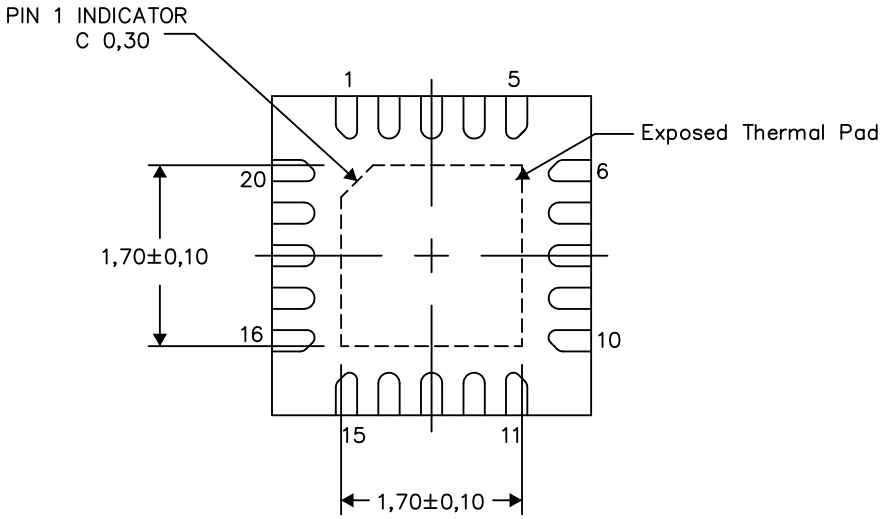
RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

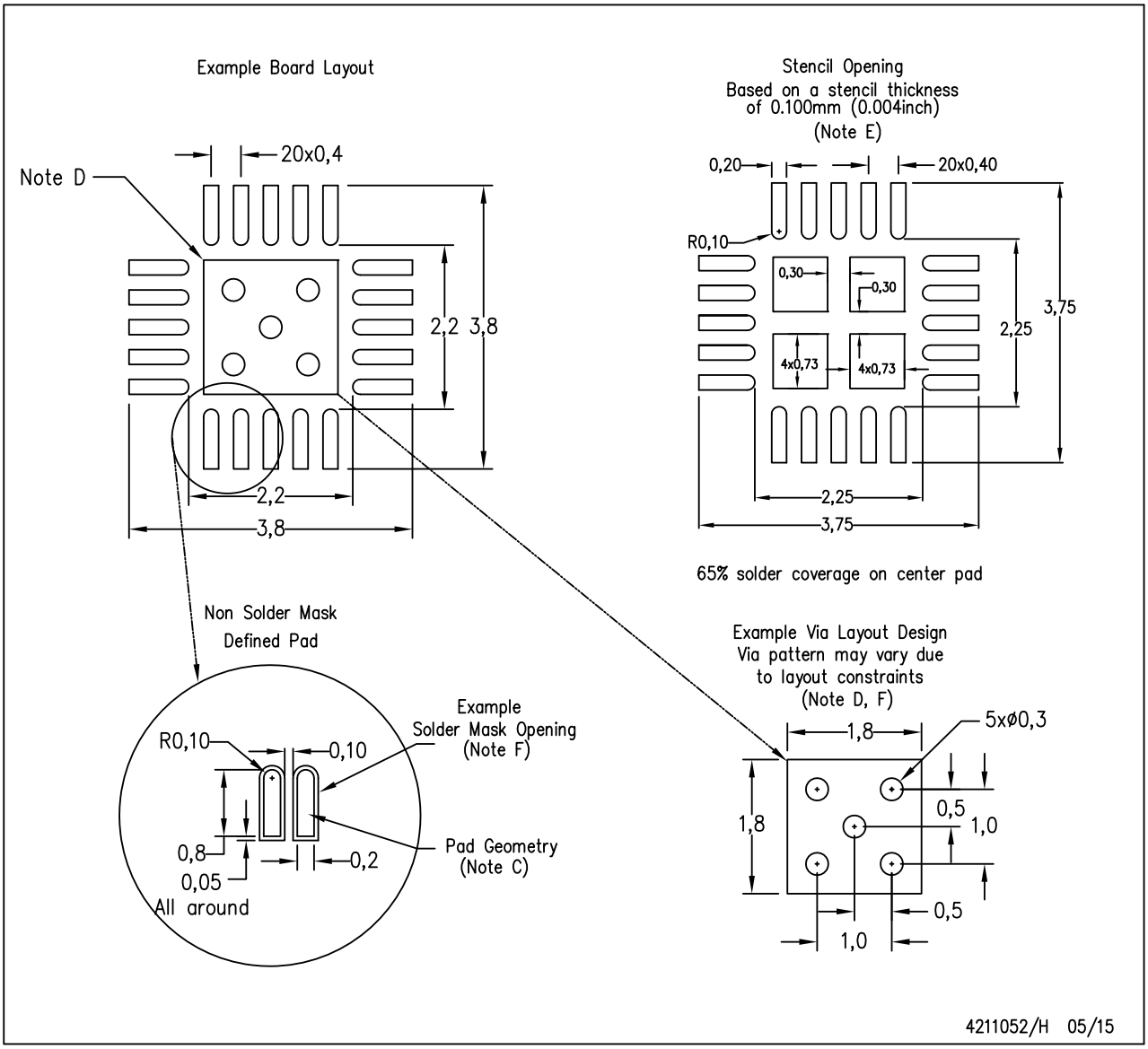
Exposed Thermal Pad Dimensions

4209762/I 05/15

NOTE: All linear dimensions are in millimeters

LAND PATTERN DATA

RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
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