# Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

Texas Instruments
TPS65192RHDR

For any questions, you can email us directly:
sales@integrated-circuit.com

Distributor of Texas Instruments: Excellent Integrated System Limited
Datasheet of TPS65192RHDR - IC LEVEL SHIFTER 9CH 28VQFN
Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com



# 9-Channel Level Shifter With Gate Voltage Shaping and Discharge Functions

## FEATURES

- **9-Channel Level Shifter Supports 6 × CLK, VST, ODD, and EVEN Signals**
- **Organized as Two Groups of 7 + 2 Channels**
- **Separate Positive Supplies ($V_{GHX}$) for Each Group**
- **$V_{GHX}$ Levels up to 38V**
- **$V_{GL}$ Levels Down to –13V**
- **Panel DISCHARGE Function**
- **Suitable for 4-Phase and 6-Phase Applications**
- **Gate Voltage Shaping on Channels 1 to 6**
- **Supports Single and Multiple Flicker Clocks**
- **Peak Output Currents greater than 500mA**
- **28-Pin 5×5 mm QFN Package**

## APPLICATIONS

- **LCD Displays Using Gate-in-Panel (GIP) Technology**

## DESCRIPTION

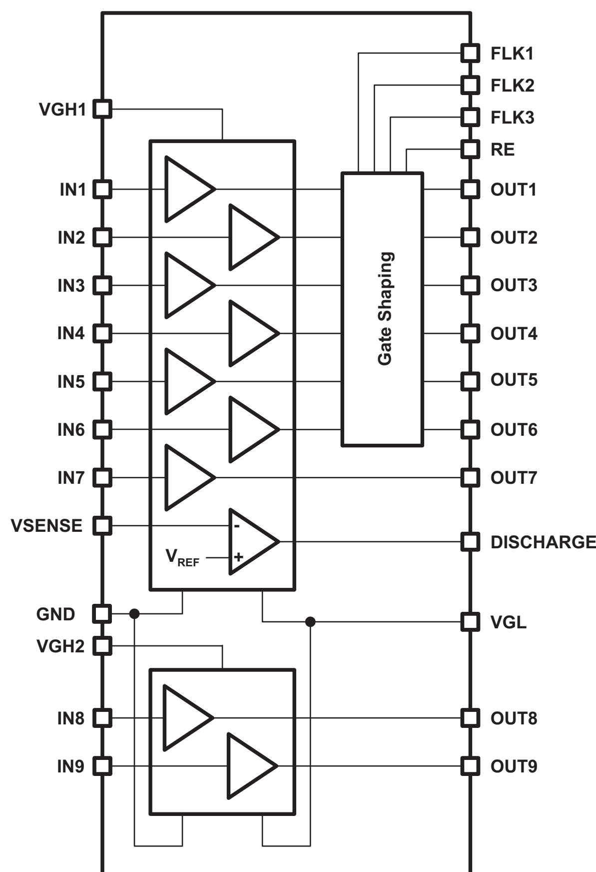
The TPS65192 is a 9 channel level-shifter intended for use in LCD display applications such as TVs and monitors. The device converts the logic-level signals generated by the Timing Controller (T-CON) to the high-level signals used by the display panel.

The 9 level shifter channels are organized as two groups. Channels 1 through 7 are powered from $V_{GH1}$ and $V_{GL}$, and channels 8 and 9 are powered from $V_{GH2}$ and $V_{GL}$. Each level-shifter channel features low impedance output stages that achieve fast rise and fall times even when driving the capacitive loading typically present in LCD display applications.

Level shifter channels 1 through 6 support gate voltage shaping, which can be used to improve picture quality by reducing image sticking. Novel decoding logic enables a single flicker clock signal to control gate voltage shaping for all CLK channels without the need for synchronization. The device also supports the use of multiple flicker clocks. The rate of decay is set by an external resistor or resistor network connected to the RE pin.

A tenth level shifter channel specially configured with a comparator input stage allows designers to implement panel discharging during power-down.

## BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2009, Texas Instruments Incorporated

Distributor of Texas Instruments: Excellent Integrated System Limited
Datasheet of TPS65192RHDR - IC LEVEL SHIFTER 9CH 28VQFN
Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION(1)

| $T_A$ | ORDERING | PACKAGE | PACKAGE MARKING |
|---|---|---|---|
| –40°C to 85°C | TPS65192RHDR | 28-Pin QFN | TPS65192 |

(1) The device is supplied taped and reeled, with 3000 devices per reel.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

| | | VALUE | UNIT |
|---|---|---|---|
| Supply voltage (2) | VGH1, VGH2 | –0.3 to 45 | V |
| | VGL | 0.3 to –15 | V |
| Input voltage(2) | IN1 through IN9, VSENSE, FLK1, FLK2, FLK3 | –0.3 to 7.0 | V |
| | RE | –0.3 to 45 | V |
| Output current | RE | 0.1 | A |
| ESD rating | HBM | 2 | kV |
| | MM | 200 | V |
| | CDM | 700 | V |
| Continuous power dissipation | | See Dissipation Rating Table | |
| Operating ambient temperature range | | –40 to 85 | °C |
| Operating junction temperature range | | –40 to 150 | °C |
| Storage temperature range | | –65 to 150 | °C |
| Lead temperature (soldering, 10 sec) | | 300 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND pin.

## DISSIPATION RATINGS

| PACKAGE | $\theta_{JA}$ | $T_A \leq 25°C$ POWER RATING | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| 28-Pin QFN(1) | 35°C/W | 3.57W | 2.29W | 1.86W |

(1) This data is based on using a JEDEC High-K board with the exposed die pad connected to a Cu pad on the board connected to the ground plane by a 2x3 thermal via matrix.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{GH1}$, $V_{GH2}$ | Positive supply voltage range | 12 | 30 | 38 | V |
| $V_{GL}$ | Negative supply voltage range | –13 | –7 | –2 | V |
| $T_A$ | Operating ambient temperature | –40 | | 85 | °C |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

 Copyright © 2009, Texas Instruments Incorporated

## ELECTRICAL CHARACTERISTICS

$V_{GH1} = V_{GH2} = 30V$; $V_{GL} = –7$ V; $T_A = –40°C$ to 85°C; typical values are at 25°C (unless otherwise noted).

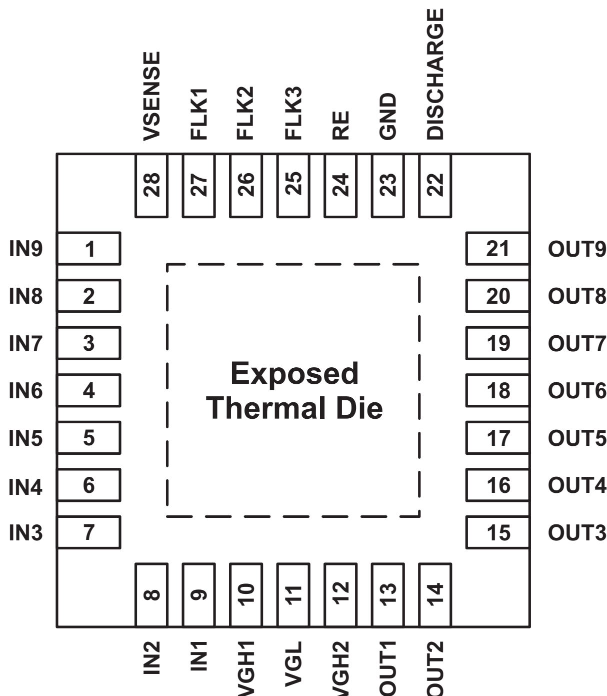
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $I_{GH1}$ | $V_{GH1}$ Supply current | IN1 to IN7 = GND; $V_{SENSE}$ = 0V | | 0.35 | 3 | mA |
| $I_{GH2}$ | $V_{GH2}$ Supply current | IN8 and IN9 = GND; $V_{SENSE}$ =0V | | 0.012 | 1 | mA |
| $I_{GL}$ | $V_{GL}$ Supply current | IN1 to IN9 = GND; $V_{SENSE}$ = 0V | | 0.144 | 4 | mA |
| $V_{UVLO}$ | Undervoltage lockout threshold | $V_{GH1}$ rising | 10.5 | | 13.5 | V |
| $V_{HYS}$ | Undervoltage lockout hysteresis | $V_{GH1}$ falling | | 450 | | mV |
| **LEVEL SHIFTERS** | | | | | | |
| $I_{OUTX}$ | Output current | Continuous; OUT1 to OUT7 | ±15 | | | mA |
| | | Peak; OUT1 to OUT7 | ±300 | ±650 | | |
| | | Continuous; OUT8 and OUT9, DISCHARGE | ±15 | | | mA |
| | | Peak; OUT8 an OUT9, DISCHARGE | ±150 | ±250 | | |
| $I_{INX}$ | Input current | IN1 to IN9 = GND | | | ±1 | µA |
| | | IN1 to IN9 = 3.3 V | | | ±1 | |
| $V_{IH}$ | High level input voltage | IN1 to IN9 | | | 2.0 | V |
| $V_{IL}$ | Low level input voltage | IN1 to IN9 | 0.5 | | | V |
| $V_{DROPH}$ | Output voltage drop high | OUT1 to OUT7; $I_{LOAD}$ = 10 mA | | 0.12 | 0.4 | V |
| | | OUT8 and OUT9, DISCHARGE; $I_{LOAD}$ = 10 mA | | 0.36 | 1.0 | |
| $V_{DROPL}$ | Output voltage drop low | OUT1 to OUT7; $I_{LOAD}$ = –10 mA | | 0.07 | 0.3 | V |
| | | OUT8 and OUT9, DISCHARGE; $I_{LOAD}$ = –10 mA | | 0.17 | 1.0 | |
| $t_R$ | Rise time | OUT1 to OUT7; $C_{LOAD}$ = 4.7 nF (1) | | 275 | 520 | ns |
| | | OUT8 and OUT9; $C_{LOAD}$ = 4.7 nF (1) | | 761 | 1000 | |
| $t_F$ | Fall time | OUT1 to OUT7; $C_{LOAD}$ = 4.7nF (1) | | 220 | 370 | ns |
| | | OUT8 and OUT9; $C_{LOAD}$ = 4.7 nF (1) | | 526 | 850 | |
| $t_{PH}$ | Propagation delay | Rising edge, $C_L$ = 150 pF | | | 60 | ns |
| $t_{PL}$ | | Falling edge, $C_L$ = 150 pF | | | 60 | |
| **GATE VOLTAGE SHAPING** | | | | | | |
| $t_{PH}$ | Propagation delay – gate voltage shaping enabled | FLK falling | | | 100 | ns |
| $t_{SU}$ | Set-up time | Time active IN signals must be stable before falling edge of FLK | | | 70 | ns |
| $r_{DS(on)}$ | Resistance between OUT and RE pins | | | 70 | 100 | Ω |
| $I_{LEAK}$ | Leakage current from RE pin | | | | ±10 | µA |
| **DISCHARGE** | | | | | | |
| $V_{SENSE}$ | Discharge voltage sense threshold | $V_{SENSE}$ falling | 1.275 | 1.5 | 1.725 | V |
| $I_{SENSE}$ | Discharge voltage sense input current | $V_{SENSE}$ = 2V | | | ±1 | µA |
| $V_{HYS}$ | Discharge voltage sense hysteresis | $V_{SENSE}$ rising | | 40 | | mV |

(1) Rise and fall times are measured between 10% and 90% of the waveform's amplitude.

Copyright © 2009, Texas Instruments Incorporated

## DEVICE INFORMATION

### PIN ASSIGNMENT




### PIN FUNCTIONS

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| IN9 | 1 | I | Level shifter channel 9 input. Connect this pin to GND, if not used. |
| IN8 | 2 | I | Level shifter channel 8 input. Connect this pin to GND, if not used. |
| IN7 | 3 | I | Level shifter channel 7 input. Connect this pin to GND, if not used. |
| IN6 | 4 | I | Level shifter channel 6 input. Connect this pin to GND, if not used. |
| IN5 | 5 | I | Level shifter channel 5 input. Connect this pin to GND, if not used. |
| IN4 | 6 | I | Level shifter channel 4 input. Connect this pin to GND, if not used. |
| IN3 | 7 | I | Level shifter channel 3 input. Connect this pin to GND, if not used. |
| IN2 | 8 | I | Level shifter channel 2 input. Connect this pin to GND, if not used. |
| IN1 | 9 | I | Level shifter channel 1 input. Connect this pin to GND, if not used. |
| VGH1 | 10 | P | Positive supply voltage for level shifter channels 1 through 7 and discharge function. Bypass this pin with a parallel combination of 10µF and 100nF ceramic capacitors. |
| VGL | 11 | P | Negative supply voltage. Bypass this pin with a parallel combination of 10µF and 100nF ceramic capacitors. |
| VGH2 | 12 | P | Positive supply voltage for level shifter channels 8 and 9. Bypass this pin with a parallel combination of 10µF and 100nF ceramic capacitors. |
| OUT1 | 13 | O | Level shifter channel 1 output. Leave this pin floating, if not used. |
| OUT2 | 14 | O | Level shifter channel 2 output. Leave this pin floating, if not used. |
| OUT3 | 15 | O | Level shifter channel 3 output. Leave this pin floating, if not used. |
| OUT4 | 16 | O | Level shifter channel 4 output. Leave this pin floating, if not used. |
| OUT5 | 17 | O | Level shifter channel 5 output. Leave this pin floating, if not used. |
| OUT6 | 18 | O | Level shifter channel 6 output. Leave this pin floating, if not used. |
| OUT7 | 19 | O | Level shifter channel 7 output. Leave this pin floating, if not used. |


Copyright © 2009, Texas Instruments Incorporated

Distributor of Texas Instruments: Excellent Integrated System Limited
Datasheet of TPS65192RHDR - IC LEVEL SHIFTER 9CH 28VQFN
Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com



## PIN FUNCTIONS (continued)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| OUT8 | 20 | O | Level shifter channel 8 output. Leave this pin floating, if not used. |
| OUT9 | 21 | O | Level shifter channel 9 output. Leave this pin floating, if not used. |
| DISCHARGE | 22 | O | Panel discharge output. Leave this pin floating, if not used. |
| GND | 23 | P | Ground. |
| RE | 24 | O | Gate voltage shaping discharge resistor connection. Leave this pin floating, if not used. |
| FLK3 | 25 | I | Gate voltage shaping flicker clock input for channels 3 and 6. Connect this pin to GND if not used. |
| FLK2 | 26 | I | Gate voltage shaping flicker clock input for channels 2 and 5. Connect this pin to GND if not used. |
| FLK1 | 27 | I | Gate voltage shaping flicker clock input for channels 1 and 4. Connect this pin to GND if not used. |
| VSENSE | 28 | I | Panel discharge voltage sense. Connect this pin to GND, if not used. |
| Exposed Thermal Die | Pad | P | Connect to VGL |

## TYPICAL CHARACTERISTICS

### TABLE OF GRAPHS

| | | FIGURE |
|---|---|---|
| Output Rise and Fall Time | Channels 1 to 7, $C_L$ = 4.7 nF, rising edge | Figure 1 |
| | Channels 1 to 7, $C_L$ = 4.7 nF, falling edge | Figure 2 |
| | Channels 8 to 9, $C_L$ = 4.7 nF, rising edge | Figure 3 |
| | Channels 8 to 9, $C_L$ = 4.7 nF, falling edge | Figure 4 |
| | Channels 1 to 7, $C_L$ = 8 pF, rising edge | Figure 5 |
| | Channels 1 to 7, $C_L$ = 8 pF, falling edge | Figure 6 |
| | Channels 8 to 9, $C_L$ = 8 pF, rising edge | Figure 7 |
| | Channels 8 to 9, $C_L$ = 8 pF, falling edge | Figure 8 |
| Propagation Delay | IN to OUT, channels 1 to 7, $C_L$ = 150 pF, rising edge | Figure 9 |
| | IN to OUT, channels 1 to 7, $C_L$ = 150 pF, falling edge | Figure 10 |
| | IN to OUT, channels 8 to 9, $C_L$ = 150 pF, rising edge | Figure 11 |
| | IN to OUT, channels 8 to 9, $C_L$ = 150 pF, falling edge | Figure 12 |
| | FLK to OUT, channels 1 to 6, $C_L$ = 150 pF, RE = 1 kΩ | Figure 13 |
| Output Current | Channels 1 to 7, $C_L$ = 10 nF | Figure 14 |
| | Channels 8 to 9, $C_L$ = 10 nF | Figure 15 |
| Panel Discharge | Power-on sequencing | Figure 16 |
| | Power-off-sequencing | Figure 17 |

Copyright © 2009, Texas Instruments Incorporated

Distributor of Texas Instruments: Excellent Integrated System Limited
Datasheet of TPS65192RHDR - IC LEVEL SHIFTER 9CH 28VQFN
Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com



OUTPUT RISE TIME
CHANNELS 1-7, $C_{OUT}$ = 4.7 nF

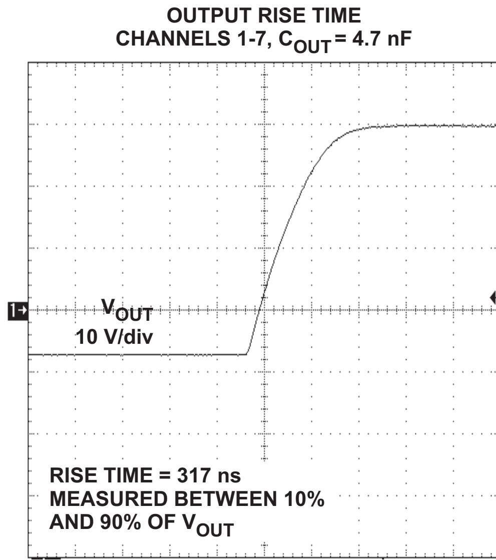



Figure 1.

OUTPUT FALL TIME
CHANNELS 1-7, $C_{OUT}$ = 4.7 nF

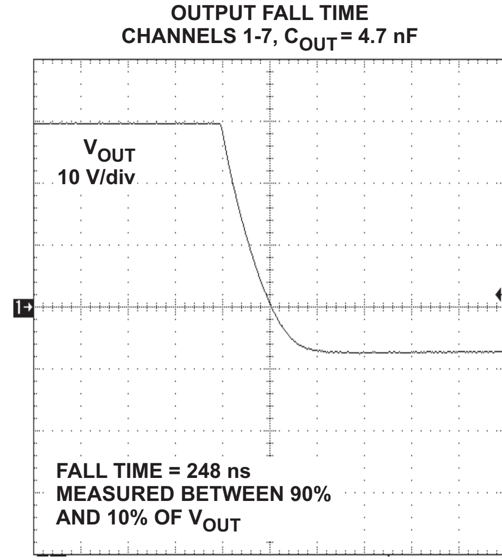



Figure 2.

OUTPUT RISE TIME
CHANNELS 8-9, $C_{OUT}$ = 4.7 nF

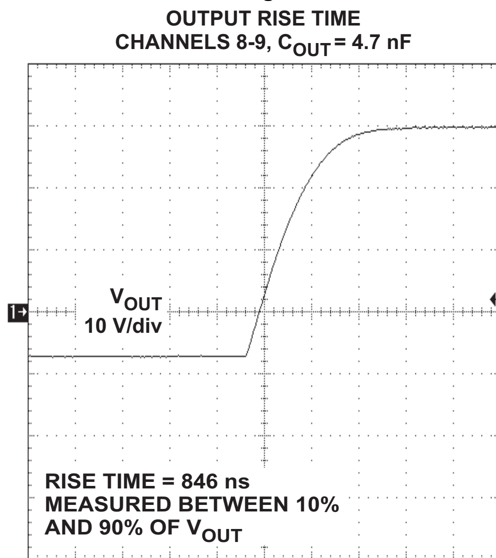



Figure 3.

OUTPUT FALL TIME
CHANNELS 8-9, $C_{OUT}$ = 4.7 nF

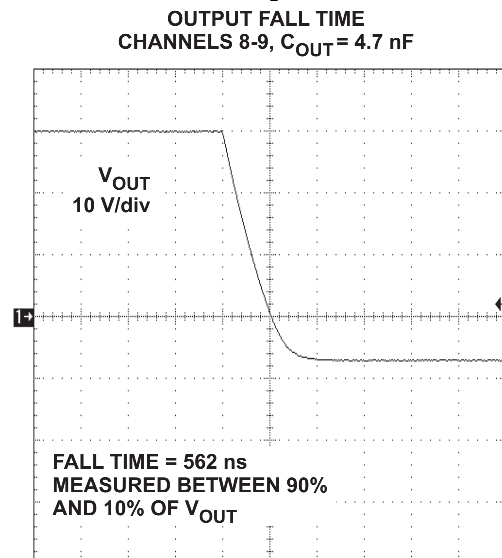



Figure 4.


Copyright © 2009, Texas Instruments Incorporated

OUTPUT RISE TIME
CHANNELS 1-7, $C_{OUT}$ = 8 pF

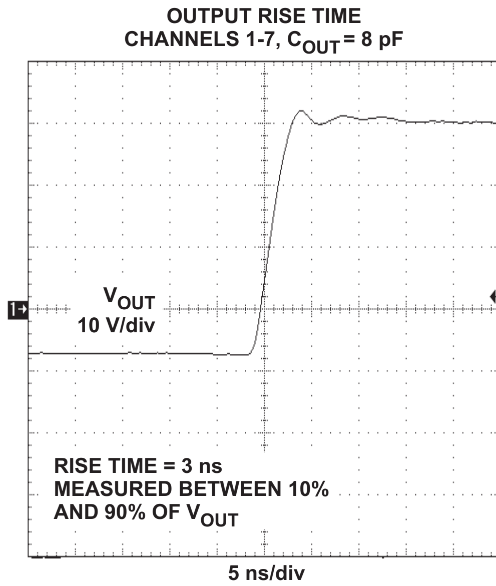



**Figure 5.**

OUTPUT FALL TIME
CHANNELS 1-7, $C_{OUT}$ = 8 pF

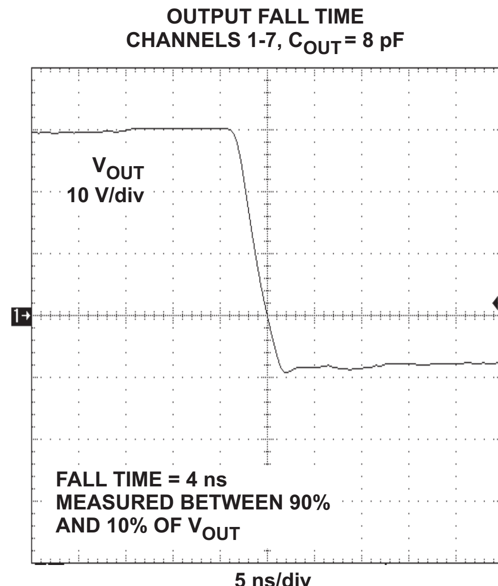



**Figure 6.**

OUTPUT RISE TIME
CHANNELS 8-9, $C_{OUT}$ = 8 pF

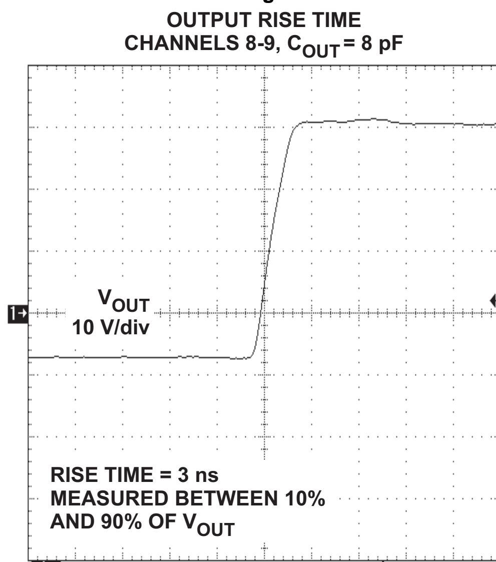



**Figure 7.**

OUTPUT FALL TIME
CHANNELS 8-9, $C_{OUT}$ = 8 pF

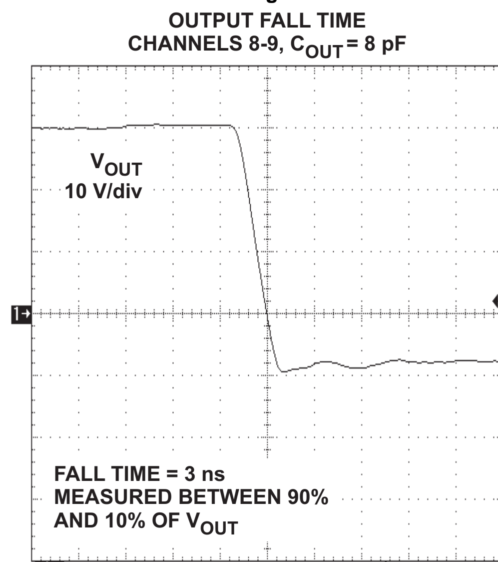



**Figure 8.**

Copyright © 2009, Texas Instruments Incorporated

OUTPUT FALL TIME
CHANNELS 8-9, $C_{OUT}$ = 8 pF

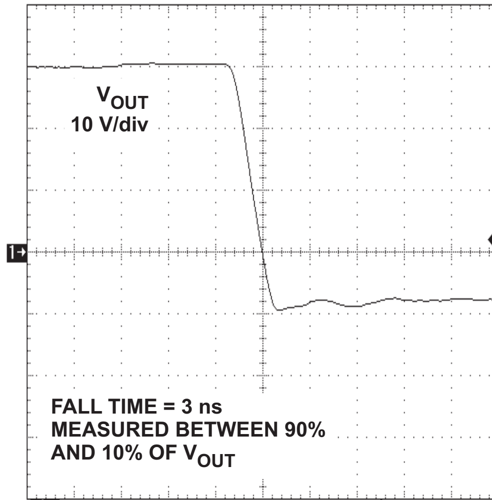



**Figure 9.**

PROPAGATION DELAY – FALLING
IN-OUT, CHANNELS 1-7, $C_{OUT}$ = 8 pF

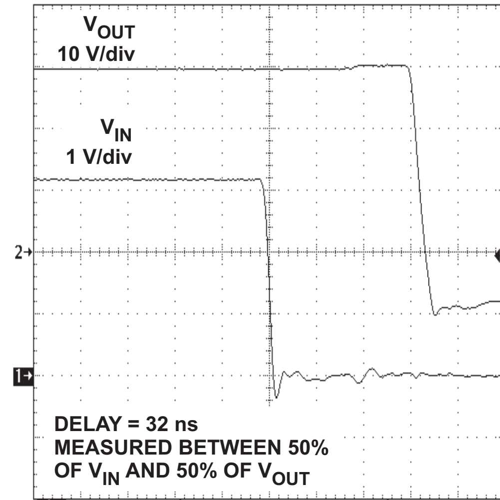



**Figure 10.**

PROPAGATION DELAY – RISING
IN-OUT, CHANNELS 8-9, $C_{OUT}$ = 8 pF

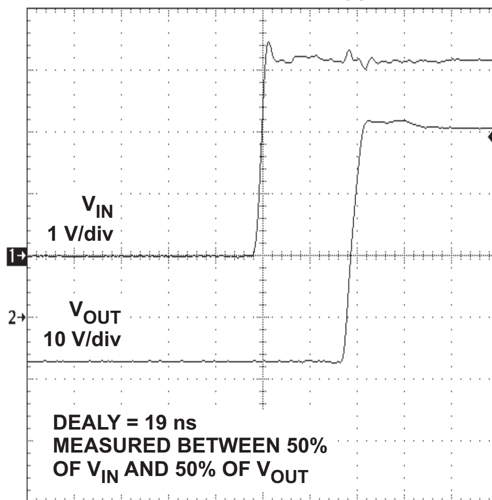



**Figure 11.**

PROPAGATION DELAY – FALLING
IN-OUT, CHANNELS 8-9, $C_{OUT}$ = 8 pF

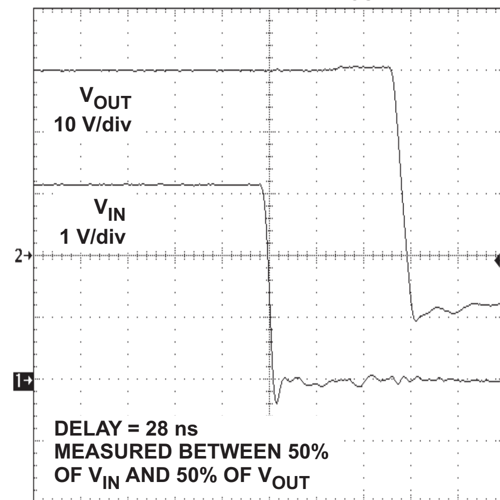



**Figure 12.**


Copyright © 2009, Texas Instruments Incorporated

Distributor of Texas Instruments: Excellent Integrated System Limited
Datasheet of TPS65192RHDR - IC LEVEL SHIFTER 9CH 28VQFN
Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com



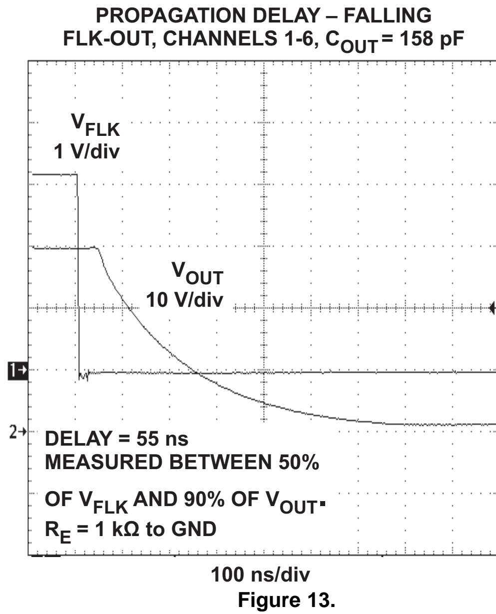



Figure 13.

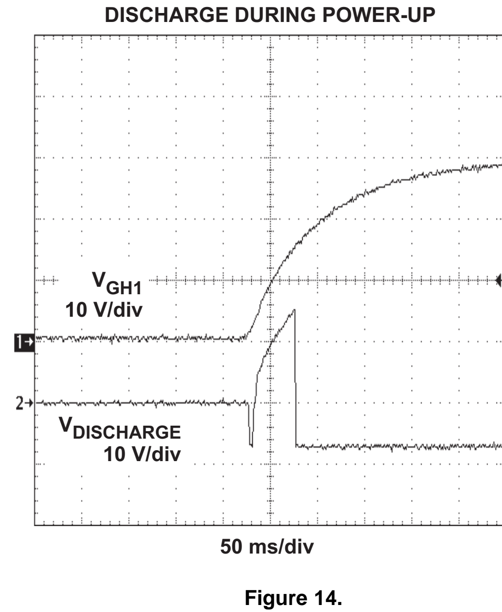



Figure 14.

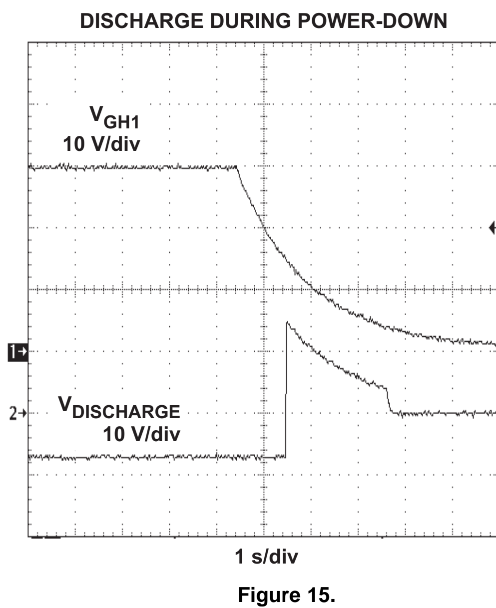



Figure 15.

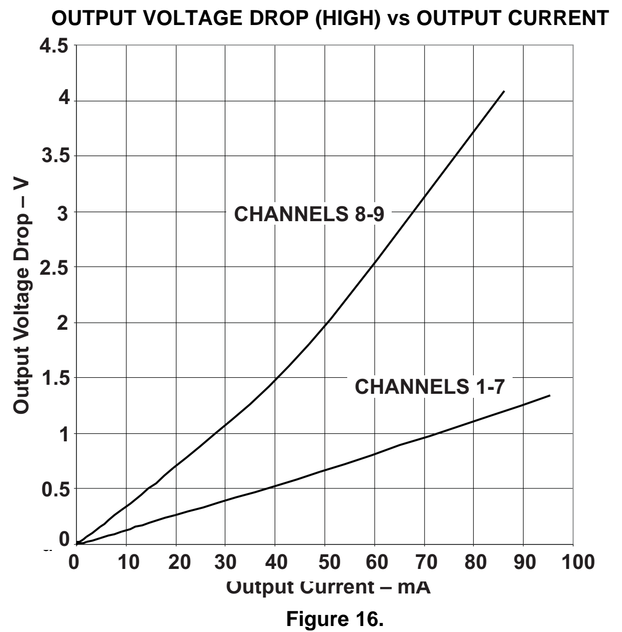



Figure 16.

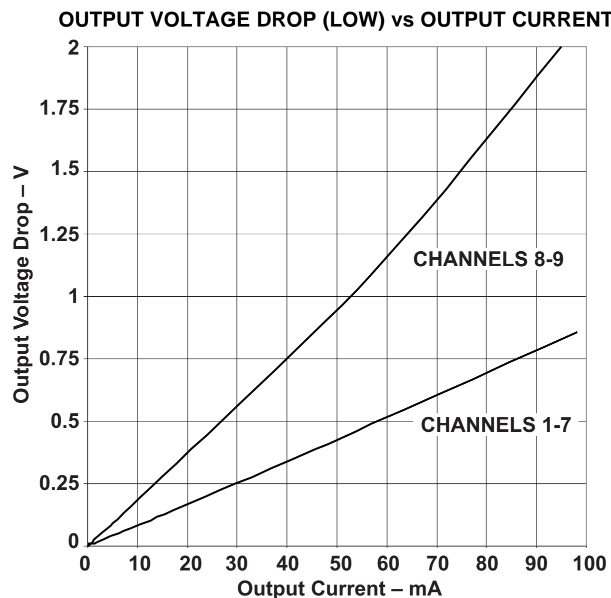



Figure 17.

# DETAILED DESCRIPTION

## LEVEL SHIFTERS

The 9 level shifter channels in the TPS65192 are divided into two groups. Channels 1 through 7 are powered from $V_{GH1}$ and $V_{GL}$, channels 8 and 9 are powered from $V_{GH2}$ and $V_{GL}$. Channels 1 to 6 support gate shaping and channels 7 through 9 do not (see the block diagram on page 1).

Figure 18 contains a simplified block diagram of one channel with gate voltage shaping.

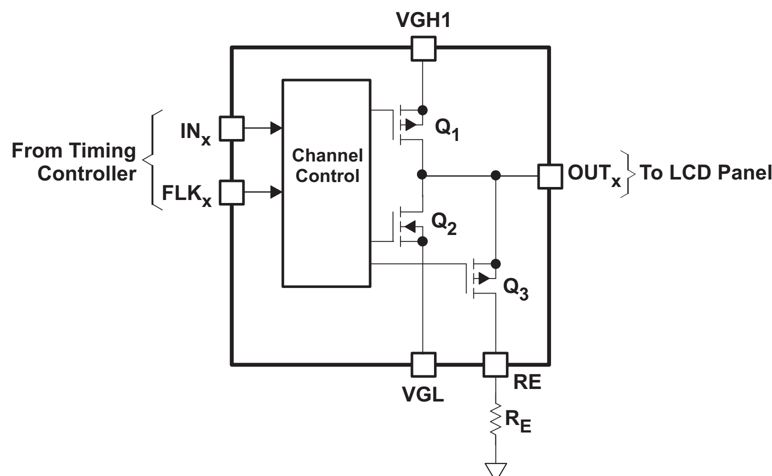



Figure 18. Level Shifter Channel With Gate Voltage Shaping

On the rising edge of IN, $Q_1$ turns on, $Q_2$ and $Q_3$ turn off, and OUT is driven to $V_{GH1}$. On the falling edge of FLK, $Q_1$ turns off, $Q_3$ is turned on, and the panel now discharges through $Q_3$ and RE (see Figure 19). On the falling edge of IN, $Q_2$ turns on and $Q_3$ turns off, and OUT is driven to $V_{GL}$. This sequence is repeated in turn for each channel.


Copyright © 2009, Texas Instruments Incorporated

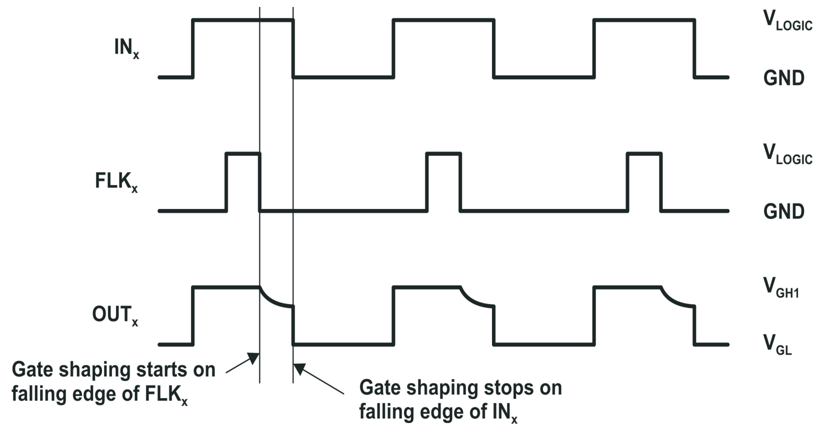



**Figure 19. Gate Voltage Shaping Timing Diagram**

The alternative configuration shown in Figure 20 can be used to define a minimum gate voltage reached during gate voltage shaping.

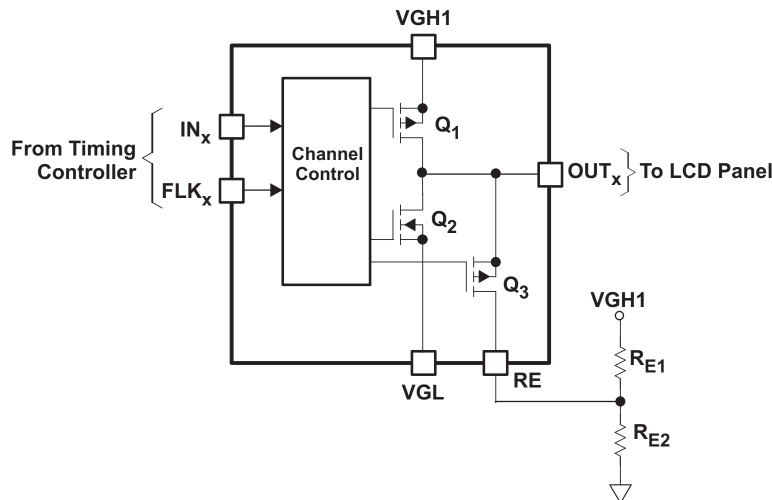



**Figure 20. Alternative Gate Voltage Shaping Circuit Configuration**

In this circuit, resistors $R_{E1}$ and $R_{E2}$ define both the rate of change of gate voltage decay and the minimum gate voltage $V_{MIN}$. Using the Thevenin equivalent, the operating parameters of Figure 20 are easily expressed as follows:

$$V_{MIN} = V_{VGH1} \times \left( \frac{R_{E2}}{R_{E1} + R_{E2}} \right)$$

$$R_E = \frac{R_{E1} \times R_{E2}}{R_{E1} + R_{E2}} \qquad (1)$$

## FLICKER CLOCKS

The gate voltage shaping control logic in the TPS65192 allows the device to be used with one, two or three flicker clock signals, according to the application requirements.

In 6-phase applications where one signal controls gate voltage shaping for six CLK channels, the flicker clock should be connected to FLK1 and the unused pins FLK2 and FLK3 connected to GND.

In 6-phase applications where three signals control gate voltage shaping for six CLK channels, the flicker clock for channels 1 and 4 should be connected to FLK1, the flicker clock for channels 2 and 5 connected to FLK2, and the flicker clock for channels 3 and 6 connected to FLK3.

In 4-phase applications where two signals control gate voltage shaping for four CLK channels, the flicker clock for phases 1 and 3 should be connected to FLK1, the flicker clock for phases 2 and 4 connected to FLK2, and the unused pin FLK3 connected to GND. The unused pins IN 3 and IN6 should be connected to $V_{LOGIC}$. Alternatively, IN3 can be connected to IN2 and IN6 connected to IN5; this arrangement can simplify PCB layout. Typical schematics for each of the above cases are included in the *Applications* section of this data sheet.

Gate voltage shaping is started by the falling edge of the FLK signal(s), which must occur during a valid part of the clock waveform. For 6-phase systems, this means the last 60° of the clock waveform; for 4-phase systems, this means the last 90° of the clock waveform (see Figure 21 and Figure 22). Falling edges of the FLK signal(s) occurring outside the valid part of the clock waveform are ignored. The rising edge of the FLK signal(s) has no effect, regardless of when it occurs.

Note that gate voltage shaping is disabled when the voltage applied to the VSENSE pin is less than $V_{REF}$.

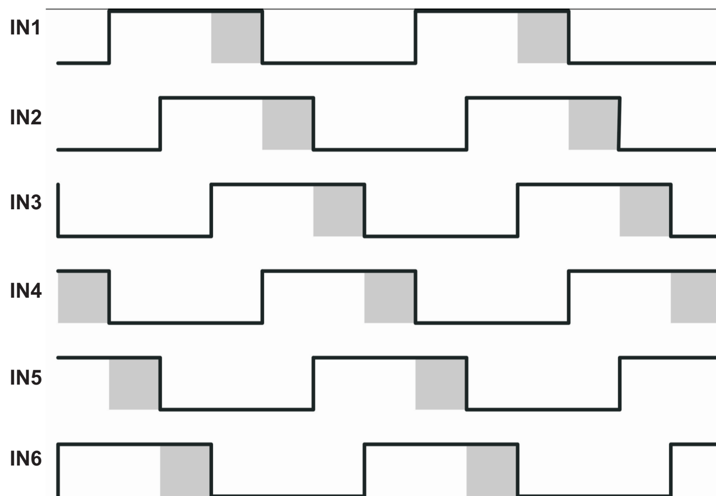



**Figure 21. FLK Falling Edge Validity, 6-Phase Applications**

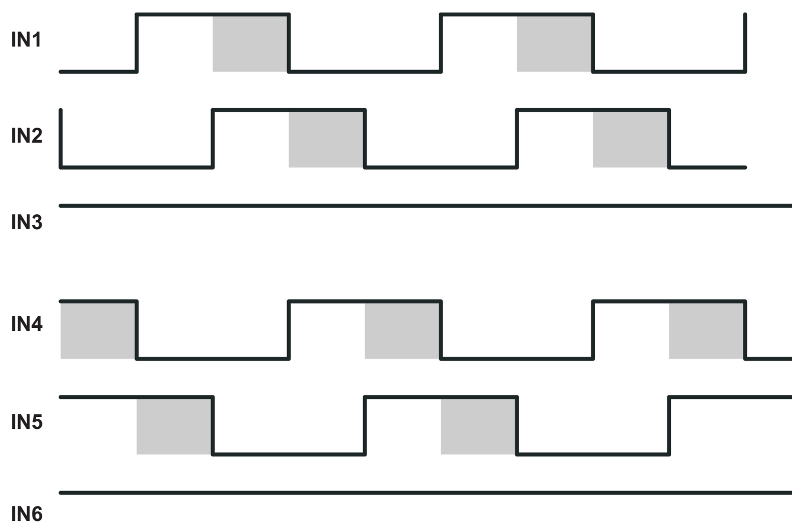



**Figure 22. FLK Falling Edge Validity, 4-Phase Applications**


Copyright © 2009, Texas Instruments Incorporated

## LEVEL SHIFTERS WITHOUT GATE VOLTAGE SHAPING

Channels 7 through 9 do not support gate voltage shaping and are controlled only by the logic level applied to their $IN_X$ pin. Figure 23 contains a block diagram of a channel that does not support gate voltage shaping.

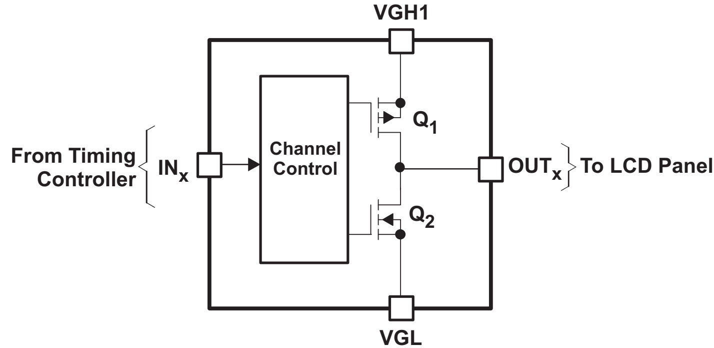



**Figure 23. Block Diagram of Level Shifter Without Gate Voltage Shaping**

## PANEL DISCHARGE

The TPS65192 contains a function for discharging the display panel during power-down. The discharge function comprises a comparator and a level shifter (see Figure 24). During normal operation, the voltage applied to the VSENSE pin is greater than $V_{REF}$, the output of the level shifter is low, and the DISCHARGE signal is at $V_{GL}$. During power-down, when the voltage applied to the VSENSE pin falls below $V_{REF}$, the level shifter output goes high and the DISCHARGE signal tracks $V_{GH1}$ as it discharges (see Figure 16 and Figure 17). Note that gate voltage shaping is disabled when the voltage applied to the VSENSE pin is less than $V_{REF}$.

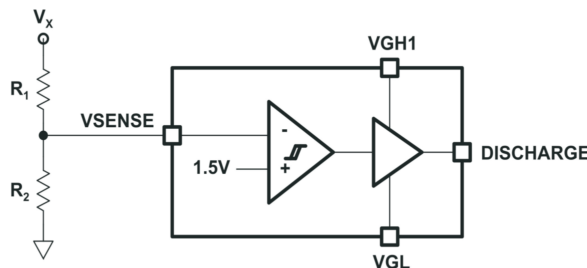



**Figure 24. Panel Discharge Function Block Diagram**

Suitable values for resistors R1 and R2 in Figure 24 can be calculated as follows:

$$R_1 = R_2 \times \left(\frac{V_X}{V_{REF}} - 1\right) = R_2 \times \left(\frac{V_X}{1.5\ V} - 1\right) \quad (2)$$

Where $V_x$ is the voltage used to activate/deactivate the discharge function.

For most applications, a value between 1kΩ and 10kΩ for $R_2$ can be used ($R_1$ depends on the value of $R_2$ and the value of $V_x$).

Distributor of Texas Instruments: Excellent Integrated System Limited
Datasheet of TPS65192RHDR - IC LEVEL SHIFTER 9CH 28VQFN
Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com



## APPLICATION INFORMATION

### Power Supply Decoupling

For proper performance, it is recommended that each power supply rail be decoupled with high quality ceramic decoupling capacitors placed as close to the IC supply pins as possible. The exact values used should be optimized for each application, but a parallel combination of 10µF and 100nF is a good place to start.

### PCB LAYOUT

The output stages of the TPS65192 are capable of sinking and sourcing high peak currents – greater than 500mA in typical applications – and care must be taken during PCB layout to ensure that this performance can be achieved in practice. In particular, the high rates of change of current occurring at the rising and falling edges of each output require stray inductance to be minimized. This is most easily achieved by routing the output signals using short, wide PCB tracks (as far as this is possible) and using a low impedance ground plane on the other side of the board to conduct return currents. Tracks between the decoupling capacitors and the corresponding power supply pins should also be kept short and wide as possible.

PCB layout must also be adequate from a thermal as well as electrical point of view. The TPS65192 is supplied in a 28-pin QFN package designed to eliminate the need for heat sinks to dissipate the power generated in the IC. The package, shown in Figure 25, is designed so that the lead-frame die pad is exposed on the bottom of the IC, thereby providing an extremely low thermal resistance path between the die and the exterior of the package ($R_{\theta JC}$).

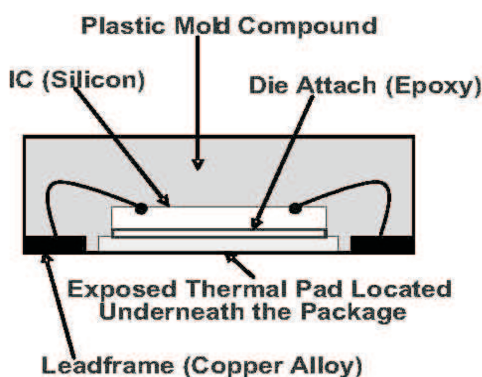



**Figure 25. Section View of a QFN Package**

Copper areas in and on a PCB act as heat sinks for the QFN device; however, signal routing typically restricts access to the power pad on the top layer of the PCB. In typical applications, therefore, the main copper area used to conduct heat away from the IC is on the bottom layer.

TI recommends placing thermal vias in the solder mask defined thermal pad to transfer heat from the top layer of the PCB to the inner or bottom layer used for heat sinking. The recommended via diameter is 0.3mm or less, and via spacing 1mm (see Figure 26). For the 5 × 5 mm QFN package used for the TPS65192, five thermal vias are typically used.


Copyright © 2009, Texas Instruments Incorporated

**Distributor of Texas Instruments: Excellent Integrated System Limited**
Datasheet of TPS65192RHDR - IC LEVEL SHIFTER 9CH 28VQFN
Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com



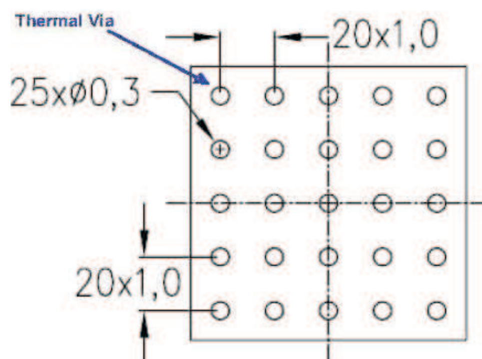



**Figure 26. Recommended Thermal Via Spacing**

The thermal vias should make their connection to the bottom (or internal) copper plane with a complete connection around the entire circumference of the plated through hole, and a ring of exposed copper (0.05mm wide) around the vias at the bottom of the copper plane. It is not recommended to cover the vias with solder mask as this can cause excessive voiding, and nor is it recommended to use a thermal relief web or spoke connection as this impedes the conduction path to the other layers (see Figure 27).

**Figure 27. Thermal Via Connection at the Bottom Layer**

In any design, the copper areas used as heat sinks should be made as large as possible.

**The power pad of the TPS65192 is electrically connected to VGL and therefore must not be connected to the PCB's ground plane.**

For more detailed information concerning the thermal performance of QFN packages and recommendations about how to mount the ICs on a PCB, refer to the following application reports:

| | |
|---|---|
| SLOA122 | *QFN Layout Guidelines* |
| SLUA271A | *QFN/SON PCB Attachment* |

Copyright © 2009, Texas Instruments Incorporated

## APPLICATION CIRCUITS

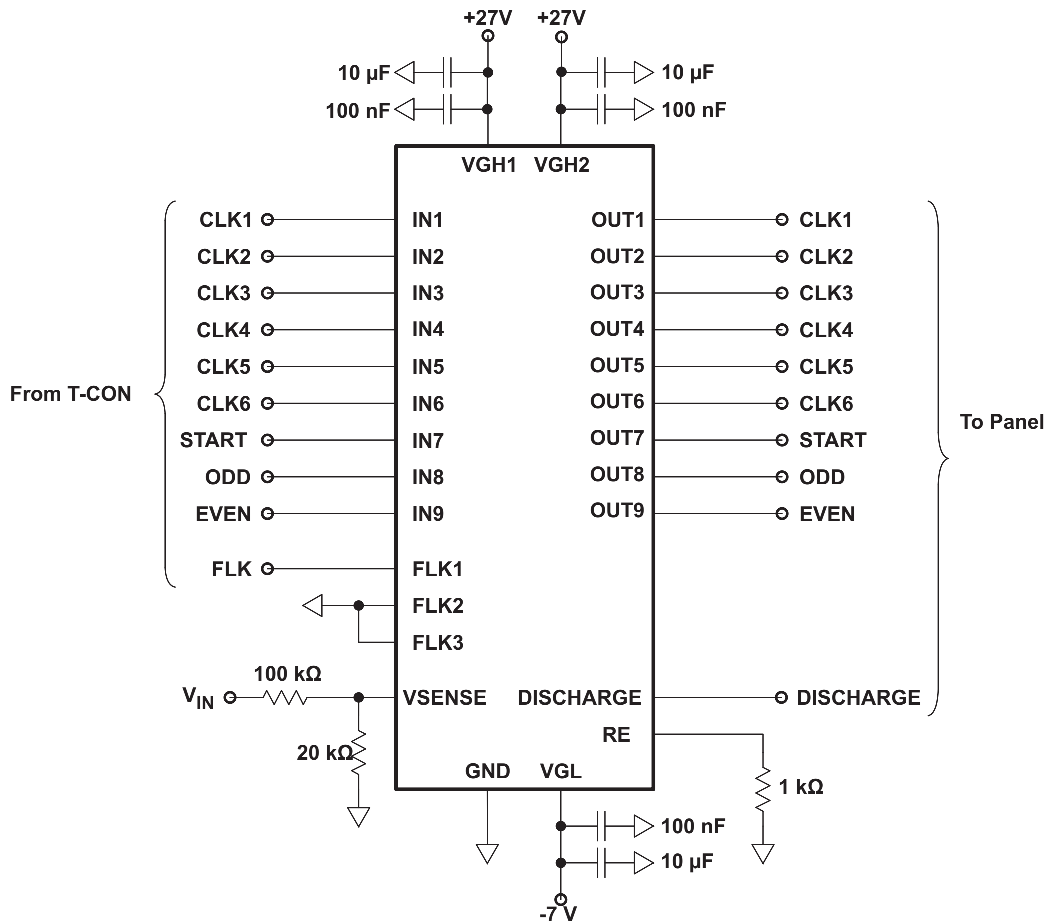



Figure 28. Typical 6-Phase HD TV Application with One Flicker Clock


Copyright © 2009, Texas Instruments Incorporated

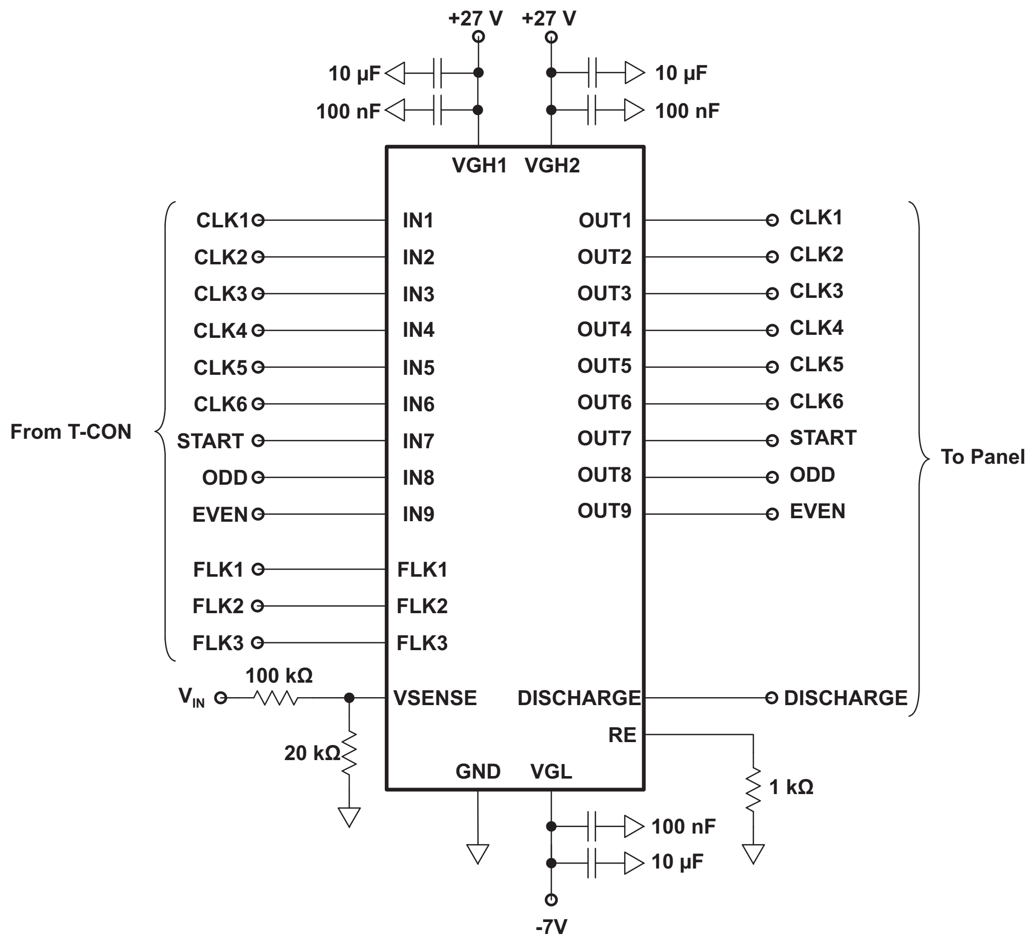



**Figure 29. Typical 6-Phase F-HD TV Application with Three Flicker Clocks**

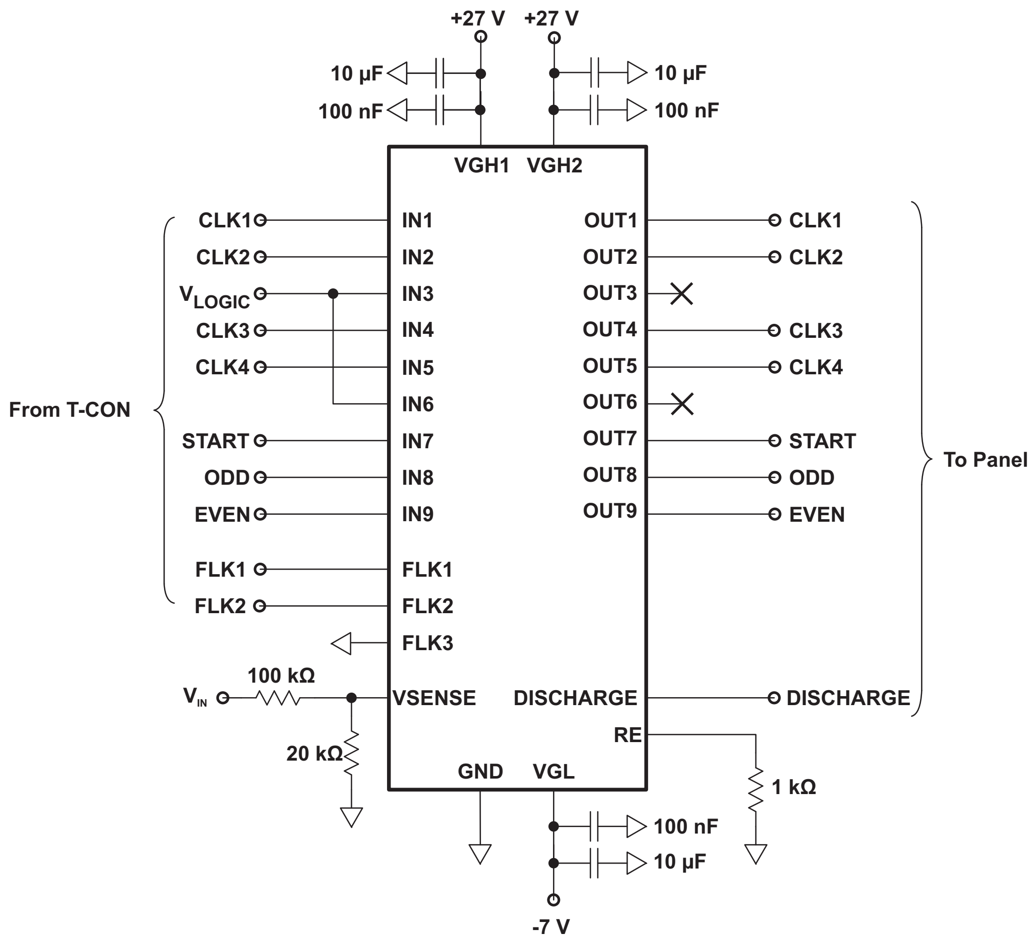



**Figure 30. Typical 4-Phase Monitor Application with Two Flicker Clocks**


Copyright © 2009, Texas Instruments Incorporated

Distributor of Texas Instruments: Excellent Integrated System Limited
Datasheet of TPS65192RHDR - IC LEVEL SHIFTER 9CH 28VQFN
Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com



## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65192RHDR | ACTIVE | VQFN | RHD | 28 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS 65192 | Samples |
| TPS65192RHDT | PREVIEW | VQFN | RHD | 28 | | TBD | Call TI | Call TI | -40 to 85 | | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

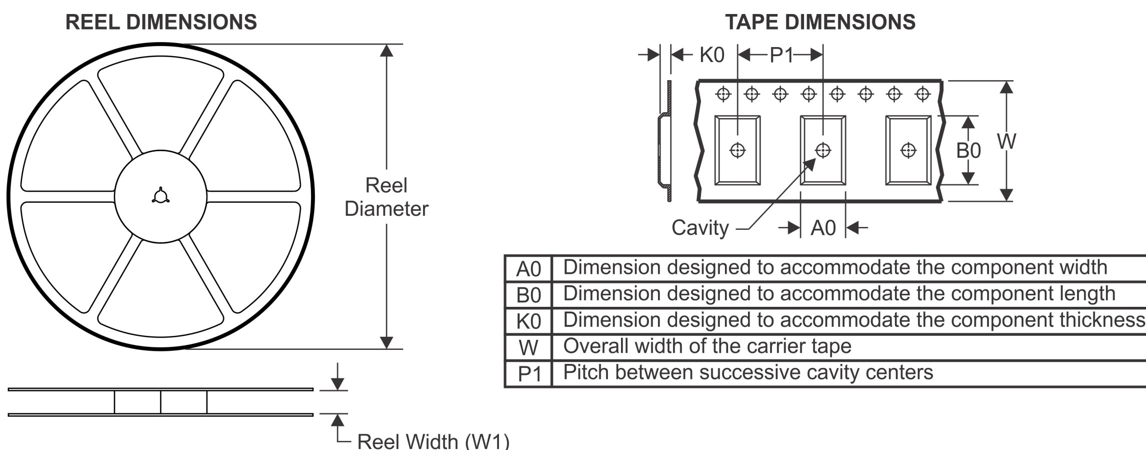
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

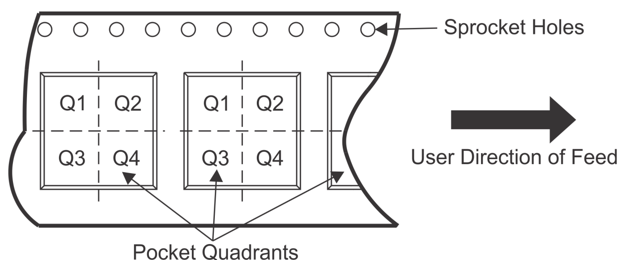
**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



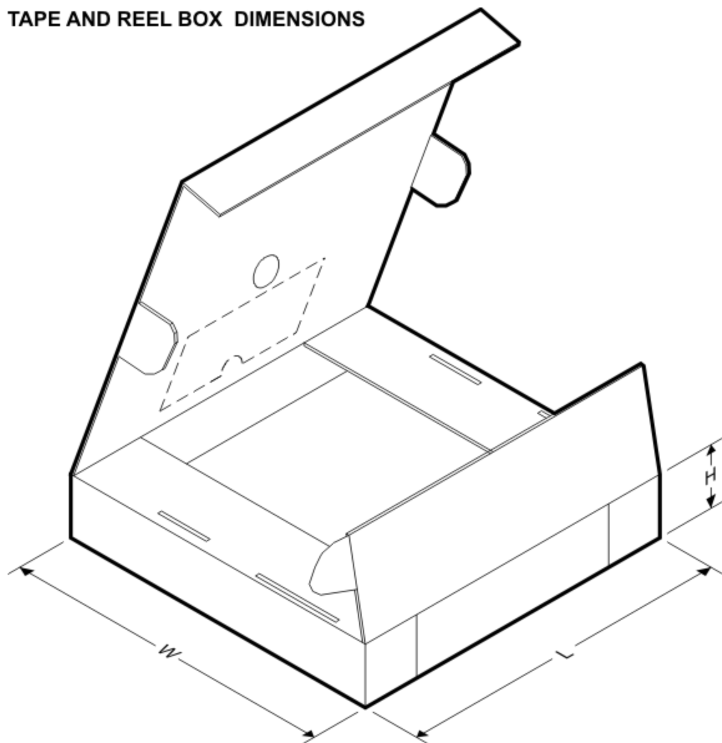

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65192RHDR | VQFN | RHD | 28 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS65192RHDR | VQFN | RHD | 28 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |

## TAPE AND REEL BOX DIMENSIONS

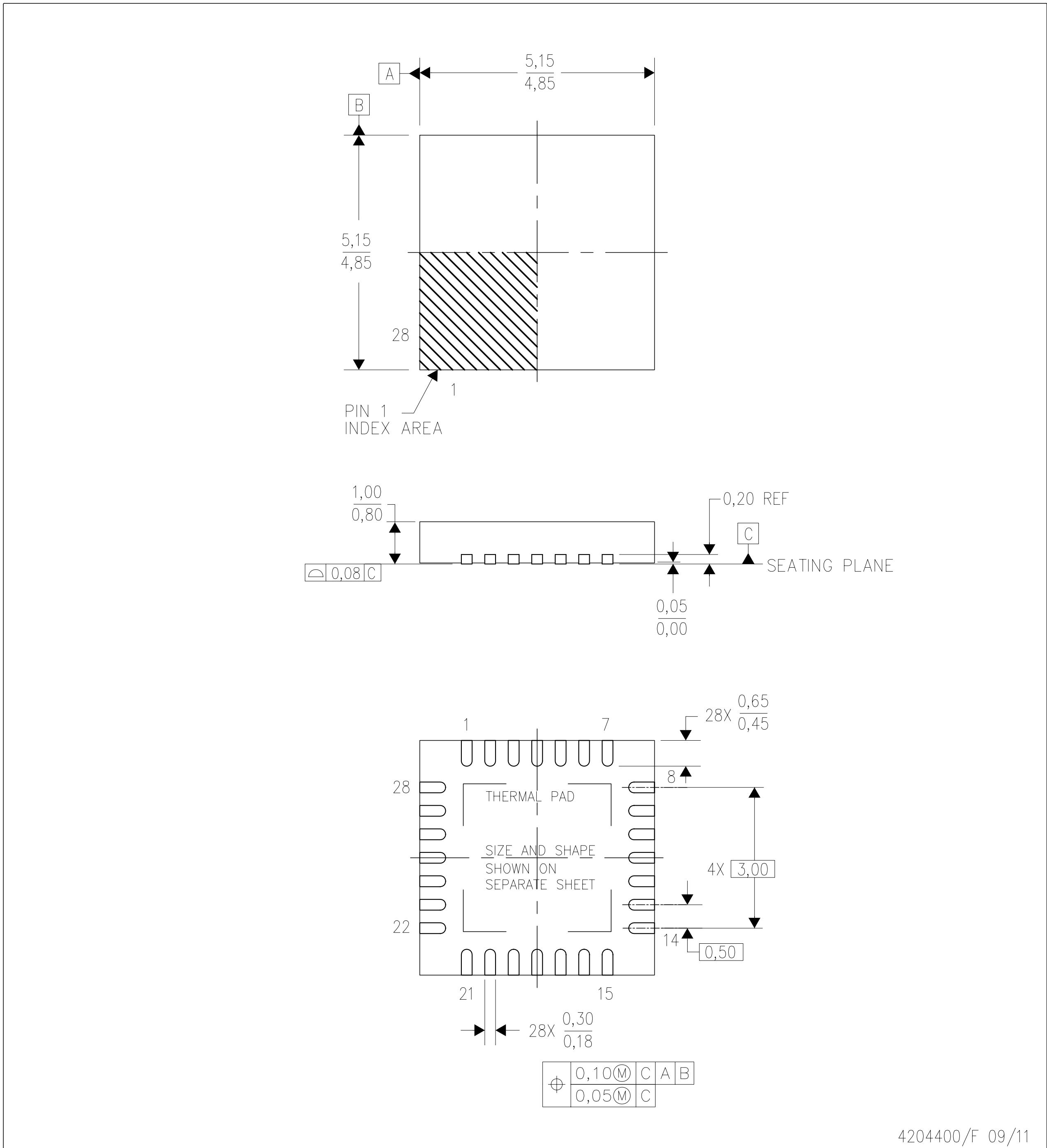



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS65192RHDR | VQFN | RHD | 28 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS65192RHDR | VQFN | RHD | 28 | 3000 | 367.0 | 367.0 | 35.0 |

## MECHANICAL DATA

RHD (S-PVQFN-N28) PLASTIC QUAD FLATPACK NO-LEAD




NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–220.

# THERMAL PAD MECHANICAL DATA

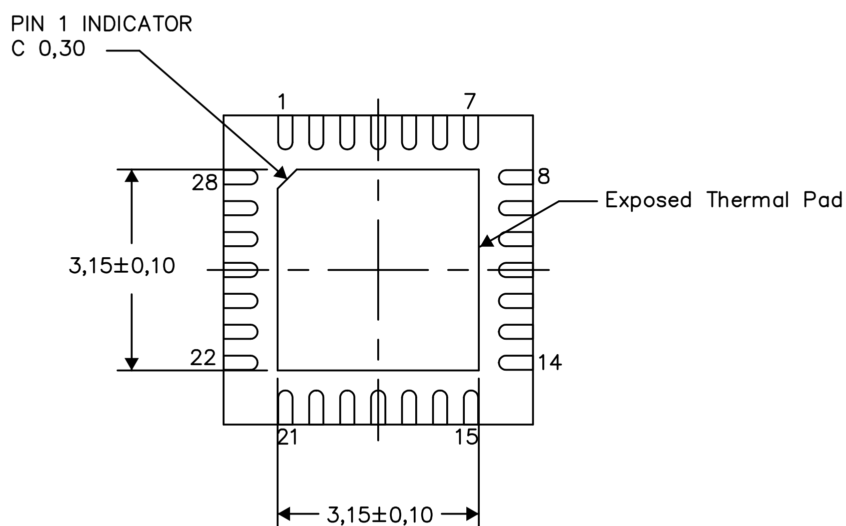
RHD (S-PVQFN-N28) PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Bottom View

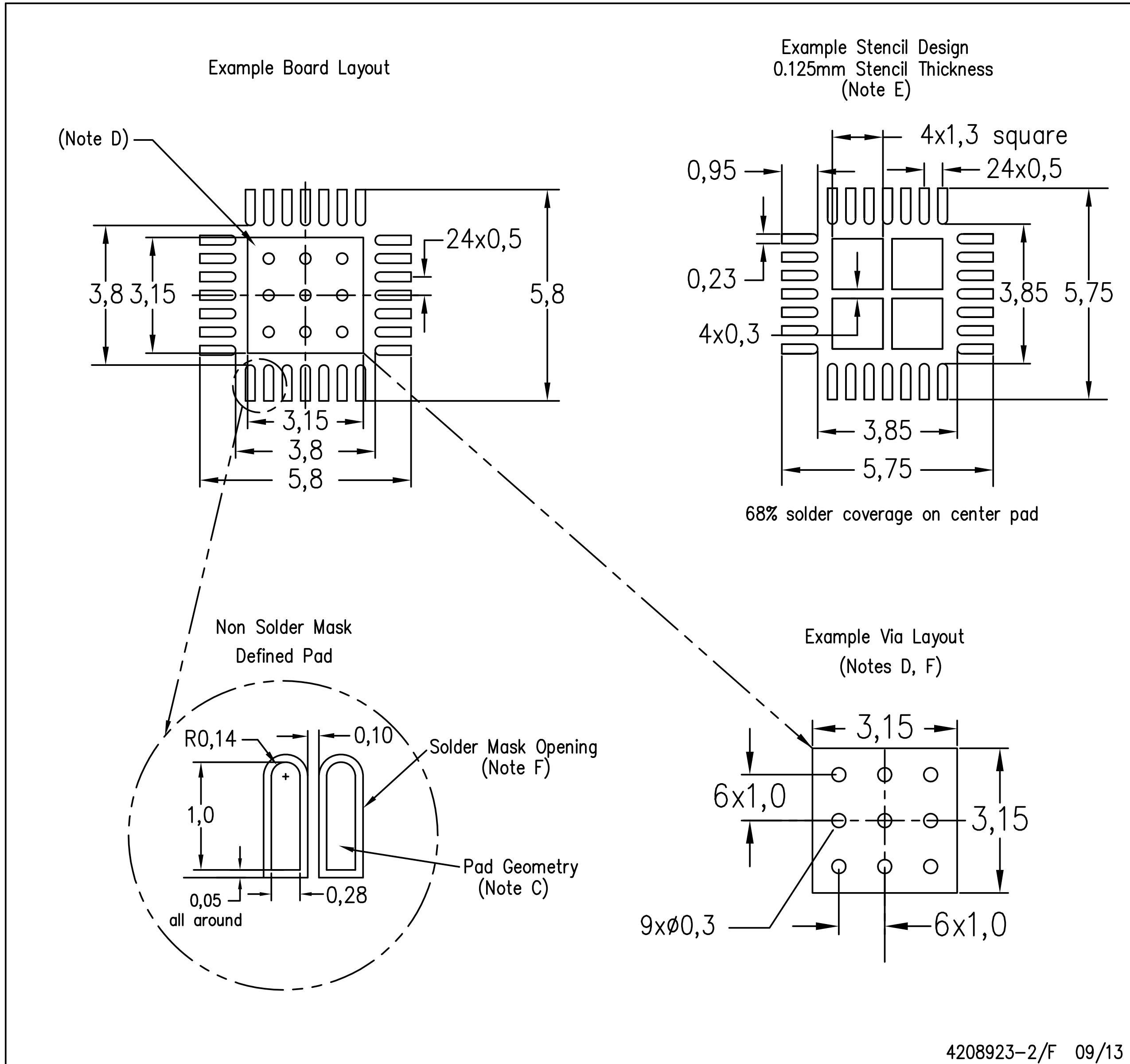
Exposed Thermal Pad Dimensions

4206358-2/J 09/13

NOTE: All linear dimensions are in millimeters

## LAND PATTERN DATA

RHD (S-PVQFN-N28) PLASTIC QUAD FLATPACK NO-LEAD




NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2014, Texas Instruments Incorporated