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[IXYS Corporation](#)

[IXGA90N33TC](#)

For any questions, you can email us directly:

sales@integrated-circuit.com

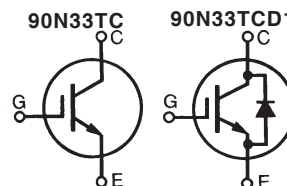

**Trench Gate,
High Speed,
IGBTs**
**IXGA90N33TC
IXGQ90N33TC
IXGQ90N33TCD1**

$$V_{CES} = 330V$$

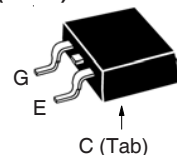
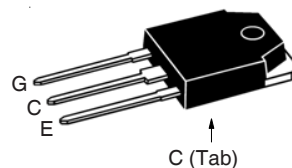
$$I_{CP} = 360A$$

$$V_{CE(sat)} \leq 1.80V$$

For PDP Applications



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ C$ to $150^\circ C$	330	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ C$ (Chip Capability)	90	A
$I_{C(RMS)}$	Lead Current Limit	75	A
I_{C110}	$T_C = 110^\circ C$	38	A
I_{CP}	$T_C \leq 150^\circ C$, $tp \leq 10\mu s$	60	A
I_{CP}	$T_C \leq 150^\circ C$, $tp \leq 10\mu s$, Duty cycle $\leq 1\%$	360	A
P_C	$T_C = 25^\circ C$	200	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ C$
M_d	Mounting Torque (TO-3P)	1.13/10	Nm/lb.in.
Weight	TO-263	2.5	g
	TO-3P	5.5	g

TO-263 AA (IXGA)

TO-3P (IXGQ)

 G = Gate C = Collector
 E = Emitter Tab = Collector

Features

- Low $V_{CE(sat)}$
 - for minimum On-State Conduction Losses
- Fast Switching

Applications

- PDP Screen Drivers

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$	330		V
$V_{GE(th)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	3.0		5.0 V
I_{CES}	$V_{CE} = V_{CES}$, $V_{GE} = 0V$ $T_J = 125^\circ C$			1 μA
				200 μA
I_{GES}	$V_{CE} = 0V$, $V_{GE} = \pm 20V$			± 200 nA
$V_{CE(sat)}$	$V_{GE} = 15V$, $I_C = 20A$, Note 1 $I_C = 45A$ $T_J = 125^\circ C$ $I_C = 90A$ $T_J = 125^\circ C$			1.40 V
			1.54	1.80 V
			1.54	V
			1.82	V
		1.95	V	

IXYS

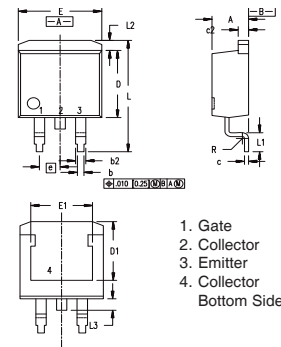
IXGQ90N33TCD1 IXGA90N33TC IXGQ90N33TC

Symbol Test Conditions

($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$I_C = 45\text{A}, V_{CE} = 10\text{V}$, Note 1	40	65	S
C_{ies}	$V_{CE} = 25\text{V}, V_{GE} = 0\text{V}, f = 1\text{MHz}$		2320	pF
C_{oes}			180	pF
C_{res}			21	pF
Q_g	$I_C = 45\text{A}, V_{GE} = 15\text{V}, V_{CE} = 0.5 \cdot V_{CES}$		69	nC
Q_{ge}			15	nC
Q_{gc}			13	nC
$t_{d(on)}$	Resistive Switching Times, $T_J = 25^\circ\text{C}$ $I_C = 45\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 240\text{V}, R_G = 5\Omega$		13	ns
t_r			30	ns
$t_{d(off)}$			38	ns
t_f			49	ns
$t_{d(on)}$	Resistive Switching Times, $T_J = 125^\circ\text{C}$ $I_C = 45\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 240\text{V}, R_G = 5\Omega$		13	ns
t_r			28	ns
$t_{d(off)}$			50	ns
t_f			74	ns
R_{thJC}	TO-3P			0.62 $^\circ\text{C/W}$
R_{thCS}		0.21		$^\circ\text{C/W}$

TO-263 Outline



1. Gate
2. Collector
3. Emitter
4. Collector Bottom Side

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.06	4.83	.160	.190
b	0.51	0.99	.020	.039
b2	1.14	1.40	.045	.055
c	0.40	0.74	.016	.029
c2	1.14	1.40	.045	.055
D	8.64	9.65	.340	.380
D1	8.00	8.89	.280	.320
E	9.65	10.41	.380	.405
E1	6.22	8.13	.270	.320
e	2.54	BSC	.100	BSC
L	14.61	15.88	.575	.625
L1	2.29	2.79	.090	.110
L2	1.02	1.40	.040	.055
L3	1.27	1.78	.050	.070
L4	0	0.13	0	.005

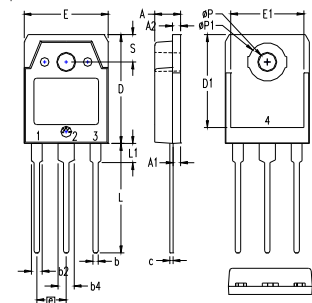
Reverse Diode

Symbol Test Conditions

($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
V_F	$I_F = 20\text{A}, V_{GE} = 0\text{V}$, Note 1			2.0 V
R_{thJC}				2.5 $^\circ\text{C/W}$

TO-3P Outline



- 1 = Gate
- 2,4 = Collector
- 3 = Emitter

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.193	4.70	4.90
A1	.051	.059	1.30	1.50
A2	.057	.065	1.45	1.65
b	.035	.045	0.90	1.15
b2	.075	.087	1.90	2.20
b4	.114	.126	2.90	3.20
c	.022	.031	0.55	0.80
D	.780	.799	19.80	20.30
D1	.665	.677	16.90	17.20
E	.610	.622	15.50	15.80
E1	.531	.539	13.50	13.70
e		.215 BSC		5.45 BSC
L	.779	.795	19.80	20.20
L1	.134	.142	3.40	3.60
ϕP	.126	.134	3.20	3.40
$\phi P1$.272	.280	6.90	7.10
S	.193	.201	4.90	5.10

Note: 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338 B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ 25°C

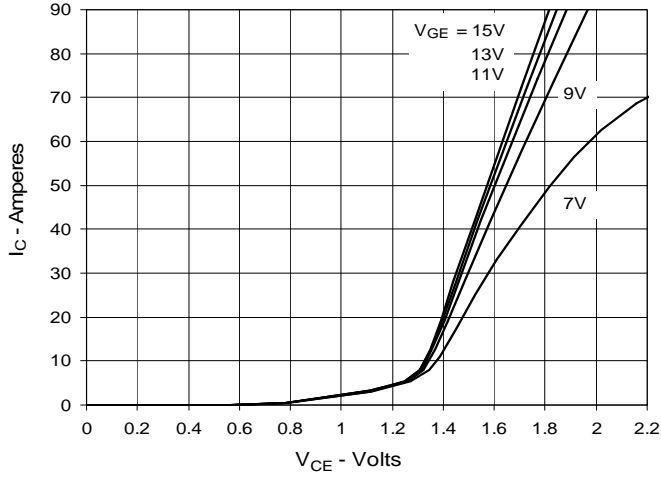


Fig. 2. Extended Output Characteristics @ 25°C

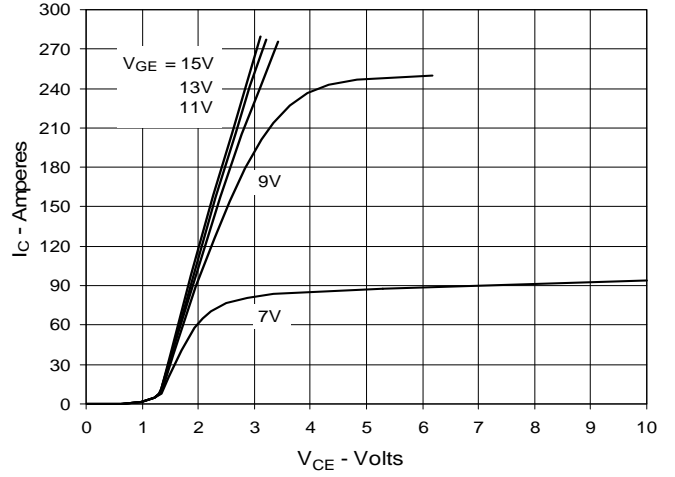


Fig. 3. Output Characteristics @ 125°C

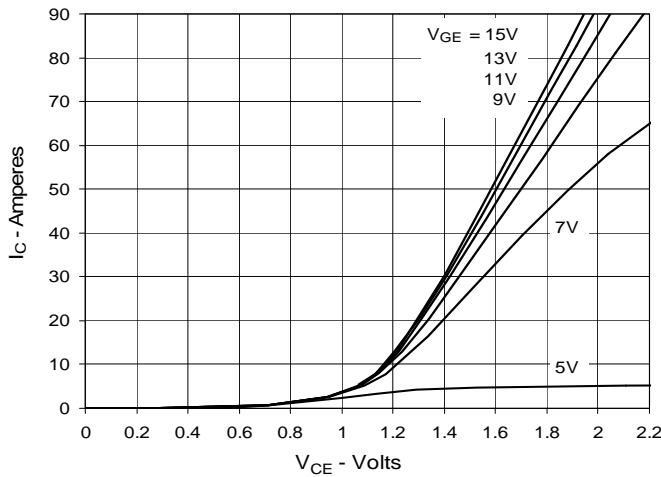


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

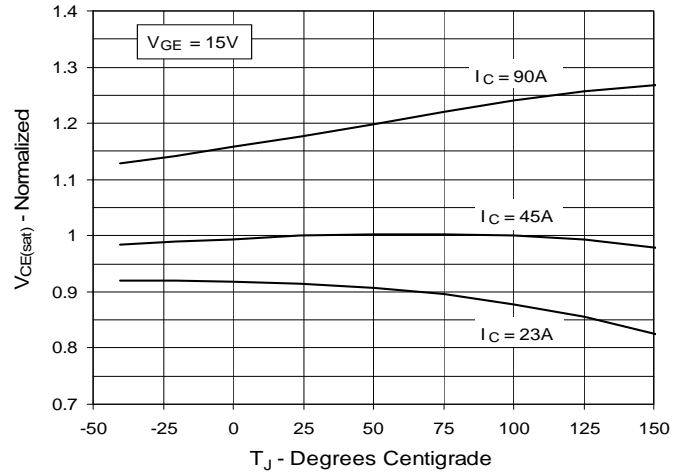


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

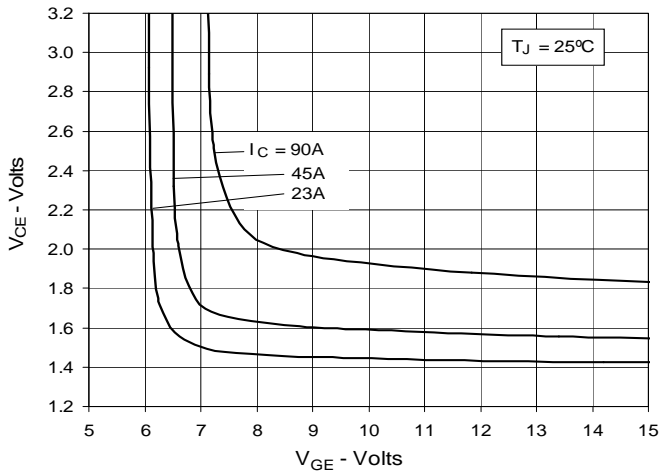


Fig. 6. Input Admittance

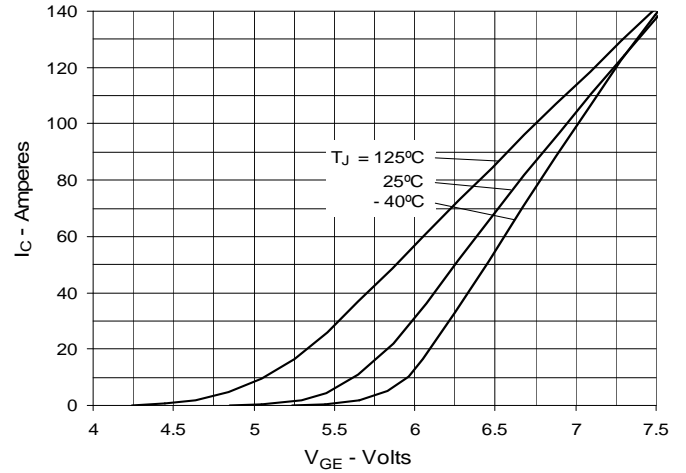


Fig. 7. Transconductance

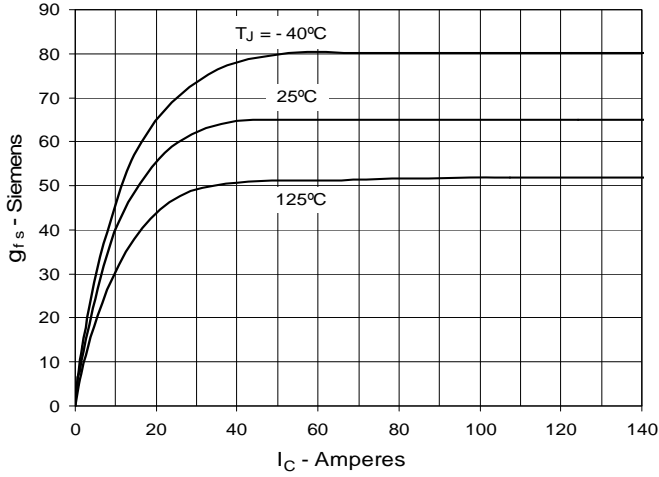


Fig. 8. Gate Charge

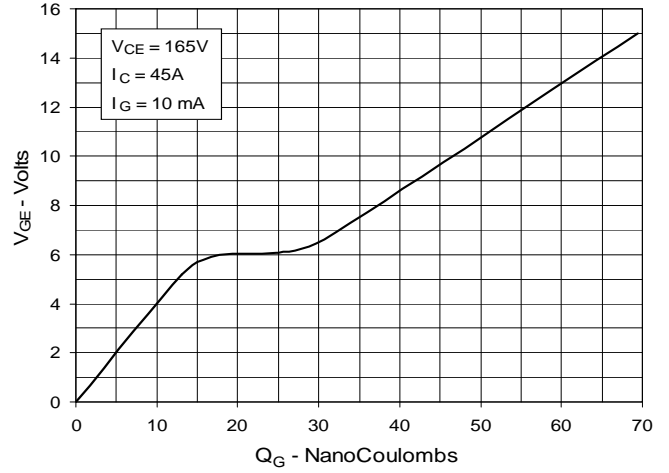


Fig. 9. Reverse-Bias Safe Operating Area

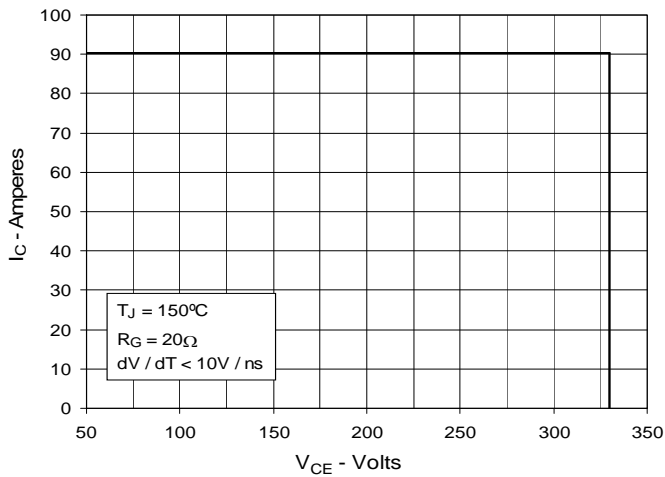


Fig. 10. Capacitance

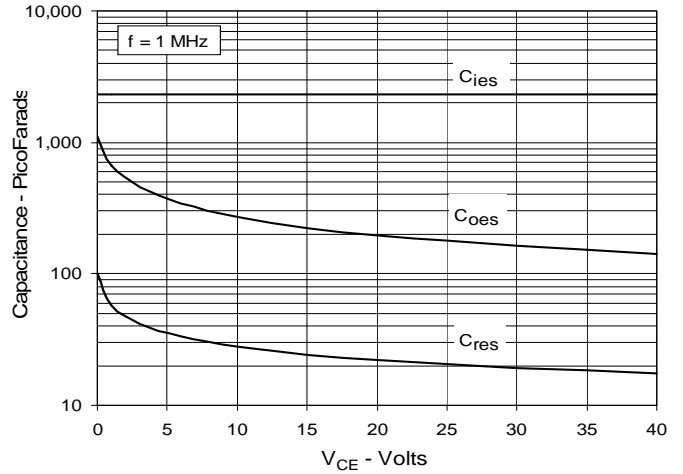


Fig. 11. Forward-Bias Safe Operating Area

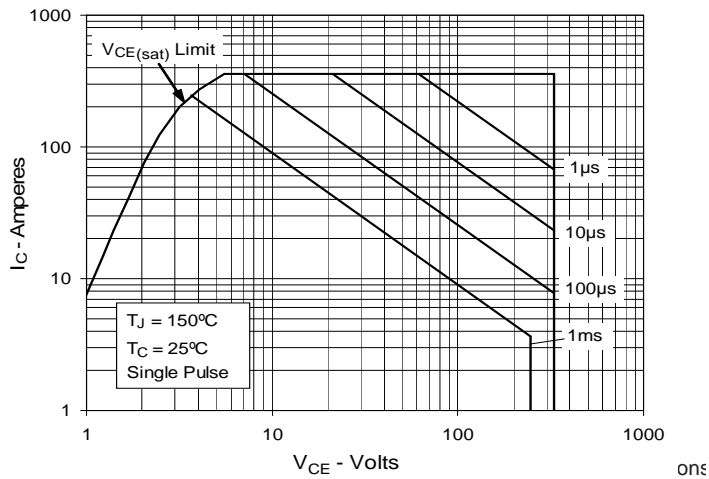


Fig. 12. Maximum Transient Thermal Impedance

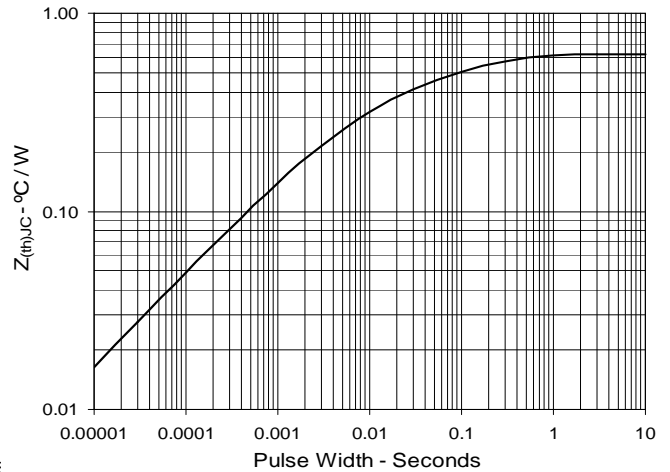


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

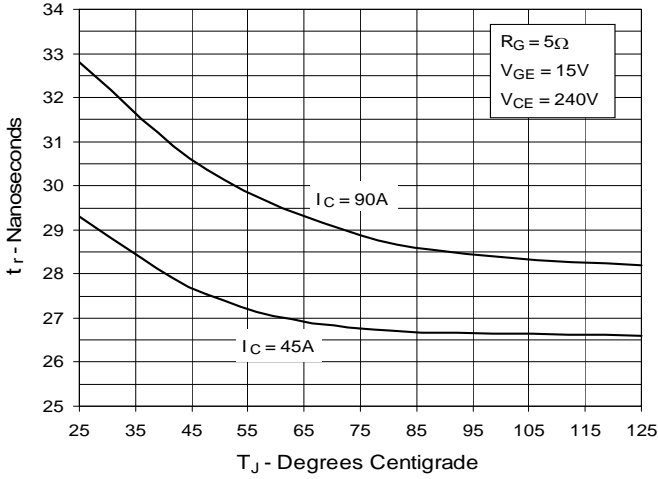


Fig. 14. Resistive Turn-on Rise Time vs. Collector Current

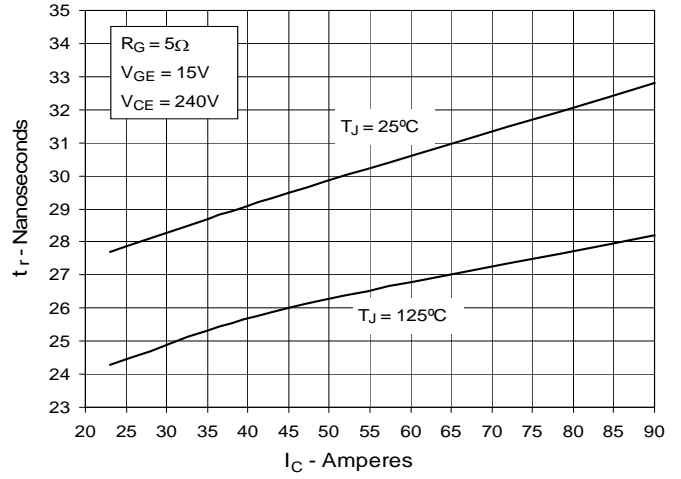


Fig. 16. Resistive Turn-on Switching Times vs. Gate Resistance

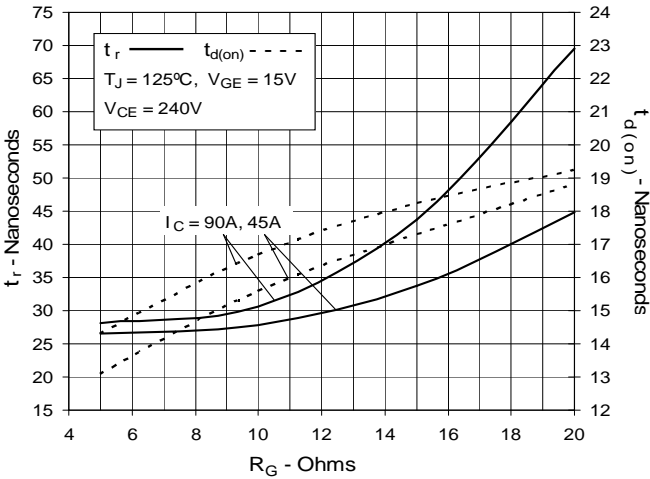


Fig. 17. Resistive Turn-off Switching Times vs. Junction Temperature

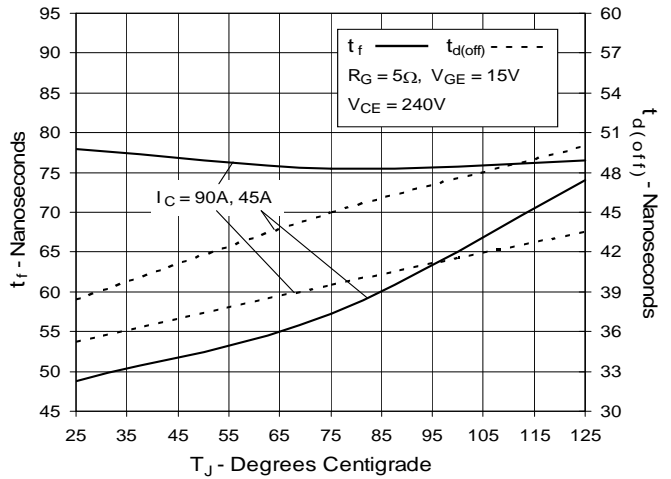


Fig. 18. Resistive Turn-off Switching Times vs. Collector Current

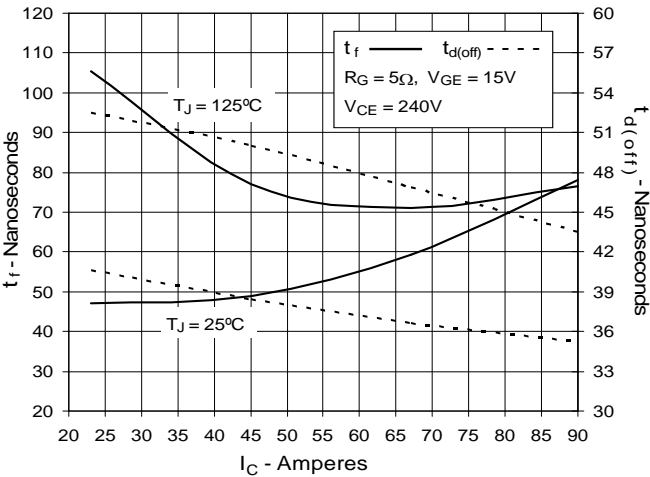


Fig. 19. Resistive Turn-off Switching Times vs. Gate Resistance

